SIEMENS

Small Size, High Performance: Switching with Modern SIPMOS Small-Signal Transistors

According to conventional definitions, the limit values given in data sheets are absolute figures in their own right. If they are exceeded, destruction of the component or sustained impairment of its functions can be expected. But this interpretation is no longer generally accepted nowadays. The Semiconductor Group offers its customers not only avalanche-specified power transistors in SIPMOS technology, but also avalanche-specified small-signal transistors, so that in most cases no special circuitry is needed to limit voltage spikes.

Depending on application, designers can even manage with a smaller chip than before because large safety margins are no longer needed in most applications. This article explains in detail how SIPMOS transistors of SMD design react to pulse-shaped loads.

As the SOA (safe operating area) diagram shows, the application range of SIPMOS transistors is wider in terms of pulse power dissipation values than defined by the DC limit values. The situation is similar for the breakdown voltage of SIPMOS transistors. Whereas the maximum permissible drain-source voltage used to be generally listed under the limit values, today there are several avalanche-specified SIPMOS transistors with which the user can momentarily exceed the minimum breakdown voltage given in the data sheets. In such cases, the breakdown voltage is no longer listed as a limit value, but as an electrical characteristic.

Voltage Strength $V_{BR(DSS)}$ in SIPMOS Small-Signal Transistors

For most SIPMOS transistors, data sheets list the maximum permissible breakdown voltage V_{DSmax} as a limit value. It is up to the designer to give the circuit an adequate safety margin. Avalanche-specified SIPMOS small-signal transistors offer more safety in this respect, because practically the entire voltage range available can be utilized. In many cases, voltage-limiting components such as zener diodes can be dispensed with as long as the permissible avalanche energy is not exceeded. So for normal operation, a transistor no longer has to be overdesigned in terms of voltage. This reduces component costs.

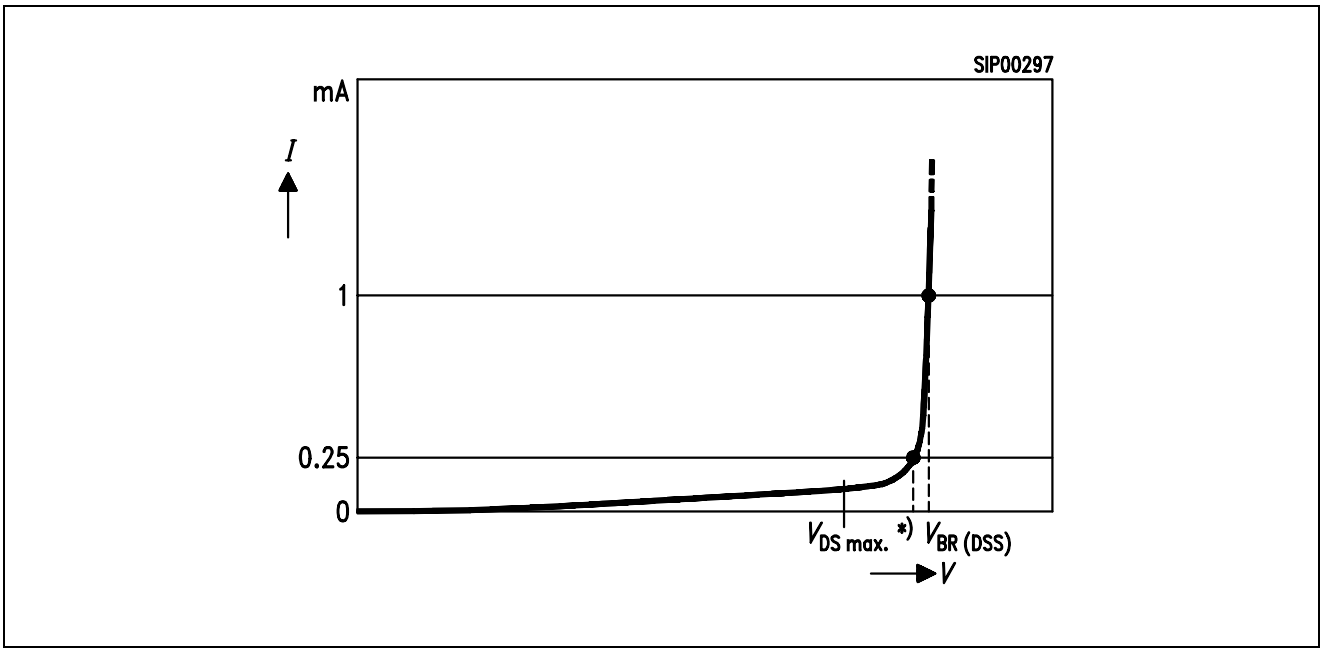

Figure 1
Breakdown Curve Avalanche-specified MOS Transistors
*) Voltage specified in data sheet for 0.25 mA

The curve up to breakdown of a MOSFET is shown in **Figure 1**. The data sheet gives the minimum value for the breakdown voltage $V_{BR(DSS)}$ determined for a drain current of 0.25 mA. At breakdown, the component has, depending on type, a differential resistance, i.e. the breakdown voltage increases with current.

Avalanche-Specified SIPMOS Transistors Cope with Voltage Spikes

The ruggedness of MOSFETs is particularly important to users and a key selection criterion. The need for extra protective circuitry will depend on the energy produced at turn-off. Whereas high-energy voltage spikes at turn-off can usually be limited by appropriate circuit design, it is not so easy to protect against overvoltages coupled in from outside.

Voltage spikes occur at turn-off not only in circuits with inductive loads, but are also produced by the extremely fast switching times of MOSFETs themselves. Parasitic inductances, which are inevitable in any circuit, can cause voltage spikes at turn-off which are higher than the breakdown voltage and can drive a transistor into breakdown. Quite apart from this, voltage transients can be coupled into the circuit from outside. In either case, the energy dissipated in the MOSFET may be enough to cause the component to fail.

Keeping Parasitic Bipolar Transistors Under Control

Where voltage spikes above breakdown voltage are possible, there is the worst-case risk of the parasitic bipolar transistor inherent in the MOSFET being activated, which is almost

invariably synonymous with destruction of the component. So the avalanche limits E_{AR} or E_{AS} given in the data sheets must not be exceeded.

Figure 2 shows a section through a SIPMOS transistor cell and the equivalent circuit diagram. It can be seen here that a vertical N-channel MOSFET inevitably contains a parasitic $n^-p^+n^-$ bipolar transistor.

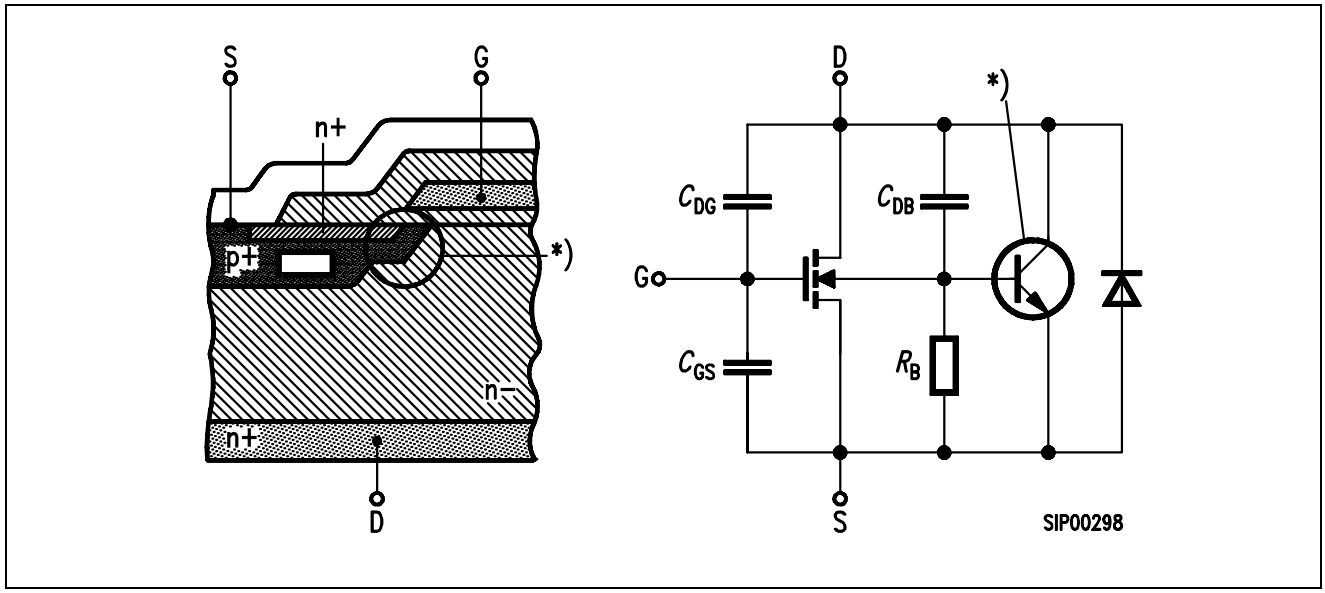

Figure 2
Section Through SIPMOS Transistor Cell and Equivalent Circuit Diagram
The parasitic bipolar transistor *), which is inevitable with this technology, is marked by a circle in the diagram on the left. It must not be activated by excessive turn-off energy

Data Sheet Figures: Dissipated Power not Necessarily Dissipated

The electronics market calls for more and more powerful components that are easier to install. Equipment is becoming more rugged and reliable, while compact systems of high performance can be made at lower cost.

One aspect of SMDs which has been largely ignored to date, but will become more important in the future, is their environmental compatibility – boards equipped with SMDs use less energy and raw materials. Unfortunately, many users still base circuit design on empirical values. A TO-220 package, for example, is often used by habit, although a much smaller SMD package such as an SOT-223 would do just as well. A cursory glance at the data sheet would suggest that the larger package is more appropriate: the total power dissipation P_{tot} for a TO-220 package is listed as 40 to 125 W for a case temperature T_C of 25 °C, while the corresponding figure for an SOT-23, as used in a BSP 17 transistor, is only 1.8 W for an ambient temperature T_A of 25 °C. Such figures are misleading, because they are based on different temperature parameters which cannot be directly compared.

A good example of this discrepancy is provided in **Table 1.** This compares the data for transistors in an SOT-223 package and a D-PAK package (similar to an SMD). The figures in Column I refer to the ambient temperature T_A, the parameter commonly used in Europe,

whereas the figures in Column II refer to the case temperature T_C, which is equally common elsewhere. The reference point (ambient or case temperature) stated in the data sheet affects not only the permissible dissipated power, but, as a consequence, the maximum permissible current as well.

If a D-PAK is considered under the same marginal conditions as an SOT-223 package, however, the D-PAK dissipates only 1.8 W of power instead of the 42 W initially suggested by the data sheet, i.e. the figures *are* comparable. In Column I of the table, the figure of 3.2 A quoted for the current applies to continuous operation. In Column II – with a relatively high current of 15 A – the figure refers to a case temperature of 25 °C. But this is not a realistic value for operation because of the inherent warming that occurs as soon as the component is turned on. If the component, is used on a standard SMD board, where the thermal resistance between case and environment dominates the overall value, a much more authoritative assessment of the devices can be made by comparing the $R_{DS(On)}$ values.

Table 1
Comparison of Data Sheet Figures for MOS Transistor SMD Packages
At first glance, the transistor data in Column II suggests superior performance, especially for power dissipation. But a closer look reveals that the two transistors are comparable in this respect. The reason is the different reference temperature: ambient temperature in Column I and case temperature in Column II

	I: SOT-223 BSP 17 ($R_{DS(On)}$= 0.1 Ω) Parameter: T_A	II: D-PAK Parameter: T_C	
I_D [3]	3.2 [1]	15 [2]	A
P_{tot}	1.8 [1]	42 [2]	W
R_{thJC}	–	< 3	K/W
R_{thJT} [5]	< 3	–	K/W
R_{thJA}	< 70 [4]	< 70	K/W

[1] T_A = 25 °C
[2] T_C = 25 °C
[3] $I_D = \sqrt{\frac{T_J - T_A}{R_{thJA} \cdot R_{DS(on\ 150\ °C)}}}$
[4] Substrate with 2 cm² copper area
[5] R_{thJT} = thermal resistance junction-tab

Pulse Power-Handling Capacity

When pulsed loads are applied, SIPMOS small-signal transistors can handle high peak levels of power dissipation. The maximum permissible junction temperature of 175 °C is not reached until power dissipation is very high as a result of the thermal capacity of the chip and of the package as well. This relationship becomes obvious if it is realized that very short pulses of dissipated power are first “intercepted” by the thermal capacity of the chip, longer pulses by the leadframe as well, and even longer ones by the encapsulation, i.e. by the plastic compound and by any heatsink fitted.

For a short duty cycle, i.e. $D \rightarrow 0$, and a pulse duration of less than 1 ms or so, the chip package is of little consequence. It does not begin to count until a duty cycle of a few percent and pulse duration of more than 1 ms. If the circuit has to be designed to handle momentary overload peaks, packages such as the SOT-223, D-PAK or TO-220 are equally suitable despite differences in dimensions, because all external protective functions will have long been activated within the times stated.

Example of a Short-Circuit

Transistor selected BSP 298, $D \rightarrow 0$ (single pulse), I_D = 2 A, V_B = 80 V, t_P = 40 µs; power P = 160 W. If Z_{th} is 0.05 K/W, temperature increase on the chip ΔT is 8 K.

It will be seen that, regardless of the package design, the junction temperature rises by only 8 K.

Example of the Avalanche Effect

The situation is similar with the avalanche effect. The example here is based on a BSP 17 transistor with an inductive load and the following figures:

V_B = 25 V, I_{AS} = 3 A, L = 1.5 mH, P = 97.5 W, with a dwell time in the avalanche state

$$t_{AV} = \frac{L}{V_{BR(DSS)}} \times I_{AS} = \frac{1.5\ \text{mH}}{65\ \text{V}} \times 3\ \text{A} = 69\ \mu\text{s} \qquad \textbf{equation 1}$$

For a transient thermal impedance Z_{th} of 0.06 K/W and the avalanche dwell time calculated from equation 1, the increase in temperature ΔT is 5.9 K. This example, too, shows relatively slight warming. Package-related differences can only be found with larger pulse duty factors or in DC operation. **Figure 3** shows the transient thermal impedance Z_{th} as a function of the pulse time t_P for different pulse duty factors D.

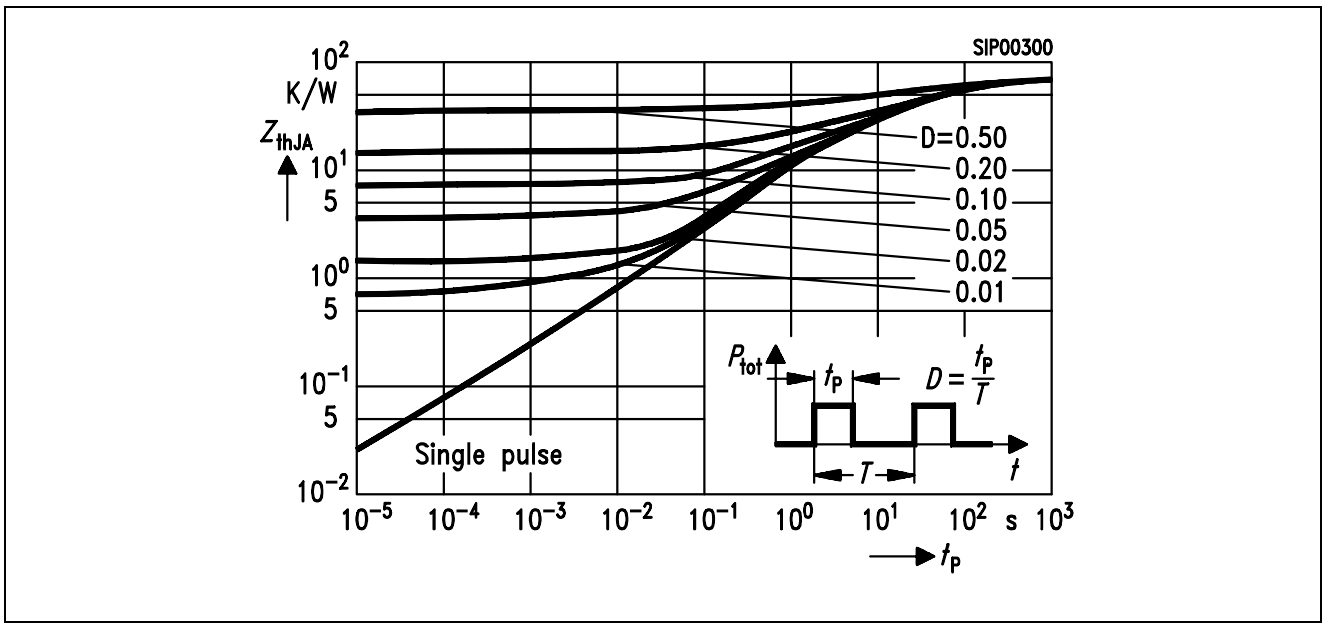

Figure 3
Transient Thermal Impedance Z_{th} as a Function of Pulse Time t_P for SOT-223 and D-PAK Packages: the curves are fully coincident despite different package dimensions

Breakdown Strength

The MIL Std 750 C test method has become common for measurement of avalanche energy. **Figure 4** shows the circuit used for testing avalanche-specified components. The method is identical for power and small-signal transistors. The following procedure is used.

The transistor remains turned on until it reaches its specified avalanche current I_{AV} (at least the rated current). Current rise is linear and determined by the inductance. When the transistor has reached I_{AV}, it is turned off. The voltage on the item under test then rises to the breakdown voltage.

The energy dissipated at breakdown is as follows:

$$E_{AS} = \frac{L \times I_D{}^2 \times V_{BR(DSS)}}{2(V_{BR(DSS)} - V_{DD})}$$ **equation 2**

Two figures are given in data sheets for the avalanche energy:

- avalanche energy, repetitive: E_{AR}
- avalanche energy, single pulse: E_{AS}

The first figure should be viewed as the upper limit when a circuit is designed so that every switching operation leads to an avalanche. In such cases, it must be remembered that extra losses occur, which add to the switching and forward power losses. For the sake of circuit efficiency, it is more appropriate to avoid periodic avalanches with a suitable circuit layout.

The second figure is intended for singular events, i.e. for operating states that can seldom be expected.

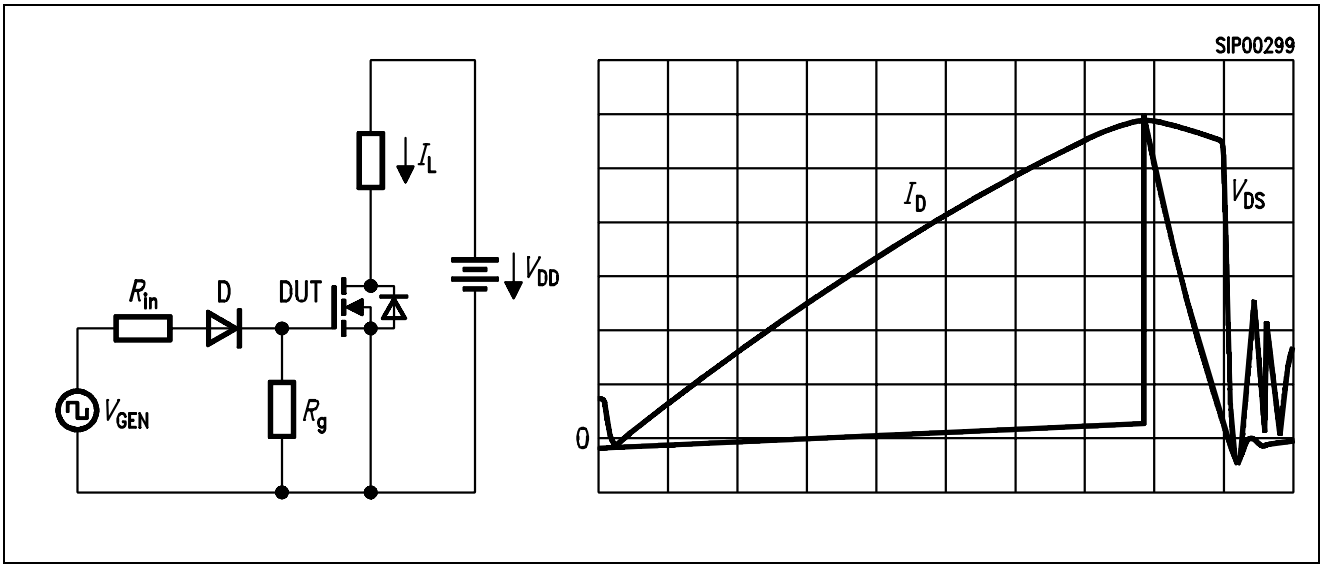

Figure 4
Test Circuit for Measuring Breakdown Strength to MIL Std 750 C (top) and Curves for Drain Current I_D and Drain-Source Voltage V_{DS} (bottom)

Table 2
Selection of Avalanche-Specified SIPMOS Small-Signal Transistors

Type	Polartiy	Package	Breakdown Voltage V	Current A	E_{AR} mJ	E_{AS} mJ
BSP 17	N-channel	SOT-223	50	2.9	1	6
BSP 298	N-channel	SOT-223	400	0.5	4	130
BSP 299	N-channel	SOT-223	500	0.4	4	130
BSP 318	N-channel	SOT-223	60	2.6	1.3	8

Table 2 presents several SIPMOS small-signal transistors for surface mounting together with the permissible avalanche values given in their data sheets. For avalanche-specified SIPMOS transistors, these values are verified before the components are shipped. Types not explicitly listed as avalanche-specified, e.g. the BSS 98 in a TO-92 package, nevertheless have the same features in principle because of the structure of their technology. Users should inquire before ordering.

Table 3
Measurement of Permissible Avalanche Energy E_{AS} on SIPMOS Small-Signal Transistors (not yet specified in data sheets for these types)

Type	Polartiy	Package	Breakdown Voltage V	Current A	E_{AS} mJ
BSS 98	N-channel	TO-92	50	0.3	20
BSS 123	N-channel	SOT-223	100	0.17	15
BSP 296	N-channel	SOT-223	100	1	160
BSP 297	N-channel	SOT-223	200	0.6	120
BSS 89	N-channel	TO-92	240	0.34	14

Table 3 lists the energy values measured in tests on representative transistor types. The breakdown energy that led to destruction of the component was far above these values.
The comparison likewise illustrates the good breakdown characteristics of SIPMOS small-signal transistors in SMD packages.

Conclusions

The ruggedness of these MOS transistors provides an extra margin of safety for circuit design which enhances both quality and reliability. Cost savings also result because the transistors no longer have to be overdesigned and, depending on circuit function and turnoff energy, extra components to limit voltage spikes can be dispensed with.

Unfortunately, the data sheet figures are not standardized sufficiently for direct comparison of different types. Special attention must therefore be paid to the reference temperature on which data for power dissipation and current is based. To sum up: small-signal transistors in SMD packages can cope just as well as larger components with heavy loads of short pulse duration.