SIEMENS

SITAC: An Optocoupler AC-Switch

Introduction

The new SITAC AC switch (SITAC = Siemens Isolated Triac AC switch) in SIPMOS technology provides an optically isolated interface between microelectronics and AC power electronics. Its voltage capability and interference immunity are adequate for 110-V and 220-V lines; the required voltage range for 380-V lines can be increased by connecting two devices in series. The input sensitivity is so high that – if the gate trigger delay time t_{GD} is not critical – the SITAC can be directly driven by the microcomputer.

For applications requiring electrical isolation between line and load side, the SITAC is ideal as a replacement for conventional optocoupler circuits because neither auxiliary voltages nor driver transistors are necessary on the line side. With a zero voltage switch the SITAC is used in AC switches and three-phase converters whereas single-phase and line-commutated converters employ the version without zero voltage switch. Special note should be taken of the SITACs high critical rates of current and voltage rise of $\mathrm{d}i/\mathrm{d}t$ = 10 A/µs and $\mathrm{d}v/\mathrm{d}t$ = 10 kV/µs that obviate the need for RC networks.

Using the schematic diagram as a basis, the advantages of the SITAC as a semiconductor switch and a driver module for power thyristors are described below. In addition, its switching performance, particularly in phase control circuits, the trigger pulse current and high rates of current rise are discussed. A very important electrical characteristic is the performance at high rates of voltage rise as are found in phase control, for instance. For 380-V line applications it is demonstrated how the voltage range can be increased by connecting 2 SITACs in parallel. The plotted voltage-time curve shows the possible maximum voltage amplitude for 380-V line operation, and the possible maximum rate of voltage rise.

Principle of the SITAC AC Switch

The SITAC (**Figure 1a**) consists of such familiar components as a GaAs infrared diode on the input side and a photodetector and triac on the output side. As can be seen from the figure, this provides electrical isolation between the control and load circuits, i.e. the result is an infrared triggered AC switch which can be used as an autonomous AC switch for low-power loads (including phase control) and as a driver module for power thyristors in the high-power range.

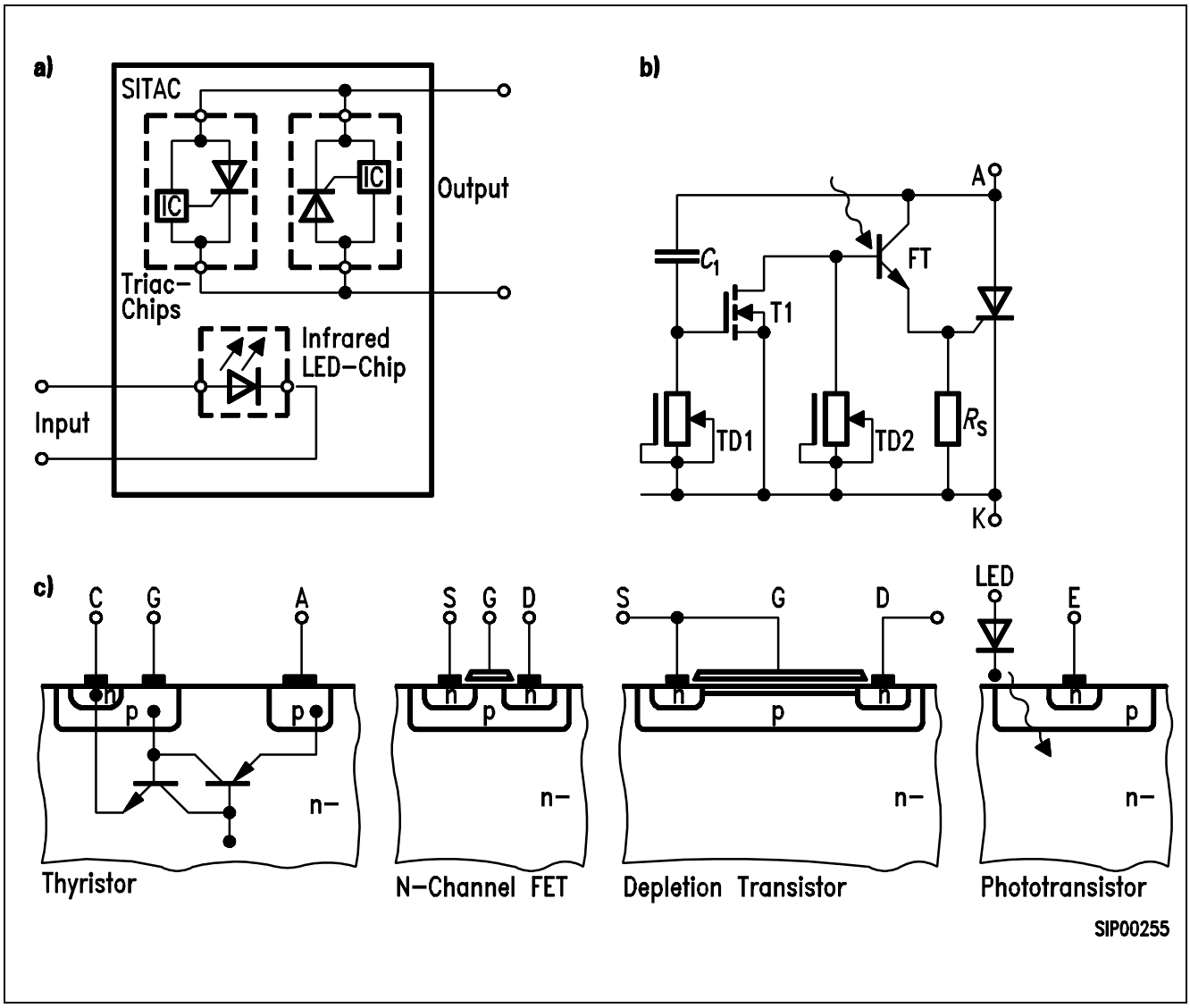

Figure 1
Principle of the SITAC
a) Block Diagram of the SITAC Opto-Triac
b) Circuit Diagram of a SITAC Branch
c) SITAC Semiconductor Branch Elements

Figure 1b shows the electrical principle of a SITAC branch. A semiconductor chip accommodates the functional units thyristor, MOSFET and phototransistor. **Figure 1c** shows the basic elements of the SITAC; lateral thyristor, n-channel FET as a switch, depletion transistor as a variable resistor, and phototransistor with LED as a driver module.

Resistor R_B is a shunt in the control circuit, designed to ensure a satisfactory dv/dt relation. But this reduces the turn-on sensitivity. This effect is compensated for by the addition of an auxiliary thyristor whose trigger current is supplied – and thus increased – by the phototransistor (FT). The auxiliary thyristor is embedded in the p-n/p-n structure of the main thyristor in such a manner that only the latter needs to be driven into conduction by the FT.

The resulting trigger pulses are extended to the n-p regions arranged on both sides of the auxiliary thyristor so that part of the hole current thus produced is diffused into the auxiliary thyristor's p-region, and cathode emission is initiated. This process reduces the dv/dt sensitivity of the main thyristor.

Phototransistor FT is connected on its collector side to the n-base of the thyristor array. It receives its current via this diode path if the thyristor anode has the correct polarity. In order to reduce the reverse current in the phototransistor, which my lead to the auxiliary thyristor being turned on when specific limits are exceeded, a variable base-emitter shunt is used. The circuit connected to the anode of the thyristor – consisting of capacitor C_1 and depletion transistor TD1 which acts as a resistor – protects the dv/dt reaction. This resistor is used to set the current limiting point using the pentode characteristic of the FET. A rise in voltage across TD1 caused by a voltage swing at the thyristor T1 turns on bridging the gate path of the auxiliary thyristor.

The SITAC is, moreover, equipped with a zero voltage control facility. To activate the control signal, a minimal anode voltage must be present at the thyristor so that the threshold voltages for all elements of the trigger circuit are exceeded. When the zero voltage switch is activated, the static control limit is about 6 – 7 V, which means that the anode voltage range in which static control is possible is between 2 and 7 V. Where the SITAC replaces a semiconductor relay, the zero voltage switch is necessary to reduce interference. For implementing phase control, the zero voltage switch must not be used. Due to the SITACs insensitivity to dv/dt, it is possible to select any angle required for phase control.

SITAC Areas of Application

The two most important areas of application are:

– Electrically isolated AC semiconductor switches to replace relays
– Electrically isolated driver circuits for power thyristors, e.g. in single-phase or three-phase AC converters

A comparison between conventional AC semiconductor switches and SITACs indicates the improvements which can be achieved. **Figure 2** shows a SITAC as an AC switch for converting low power.

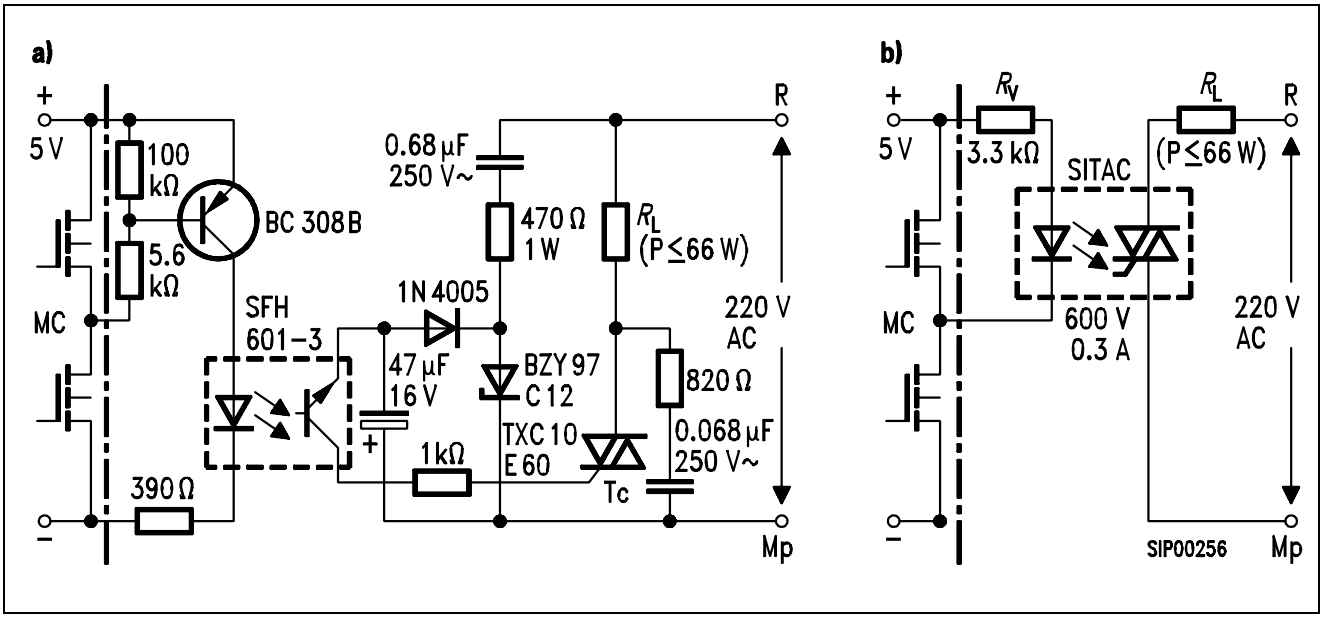

Figure 2
Semiconductor Switch for Converting AC Power
a) Drive Circuit with Microcomputer Interface for Conventional Triac using Discrete Components and Optocouplers
b) IC Interface Circuit with the SITAC

Comparison Between the Two Circuits Shown in Figure 2 with Respect to Electrical Data and Components

Figure 2a

- Electrical isolation through optocoupler
- Elaborate RC network to protect triac dv/dt sensitivity
- Drive power drawn from load circuit
- Higher dissipation in circuit due to RC network
- High component count
- Circuit not integratable
- Not hybrid-capable due to large-value resistors and capacitors
- Optimum component availability

Figure 2b

- Electrical isolation through optotriggered triac
- No RC network due to high dv/dt compatibility
- Few components
- Operable without zero voltage switch: phase control possible
- High di/dt loadability
- High input sensitivity and noise immunity
- Series connection no problem
- Modular structure no longer suitable due to low component count
- Available in DIP-6 package
- Insulation test vortage 5.3 kV
- Switchable power up to 66 W at 220-V line (I_{RMS} = 300 mA)

In addition to a semiconductor switch on the 220-V line side, the SITAC can also be employed as a driver module for power thyristors in single-phase or three phase AC circuits as per **Figure 3**. Because of its high trigger pulse current and high d*i*/d*t* values, the SITAC is also eminently suited to driving power thyristors at low delay times. The current-carrying capability of the SITACs thyristor chip for current pulses of 5 to 10 µs duration, as are found in thyristor trigger circuits, is – depending on the rate of current rise – 5 A at a chip temperature of 80 °C and a line frequency of 50 - 60 Hz. The d*i*/d*t* limit is around 10 A/µs. The current-carrying capacity is reduced to 5 A for current pulses of up to 100 µs duration, and, for pulses of greater duration, depends on the on-state power dissipation permissible for the particular junction temperature. Trigger circuits for high blocking capability thyristors operating at line voltages of 380 V or more can be implemented by connecting SITACs in series.

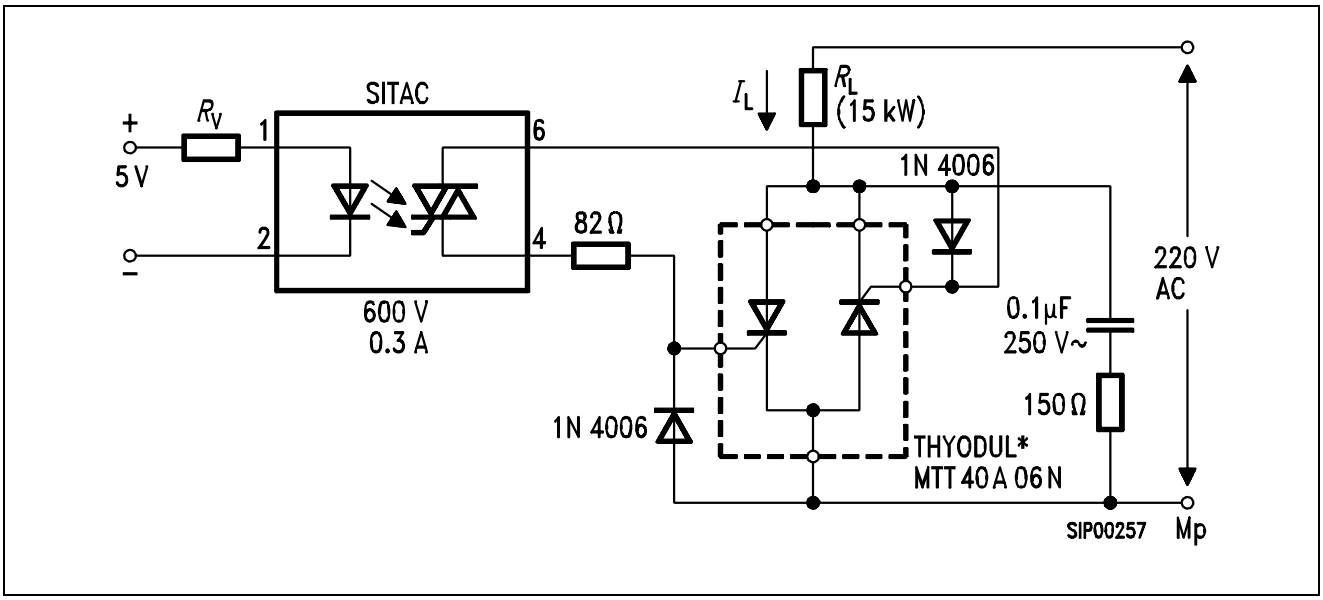

Figure 3
SITAC Used as a Driver Module for a Power Thyristor

Electrical Characteristerics of the SITAC

The most important electrical characteristics of the SITAC and their influence on the switching performance are discussed below.

a) Forward Trigger Current I_{FT}

As can be seen from **Figure 4**, the forward trigger current of the SITAC has a positive temperature coefficient ($TC \approx 5.5 \times 10^{-3}$ mA/°C). This thermal characteristic in conjunction with operating temperature of the system are fed into a control loop which makes it possible, for instance, to achieve a specific phase angle by simply varying the magnitude of the control current. When the operating temperature rises, arrays with a usually negative temperature coefficient of forward current, such as standard phase control thyristors and triacs, automatically take action to improve trigger performances and increase turn-on speed. Moreover, the forward trigger current of the SITAC also depends to some extent on the anode voltage. A higher anode voltage causes the current to fall ($I_{FT} \approx$ 1.3 mA/V_A = 30 V $\rightarrow$ $I_{FT} \approx$ 1 mA/ V_A = 500 V). When current pulses are used for triggering the SITAC the minimum pulse duration must be selected to suit the turn-on time resulting from the particular operating conditions.

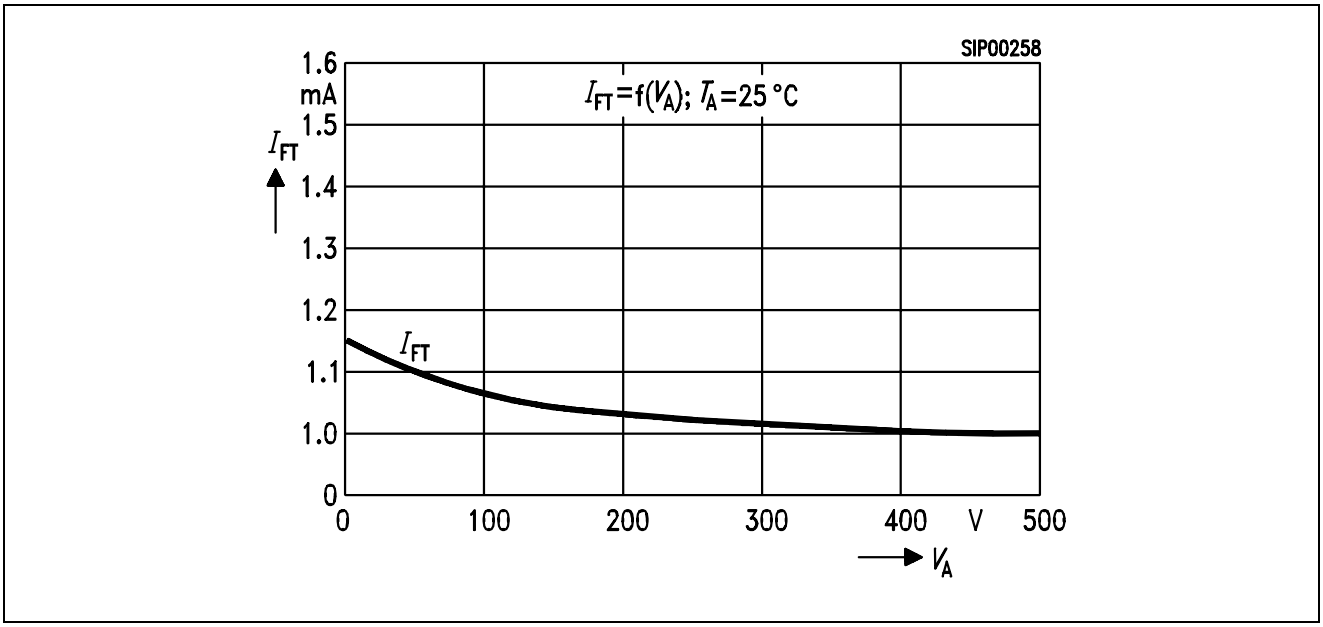

Figure 4
Forward Trigger Current I_{FT} as a Function of Temperature

b) Gate Trigger Delay Time t_{GD}

Figure 5 shows the gate trigger delay time t_{GD} as a function of the turn-on overdrive factor for different temperatures. As the junction temperature increases the turn-on time increases as well because – with the forward current I_F remaining equal and the forward trigger current I_{FT} rising with temperature – the overdrive ratio I_F/I_{FT} is reduced. In the event of excessive overdrive, the turn-on time curve approaches its asymptote, which explains the decreasing influence of temperature in this region. The turn-on time may rise into this millisecond range when the I_F/I_{FT} ratio is less than 1.1. This must be taken into consideration if the SITAC is directly accessed from the microcomputer IC.

The gate trigger delay time t_{GD} and gate controlled rise time t_{GR} are determined by the applied anode voltage, with t_{GD} and t_{GR} rising at a more than proportional rate for V_A < 20 V and V_A < 200 V respectively.

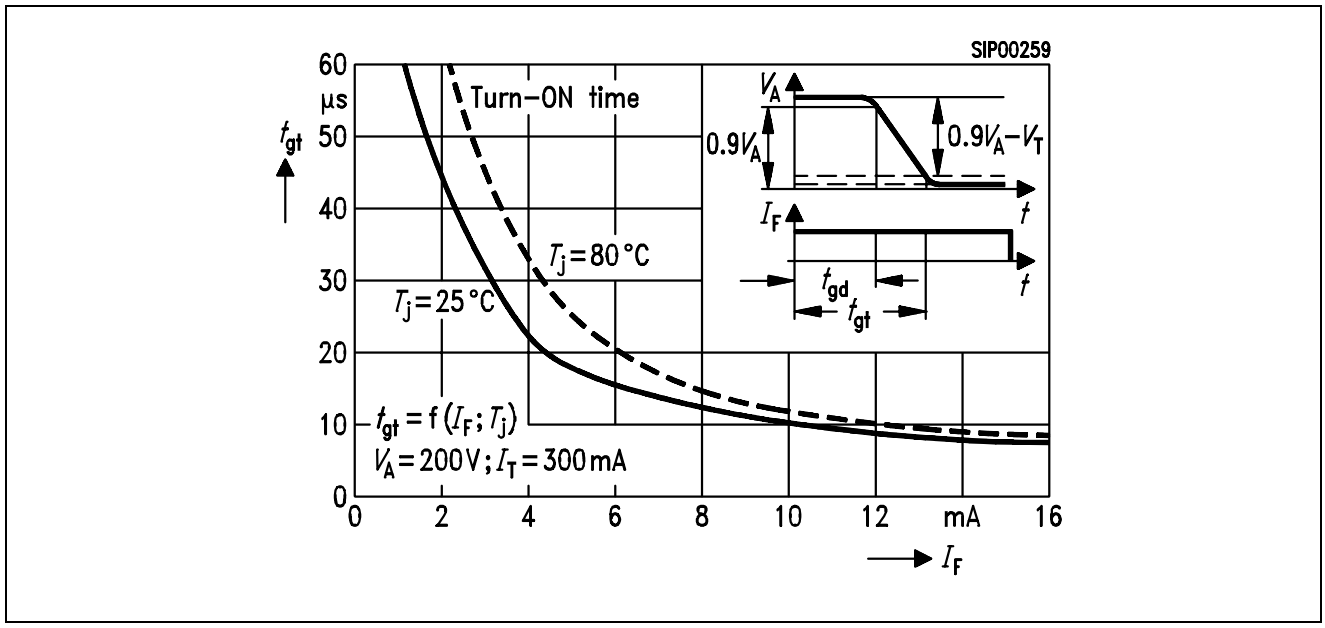

Figure 5
Turn-on Time as a Function of Trigger Current for Different Junction Temperatures

c) Maximum Operating Frequency

The SITACs maximum operating frequency $f_G = f(\hat{i}_T, L, \vartheta)$ is a function of pulse current, load inductance and temperature. As shown in **Figure 6**, a maximum clock frequency of 5 kHz is possible for the SITAC. This frequency range is limited by the magnitude of load current $\hat{i}_T$ and inductive load L. These parameters in turn influence the frequency-determining recovery time. The magnitude of the current determines to a large extent the junction temperature, the rate of current rise at commutation, and, in conjunction with the inductive component, the rate of voltage rise at the SITAC after current turn-off, raising the voltage to an excessive level. It should be noted in this context that the ratio of junction temperature to the dissipated power is given by the total thermal resistance of the SITAC ($R_{th\ JAmax} \approx 150$ K/W).

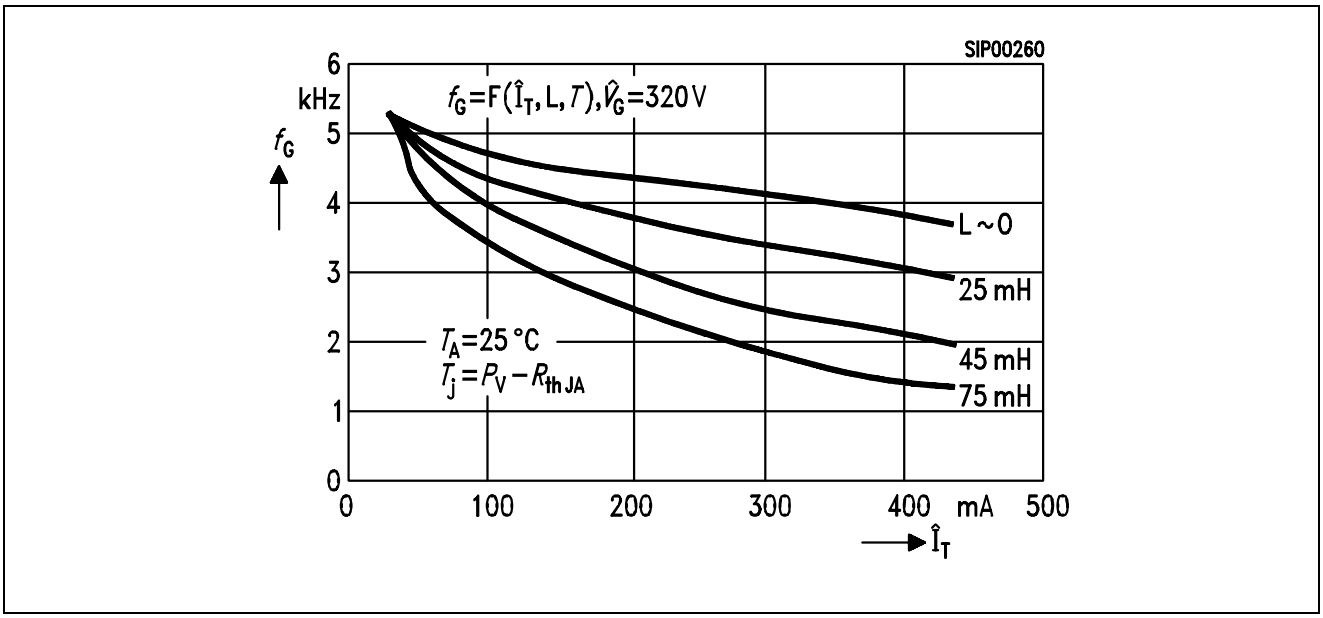

Figure 6
Maximum Operating Frequency as a Function of Trigger Pulse Current for Different Load Inductances

d) Trigger Pulse Current I_{TP}

In addition to the pulse current produced by a single 50-Hz half-wave, for which a maximum rating of 5 A is specified in the data sheet, most applications must be capable of withstanding repetitive operation and high intensity current pulses. A typical example is the SITAC used as a driver module for power thyristors or triacs. In this case, the SITAC is connected on its output side between gate and anode of the power switch to be triggered, and carries the full output circuit current for as long as the switch is turned on. The flow and turn-on dissipation are at a maximum when triggering occurs at the maximum voltage point. For this reason, a check should be made in each case to see whether a current limiting resistor matched to the trigger pulse current of the SITAC is required in the control circuit.

Figure 7 shows the trigger pulse current as a function of pulse duration for a frequency of 50 Hz. The specified pulse currents can be attained up to rates of current rise of di/dt = 10 A/µs. The diagram shows the hyperbolic power dissipation characteristic of the SITAC (0.3 W per half-wave). For pulses that are longer than 100 µs (10^2-10^4) the I_{Tp} is determined by the total power dissipation. If the pulse duration is less than 100 µs (10^1-10^2), the trigger pulse current – at di/dt 10 A/µs is – determined by primary effects in the component itself (not by the hyperbolic power dissipation curve). The maximum trigger pulse current at a rate of current rise of 10 A/µs is I_{Tp} = 5 A.

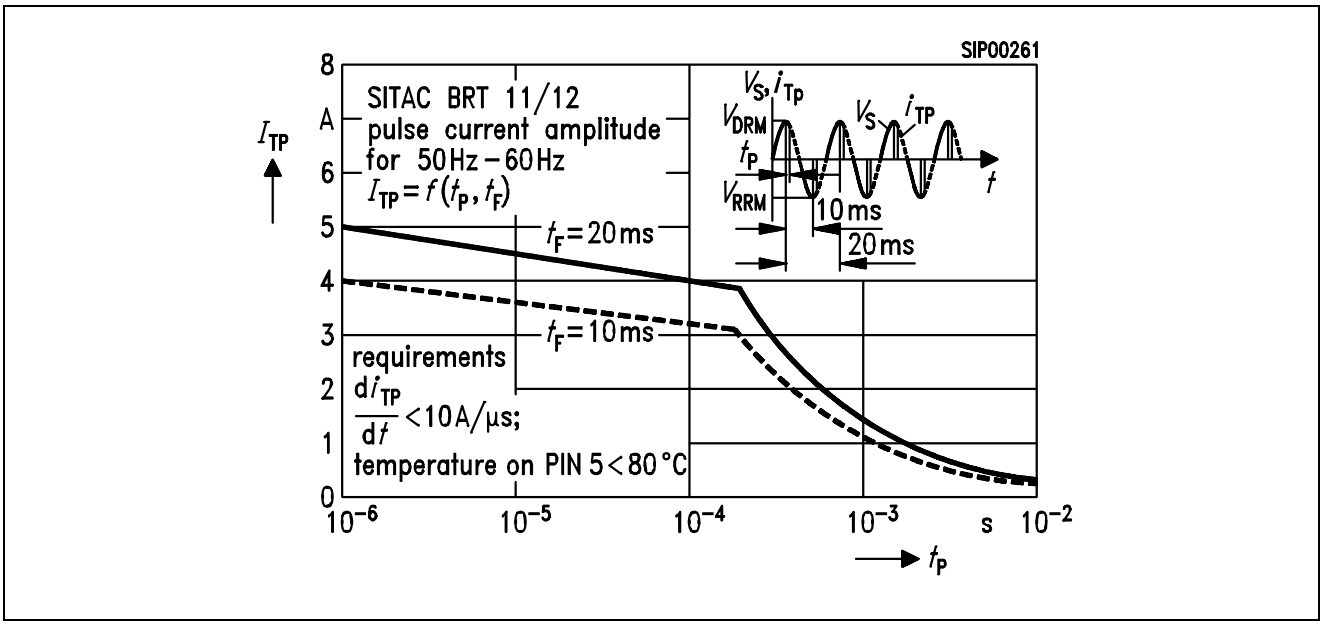

Figure 7
Trigger Pulse Current as a Function of Pulse Duration for 50 - 60 Hz Half and Full Cycles at Rates of Current Rise of 10 A/µs

Maximum Available Reverse Voltage and d*v*/d*t* Load of a SITAC when Used in 220-V and 380-V Lines

In circuits where inductive loads are switched and, consequently, current and voltage are 90° out of phase, the voltage is at a maximum whenever the current passes through zero (see **Figure 8**). The maximum voltage $\hat{V}_S$ a SITAC is exposed to in 220-V and 380-V circuits is discussed in the following.

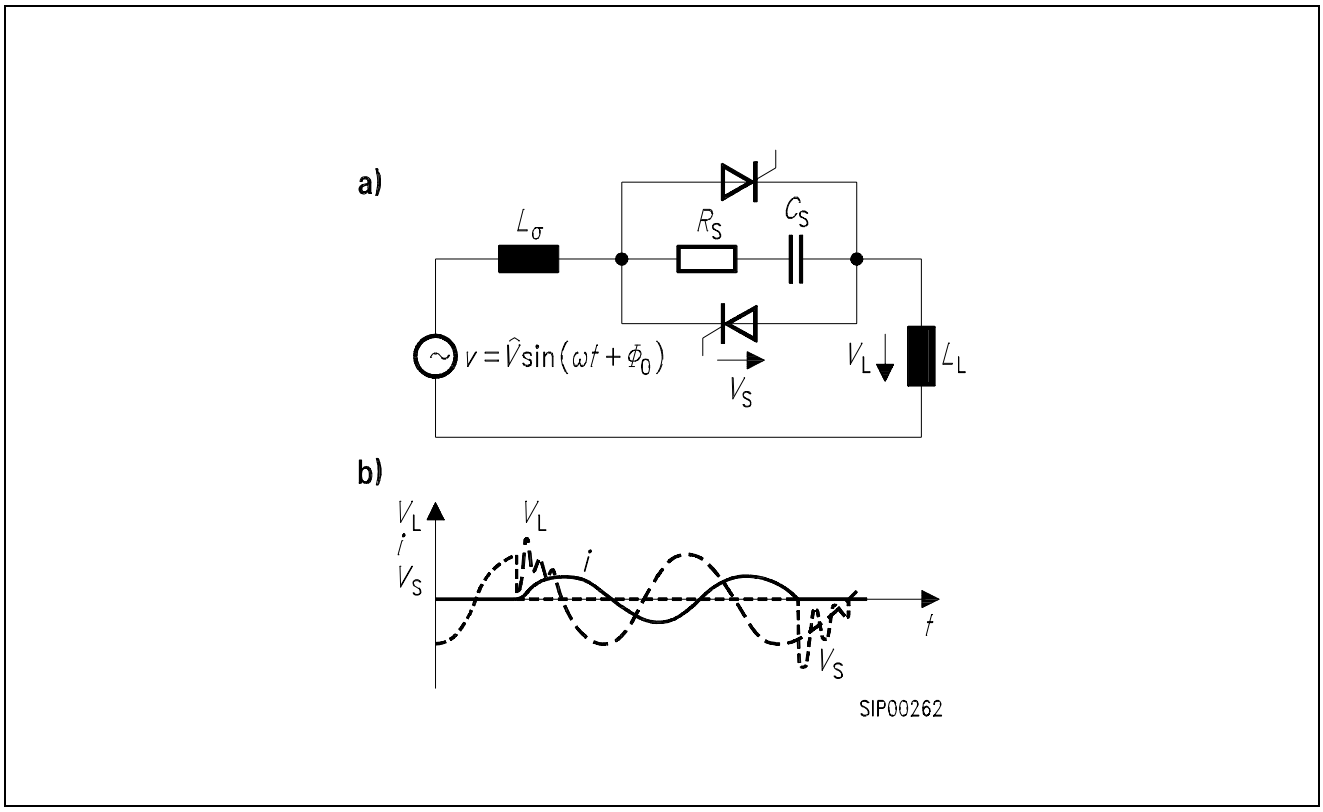

Figure 8
SITAC Used as an AC Switch in a Network
a) Single-phase AC Converter Circuit with Sinusoidal Input
b) Curves for Load Current i_L (t), Load Voltage v_L(t), and Semiconductor Voltage v_S (t)

As is evident in **Figure 8**, a transient oscillation of medium frequency is superimposed on the load voltage $v_L(t)$ as soon as the SITAC turns on at zero current point (disregarding the transient current) as a result of the parasitic capacitances C_P (winding and semiconductor capacitances) and parasitic inductance L_σ. The radian frequency of this oscillation is approximately $\frac{1}{\sqrt{L_\sigma C_P}}$. In this case (purely inductive load), the critical point is when the semiconductor switch is turned off since the supply voltage is at a maximum at this moment. The voltage across the semiconductor switch is $v_S = v_{RB} + v_{CB}$. In case switching is effected as the current passes through zero, $v_{RB} \approx 0$ and consequently $v_S \approx v_{CB}$. Since the semiconductor switch is turned off the condition $v_S \approx 0$ V applies.

Generally, this can be expressed by the following formula:

$$\frac{V_S}{\hat{V}} = -\frac{2\alpha\omega\omega_0}{(\omega_0^2 - \omega^2)^2 + 4\alpha^2\omega^2}\cos(\omega t + \phi_0) + \frac{\omega_0^2(\omega_0^2 - \omega^2)}{(\omega_0^2 - \omega^2)^2 + 4\alpha^2\omega^2}\sin(\omega t + \phi_0)$$

$$+ \frac{e^{-\alpha t}\omega_0^2}{2\omega_e}\left[\frac{\alpha\cos(\omega_e t + \phi_0) + (\omega - \omega_e)\sin(\omega_e t + \phi_0)}{\omega_0^2 - 2\omega\omega_e + \omega^2}\right.$$

$$\left. - \frac{\alpha\cos(\omega_e t - \phi_0) - (\omega + \omega_e)\sin(\omega_e t - \phi_0)}{\omega_0^2 + 2\omega\omega_e + \omega^2}\right] \qquad \textbf{equation 1}$$

where attenuation $\alpha = \frac{R_B + R'}{2(L_\sigma + L)}$

and chararcteristic frequency: $\omega_0^2 = \frac{1}{(L_\sigma + L)(C_B + C')}$

(R' = parasitic resistance in the circuit; C' = parasitic capacitance).

It can already be seen from the above equation that the semiconductor switch is connected to the available line voltage $v(t)$ upon which an attenuated voltage of a higher frequency is superimposed. The general expression (1) comprises the following equations:

$$\frac{V_S}{\hat{V}} = \left(\frac{V_S}{\hat{V}}\right)_\infty + \left(\frac{V_S}{\hat{V}}\right)_f \qquad \textbf{equation 2}$$

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Forced oscillation — Free-running oscillation

It follows from equation 2 that

$$\left(\frac{V_S}{\hat{V}}\right)_\infty = \frac{1}{\omega C}\frac{-\cos(\omega t + \phi_0 + \phi)}{\sqrt{\left(\frac{1}{\omega C} - \omega L\right)^2 + R}} \qquad \textbf{equation 3}$$

where $\phi = arc\ tan\left(\frac{\frac{1}{\omega C} - \omega L}{R}\right)$

and $C = C_B + C'$; $R = R_B + R'$; $L = L_\sigma + L$ **equation 4**

In case the line frequency is much lower than the characteristic frequency, which applies here,

$\omega << \omega_0$

The ohmic resistance is low, so

$\omega << \omega_0$; $\omega_0 \approx \omega_e$

Consequently,

$$\left(\frac{V_S}{\hat{V}}\right)_\infty \approx \frac{-\cos(\omega t + \phi_0 + \phi)}{\sqrt{1 + \underbrace{4\frac{\alpha^2\omega^2}{\omega_0^4}}_{\text{very small}}}} \approx -\cos(\omega t + \phi_0 + \phi) \qquad \textbf{equation 5}$$

where $\phi = arc\ tan\ \frac{\omega_0^2}{2\alpha\omega} \approx \frac{\pi}{2}$

Thus, we obtain for the forced component

$$\left(\frac{\hat{V}_S}{\hat{V}}\right)_\infty \approx \sin(\omega t + \phi_0) \qquad \textbf{equation 6}$$

i.e. the steady-state switch voltage equals the line voltage.

For the transient component, the following applies

$\omega << \omega_0$; $\alpha << \omega_0$; $\omega_0 \approx \omega_e$

$$\left(\frac{V_S}{\hat{V}}\right)_f \approx \frac{e^{-\alpha t}}{2} \times \omega_0 \left[\frac{1}{\omega_0}\sin(\omega_0 t - \phi_0) - \frac{1}{\omega_0}\sin(\omega_0 t + \phi_0)\right.$$

$$\left.\frac{\omega}{\omega_0^2}\sin(\omega t - \phi_0) + \frac{\omega}{\omega_0^2}\sin(\omega t + \phi_0)\right] \qquad \textbf{equation 7}$$

and hence

$$\left(\frac{\hat{V}_S}{\hat{V}}\right)_f \approx e^{-\alpha t}\left(\frac{\omega}{\omega_0}\cos\phi_0 \sin\omega_0 t - \sin\phi_0 \cos\omega_0 t\right) \qquad \textbf{equation 8}$$

The critical moment occurs when the semiconductor switch has to be turned off at the maximum voltage point. The following applies: and hence

$\phi_0 = \frac{\pi}{2}$; $\cos\phi_0 = 0$; $\sin\phi_0 = 1$

$$\frac{\hat{V}_S}{\hat{V}} \approx \sin\left(\omega t + \frac{\pi}{2}\right) - e^{-\alpha t}\cos\omega_0 t = \cos\omega t - e^{-\alpha t}\cos\omega_0 t \qquad \textbf{equation 9}$$

It follows from equation 8 that in this unfavorable case $(\omega_0 >> \omega)$ the voltage applied across the switch is almost twice the line voltage $(\hat{V}_S = 2\hat{V})$.

The rate of rise of switch voltage is calculated from the following equation:

$$\frac{dv_S}{dt} = \frac{\hat{V}}{\sqrt{LC}} e^{-\frac{t}{2T}} \sin \omega_0 t \qquad \textbf{equation 10}$$

For L and C, relation 4 applies.

Initially, the switch voltage is very low. It approaches a maximum only after one alternation of the high-frequency oscillation, i.e. after

$$\tau = \frac{\pi}{\omega_0} = \pi\sqrt{LC} \qquad \textbf{equation 11}$$

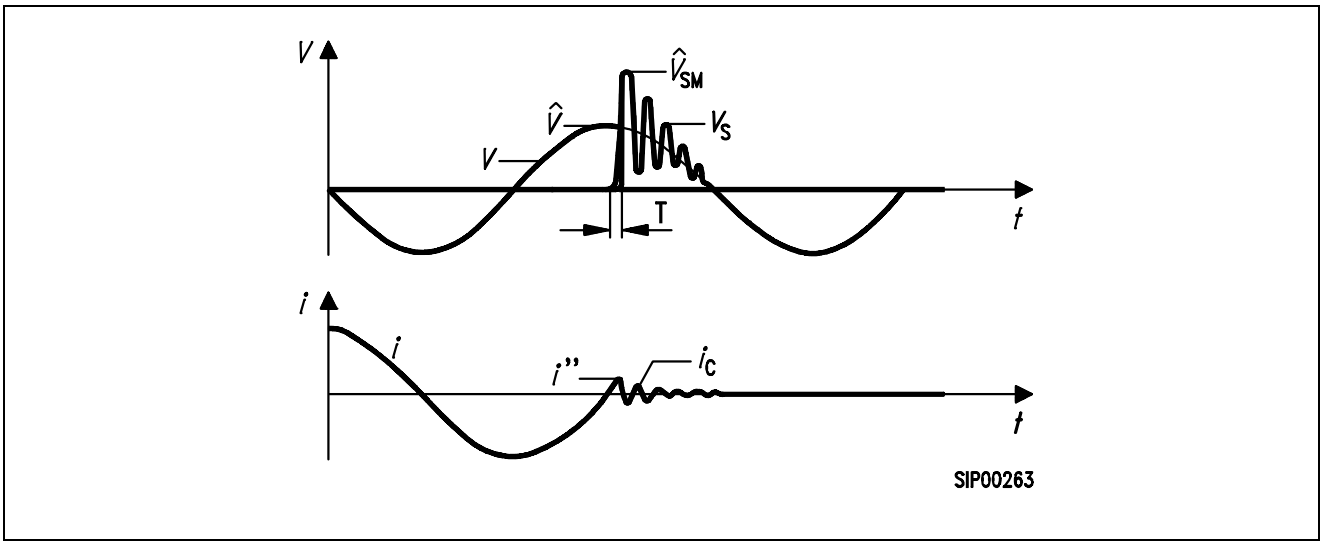

Figure 9
Switch Voltage Curve at Turn-off when Voltage is at Maximum

Maximum voltage conditions are also attained for the three-phase converter (see **Figure 10**) when an inductive load is placed across its output. **Figure 10** shows the reverse voltage curve for one semiconductor switch and the plotting method used.

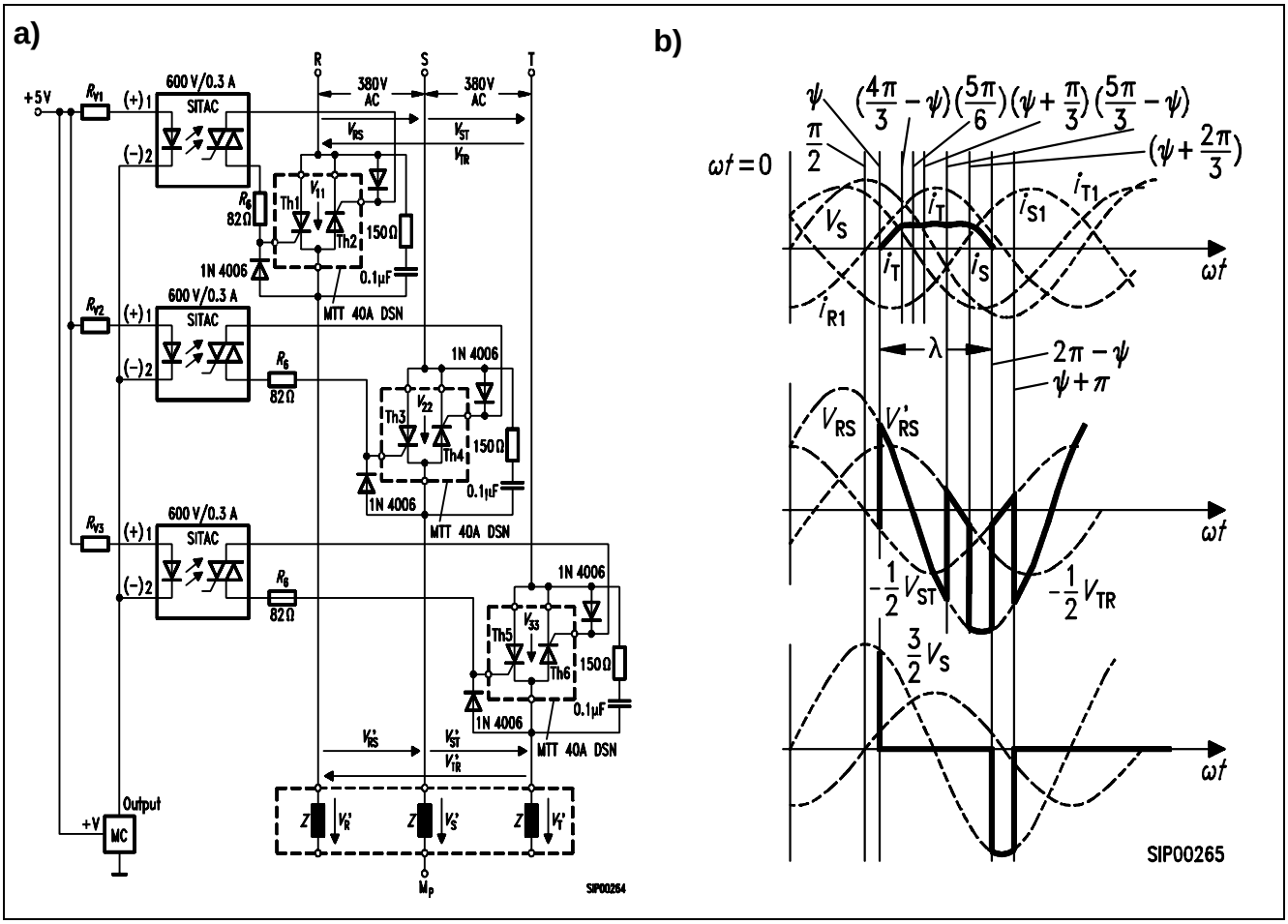

Figure 10
Three-Phase AC Converter Circuit:
a) Circuit Diagram of the Converter using SITACs as Driver Modules for Power Thyristors
b) Switch Voltage Curve

The maximum reverse voltage is defined by

$$V_S = V_{RS} + \frac{1}{2}V_{ST} \qquad \textbf{equation 12}$$

$$V_{RS} = \sqrt{3} \cdot \sqrt{2}\ \hat{V} \sin\ (\omega t + \frac{\pi}{6}) \qquad \textbf{equation 13}$$

$$V_{ST} = \sqrt{3} \cdot \sqrt{2}\ \hat{V} \sin\ (\omega t + \frac{\pi}{6} - \frac{2}{3}\pi) \qquad \textbf{equation 14}$$

From this follows that

$$V_S = \frac{3}{2}\sqrt{2}\ \hat{V} \sin\ \omega t \qquad \textbf{equation 15}$$

The crest value is

$$\hat{V}_S = \frac{3}{2}\sqrt{2}\ \hat{V} \qquad \textbf{equation 16}$$

Because of the parasitic network and component parameters, an overvoltage is produced at turn-off, as has been shown for the single-phase converter. According to equation 9, the voltage may at worst be twice as large.

$$\hat{V}_S \approx 2\frac{3}{2}\sqrt{2}\ V_{RMS} = 3\sqrt{2}V_{RMS} \qquad \textbf{equation 17}$$

For practical purpose a lower crest value is often used:

$$\hat{V}_S \approx 2.3\sqrt{2}\ V_{RMS}$$

This value is permissible since no pure inductive load is involved and shunt resistances are inserted in the circuit. In addition to the overvoltage at turn-off, the high dv/dt load is particularly critical. If the critical rate of voltage rise is exceeded, the semiconductor device may “break over”. Most of the AC switches are especially sensitive in this respect /3, 6/. To prevent breakover, there are two remedial measures:

– dv/dt limiting through RC network
– turn-on by means of zero voltage switch

Both methods have considerable disadvantages. The RC network increases the dynamic losses so that additional components are required. Turn-on by means of the zero voltage switch has the drawback in that half-wave phase control is not possible at any desired point.

The SITAC is also available without a zero voltage switch. Despite its extremely high input sensitivity ($i_{ST} \approx 1$ mA) it requires no RC network when used in very high dv/dt environments (unlike competitive devices). The SITACs dv/dt capability is tested using the circuit in **Figure 11**. In this circuit, the SITAC (S_1) is used to drive the triac (Tr 1).

The triac is operated on a 220-V line, with steep-flanked voltage spikes – generated by means of a friction plate – being superimposed on the sinusoidal line voltage. The triac itself

is protected against overvoltage and unfavorable d*v*/d*t* values but should under no circumstances be supplied with trigger current. The driver module (SITAC) must not respond to high d*v*/d*t* values. The circuit shown below is a hard-test circuit for the AC switch and driver device. By means of this circuit, interference pulses having a rate of voltage rise of up to 15 kV/µs were generated and impressed upon the line voltage without the SITAC taking action.

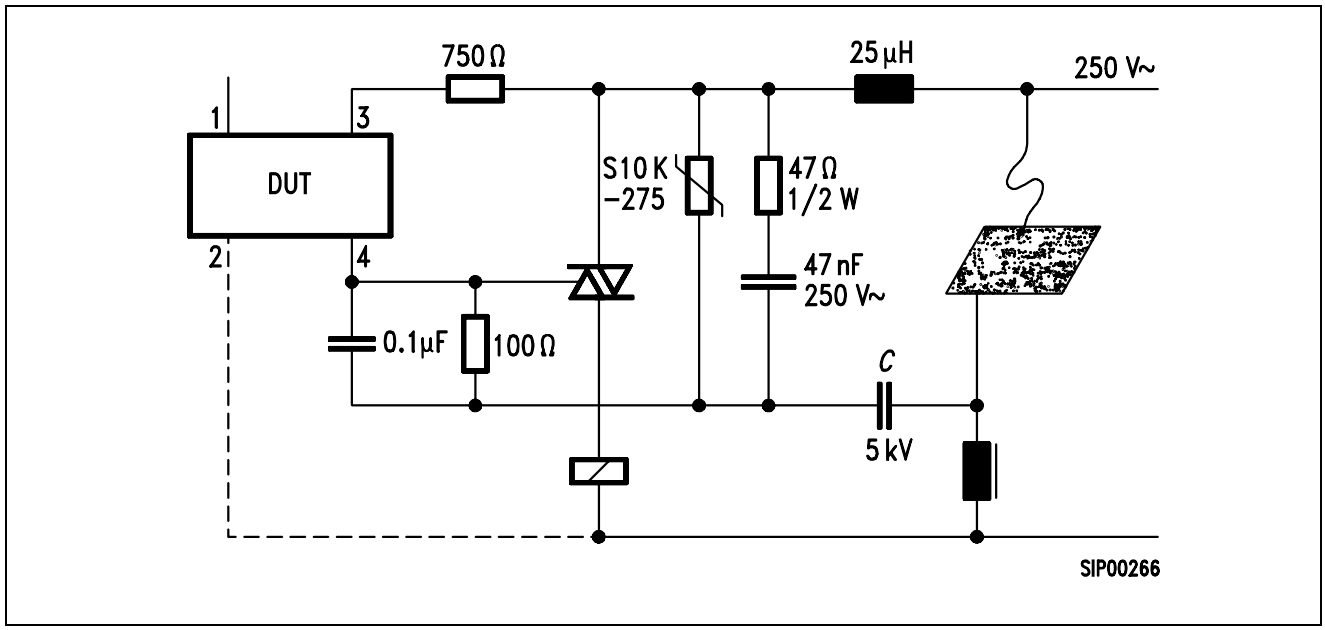

Figure 11
d*v*/d*t* Test Circuit for the SITAC (friction test) Used as a Driver Module for a Triac

The critical d*v*/d*t* for the SITAC: $dv/dt_{CR} \geq 10$ kV/µs. When this requirement is met any desired phase control angle can be achieved by the SITAC without the need for an RC network.

The maximum available reverse voltage V_S of current SITACs is 600 V. As is evident from mathematical equations 1 to 16, reverse voltages of more than 600 V are already found in 380-V circuits. For these applications, the voltage range can be increased by connecting SITACs in series.

Series Connection of SITACs

Steady-State Operation

The voltage distribution under steady-rate conditions does not pose any problems if balancing resistors are used (about 3 MΩ). These resistors may also be omitted if SITACs with a reverse current of $I_{BO} \geq 1$ mA are employed. As shown in **Figure 12a**, however, the SITACs have a very low reverse current. The reverse current is in the order of only a few microamps even at an operating temperature of 80 °C under unfavorable conditions (lower limit of reverse current spread) so that the condition $I_{VO} \geq 1$ mA can be met without difficulty.

Figure 12b shows the voltage distribution between two SITACs without RC network in the event of the voltage distribution in the negative half-wave being uneven due to SITACs with different reverse characteristics (see **Figure 12c**). Because the SITACs will not trigger until $I_{BO} \geq$ mA, the SITAC with the lower reverse voltage, although operating in the avalanche region, is not driven into conduction.

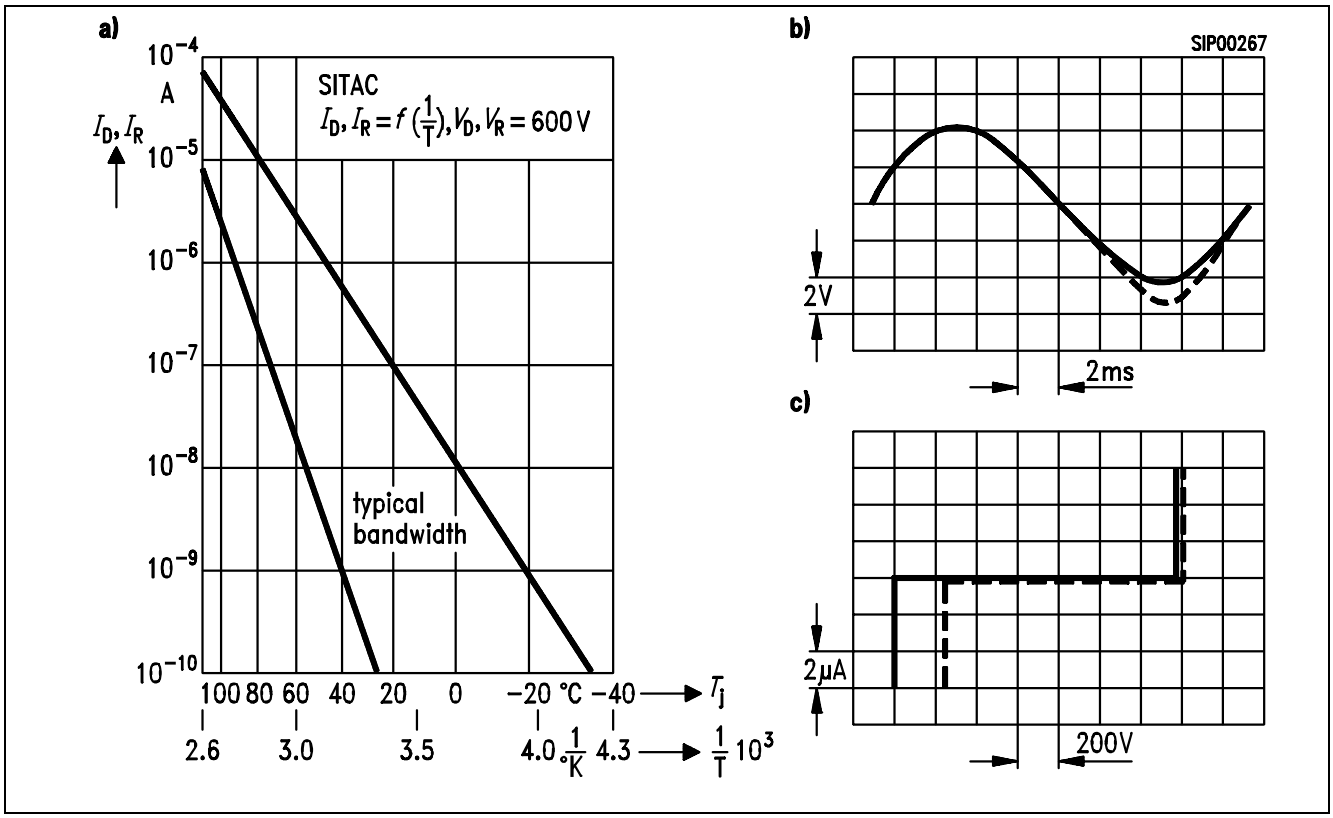

Figure 12
Static Voltage Distribution for SITACs Connected in Series
a) Reverse Current of the SITAC as a Function of Temperature and Reverse Current Spread
b) Static Voltage Distribution for n SITACs connected in Series, with uneven Voltage
c) Distribution in the Negative half-cycle
d) Reverse Voltage Characteristics of the two Series-connected SITACs; Different Reverse Voltage Profiles

Dynamic Operation

Due to the different delay times t_{GD} of the SITACs, problems may arise in the dynamic phases (turn-on) with respect to voltage load (overvoltage) and pulse current (pulse current amplitude and di/dt too high). For this reason, the maximum load ratings for series connections without corrective measures must be reduced as compared with those for independent operation. The following 3 circuit versions are possible for series operation.

Circuit Version I

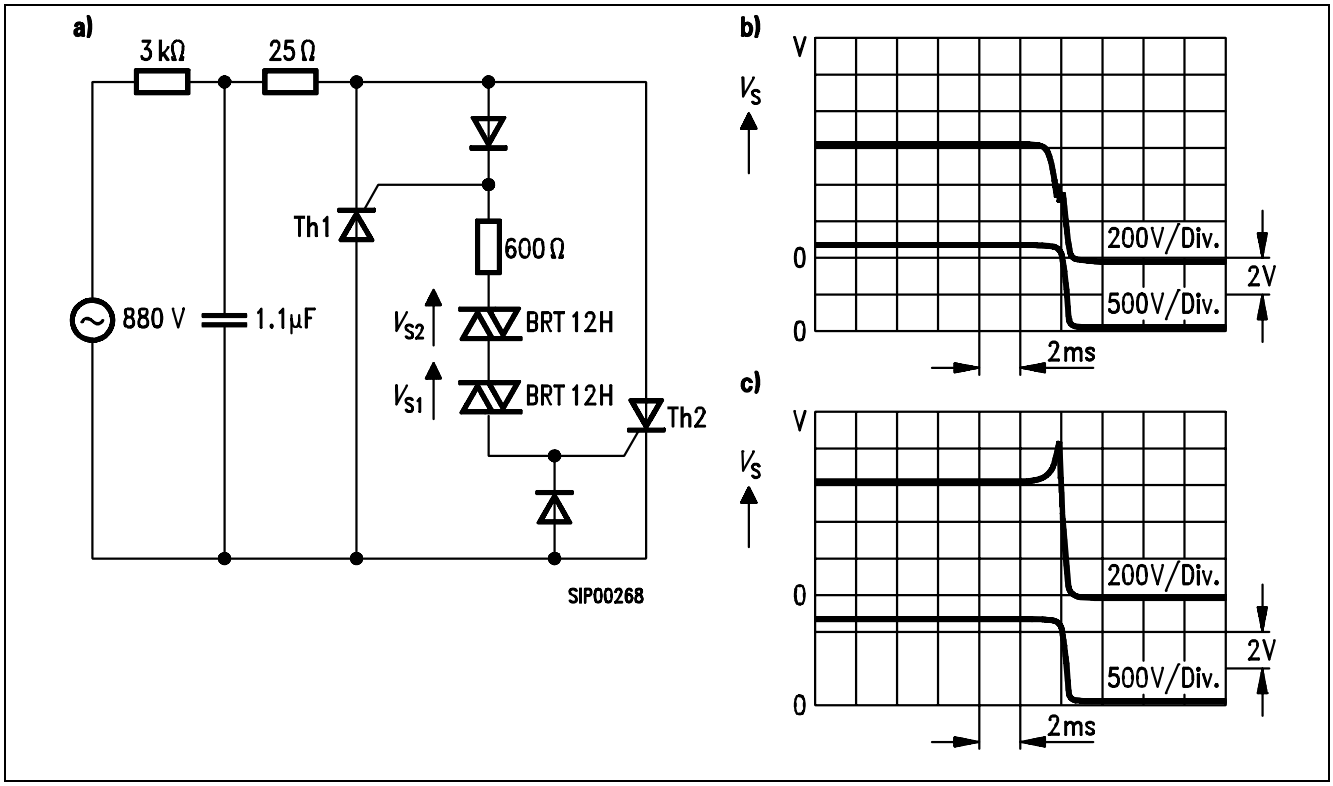

Figure 13
Series Connection of SITACs Used as a Driver Module for Power Thyristors (version I)
a) Circuit Diagram
b) Oscillograms showing Switching Performance

Connecting the SITACs in series without providing protection measures (**Figure 13a**) causes the slower device to break over as shown in **Figure 13b**. The SITAC with the shorter delay time is the first device to trigger so that the full voltage is applied to the second SITAC. This leads to breakover of the second SITAC which means that the maximum ratings reduced for this type of switching operation with respect to trigger pulse current and rate of current rise must not be exceeded. To ensure safe and non-destructive operation in the circuit as per **Figure 13a**, the following values must not be exceeded: I_P = 2 A (pulse current), t_P = 10 µs (pulse duration), di/dt = 5 A/µs (rate of current rise).

Circuit Version II

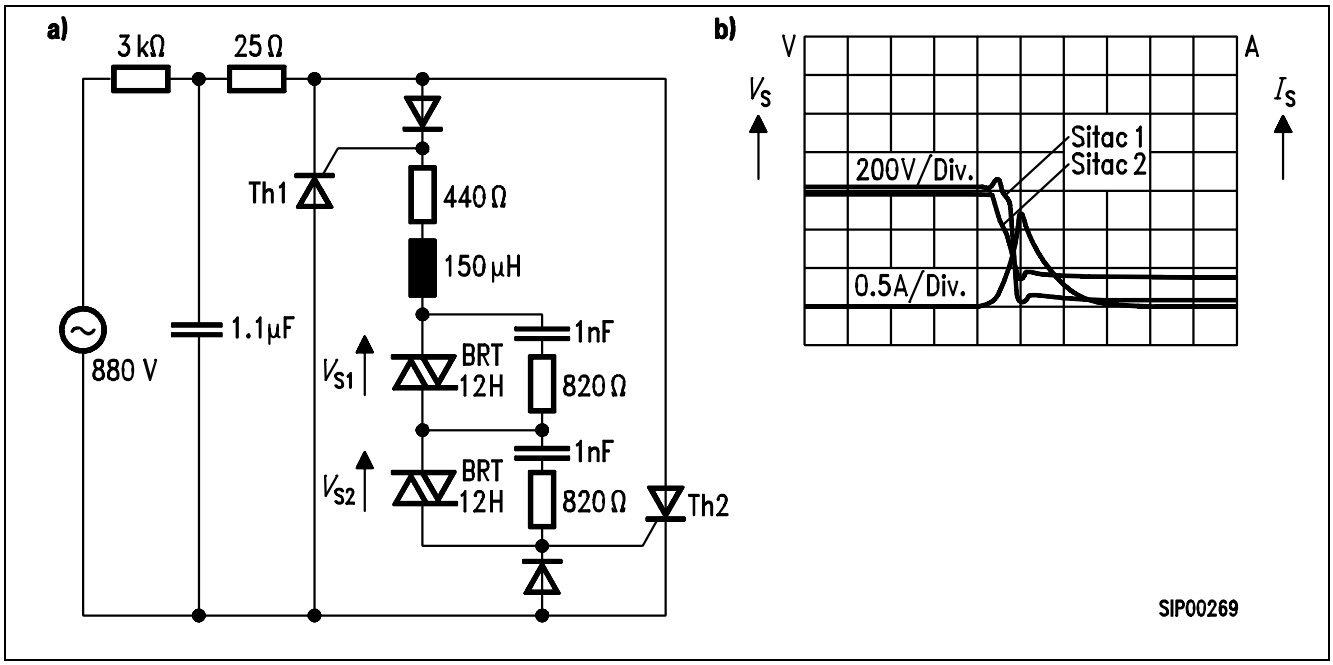

Figure 14
Series Connection of SITACs Used as a Driver Module for Thyristors (version II)
a) Circuit Diagram
b) Oscillograms showing Switching Performance

In this type of circuit, a leakage inductance is connected in series, and RC networks in parallel with the SITACs. Here, too, the processes taking place during the dynamic phase may lead to a rise in voltage at the SITACs but not to breakover as shown in **Figure 14b**. The specified maximum ratings are slightly higher:

I_P= 3 A, t_P = 10 µs, di/dt = 5 A/µs.

Circuit Version III

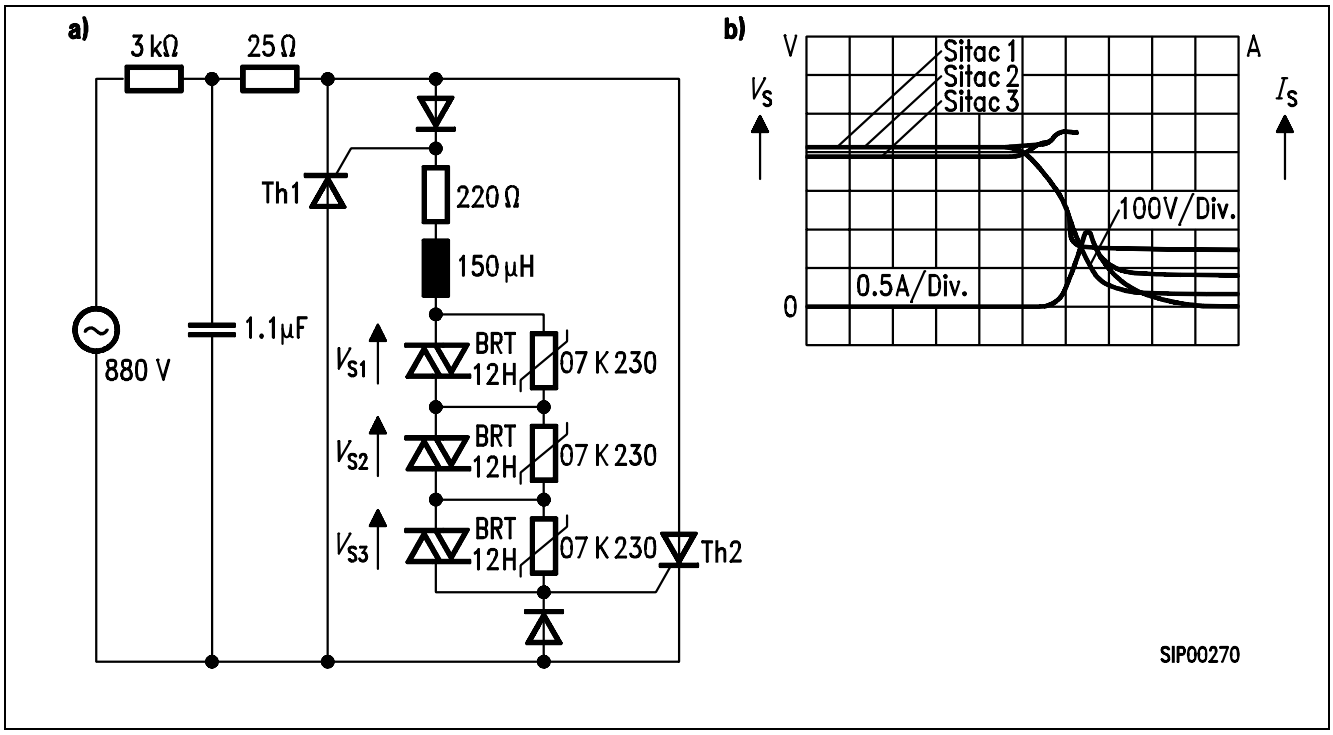

Figure 15
Series Connection of SITACs Used as a Driver Module for Thyristors (version III)
a) Circuit Diagram
b) Oscillograms showing Switching Performance

This circuit is characterized by 3 SITACs with a leakage inductance connected in series, and varistors in parallel. **Figure 15b** shows that no excessive voltages are produced in the switching phase so that the same maximum ratings apply as in the case of individual SITAC operation, i.e.

I_P = 5 A, t_P = 10 µs, di/dt = 10 A/µs.

This circuit is totally uncritical, and can be extended by connecting any number of SITACs in series, however the rated insulation voltage between the SITACs input and output has to be considered.

Parallel Connection of SITACs

This type of connection is often used to increase the switchable current. It presents no problems since the forward resistance and the trigger current have a positive temperature coefficient. The forward resistance increases as the temperature rises, which has a self-balancing effect. The trigger current, too, rises with temperature, thus ensuring stabilization during the dynamic phases. This makes it possible, among other things, to select phase control angles that automatically adjust, and thus maintain, themselves in accordance with the temperature.

Summary

The SITAC is an AC semiconductor switch in SIPMOS technology. It has a high input sensitivity (direct IC drive with 1 mA plus drive current), a high trigger pulse current of I_{TP} = 5 A at a rate of current rise of di/dt = 10 A/µs, and a unique rate of voltage rise of 10 kV/µs. These data enable the SITAC to be used as an isolated AC semiconductor switch in power circuits of up to 66 W or in phase control circuits, without requiring an RC network. Thanks to its high trigger pulse current it is ideal for use as a drive module in power thyristor circuits. The dielectric strength of the SITAC required for high blocking capability thyristors can be readily achieved by selective series connection.