LH64256C

1M (256 × 4 bit) Dynamic RAM

FEATURES

- 262,144 words × 4 bit organization
- Standard 7.62 mm 20/26-pin SOJ (SOJ20-P-300) plastic package
- Access time: 60 ns (MAX.)
- Cycle time: 120 ns (MIN.)
- Fast page mode cycle time: 40 ns (MIN.)
- Power supply: +5.0 V ± 10%
- Power consumption (MAX.):
  495 mW (Operating: t_{RC} = 120 ns)
  11 mW (Standby: TTL input level)
  5.5 mW (Standby: CMOS input level)
- Built-in latch circuit for Row-address, Column-address, and Input data
- $\overline{OE}$ = Don't care in early write operation
- $\overline{RAS}$ only refresh, hidden refresh, and $\overline{CAS}$ before $\overline{RAS}$ refresh capability
- On-chip refresh counter
- 512 refresh cycle/8 ms
- Not designed or rated as radiation hardened
- P-type bulk silicon CMOS process
- Operating temperature range: 0 to +70°C

DESCRIPTION

SHARP's LH64256C is a 262,144 words × 4 bit Dynamic Random Memory which allows fast page mode access. The LH64256C is fabricated on SHARP's advanced CMOS double-level polysilicon gate technology. With its input multiplexed and packaged in the standard 20/26-pin SOJ, it is easy to realize the memory systems with low power dissipation and large memory capacity. The LH64256C operates on a single +5.0 V power supply and the built-in biasing voltage generator circuit.

PIN CONNECTIONS

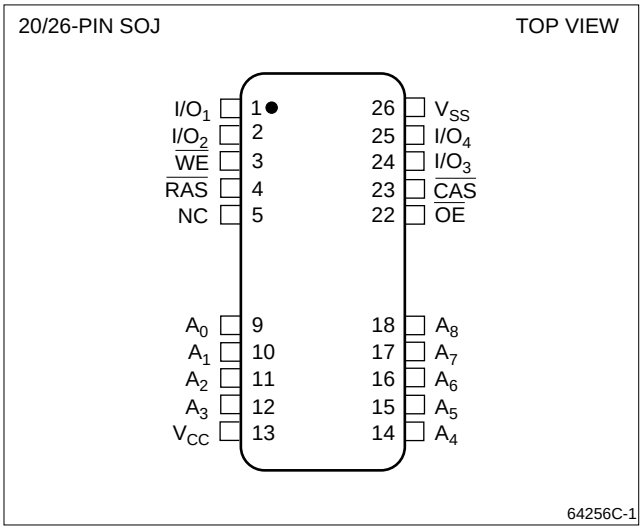


Figure 1. Pin Connections

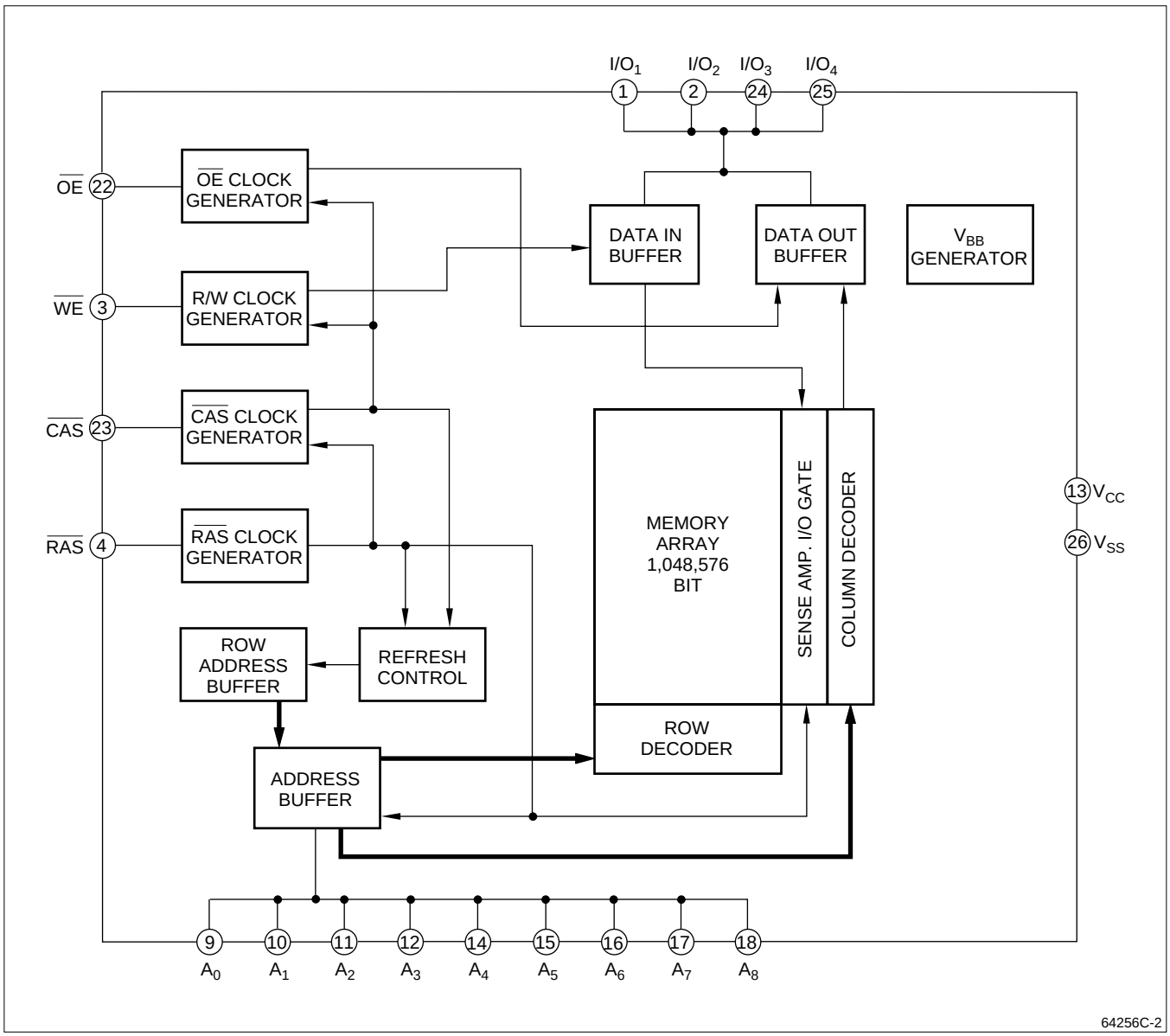


Figure 2. LH64256C Block Diagram

PIN DESCRIPTION

PIN NAME	FUNCTION
$A_0 - A_8$	Address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable

PIN NAME	FUNCTION
$I/0_1 - I/0_4$	Data input/output
V_{CC}	Power supply (+5.0 V)
V_{SS}	Power supply (0 V)
NC	No connection

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	NOTE
Applied voltage on all pins	–1.0 to +7.0	V	1
Operating temperature	0 to +70	°C	—
Storage temperature	–65 to +150	°C	—
Output short circuit current	50	mA	—
Power dissipation	600	mW	2

NOTES:
1. With respect to V_{SS}.
2. T_A = 25°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.3 V	V
	V_{IL}	–0.3	—	0.8	V

PIN CAPACITANCE (T_A = 0 to +70°C, f = 1 MHz, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 – A_8	C_{IN1}	—	7	pF
	$\overline{RAS}$, $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	7	pF
Input/Output capacitance	$I/0_1$ – $I/0_4$	C_{OUT1}	—	8	pF

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS		SYMBOL	MIN.	MAX.	UNIT	NOTES
Average supply current in normal operation	t_{RC} = MIN.		I_{CC1}	—	90	mA	1, 2
Average supply current in standby mode	TTL	RAS = CAS = V_{IH}	ICC2	—	2.0	mA	1
	CMOS	RAS = CAS ≥ V_{CC} – 0.2 V		—	1.0	mA	
Average supply current in fast page mode	t_{PC} = MIN.		I_{CC4}	—	80	mA	1, 2
Average supply current in CAS before RAS refresh cycle			I_{CC6}	—	90	mA	1, 2
Average supply current in RAS only refresh cycle			I_{CC3}	—	90	mA	1, 2
Input leakage current	0 V ≤ V_{IN} ≤ 6.5 V 0 V except on test pins		I_{LI}	–10	10	µA	—
Output leakage current	0 V ≤ V_{OUT} ≤ 0.3 V Output = Disable		I_{LO}	–10	10	µA	3
Output 'High' Voltage	I_{OH} = -5 mA		V_{OH}	2.4	—	V	—
Output 'Low' Voltage	I_{OL} = +4.2 mA		V_{OL}	—	0.4	V	—

NOTES:

1. The output pins are in high impedance state.
2. I_{CC1}, I_{CC4}, I_{CC6}, and I_{CC3} depend on cycle time.
3. The output pins are disabled by $\overline{RAS}$ = $\overline{CAS}$ = V_{IH} or $\overline{CAS}$ = V_{IH}.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] (T_A = 0 to 70°C, V_{CC} = 5 V ± 10%)

Read cycle

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Random read/write cycle time	t_{RC}	120	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	60	ns	9
Access time from column address	t_{AA}	—	35	ns	9
Access time from $\overline{CAS}$	t_{CAC}	—	20	ns	9
Access time from $\overline{OE}$	t_{OEA}	—	20	ns	9
Row address set-up time	t_{ASR}	0	—	ns	—
Row address hold time	t_{RAH}	10	—	ns	—
Column address set-up time	t_{ASC}	0	—	ns	—
Column address hold time ($\overline{RAS}$)	t_{CAH}	15	—	ns	—
Column address delay time ($\overline{RAS}$)	t_{RAD}	15	25	ns	5
Column address lead time ($\overline{RAS}$)	t_{RAL}	30	—	ns	—
RAS pulse width	t_{RAS}	60	10,000	ns	—
$\overline{RAS}$ precharge time	t_{RP}	50	—	ns	—
$\overline{CAS}$ precharge time ($\overline{RAS}$ ↓)	t_{CRP}	10	—	ns	—
$\overline{CAS}$ delay time ($\overline{RAS}$)	t_{RCD}	20	40	ns	6
$\overline{CAS}$ lead time ($\overline{RAS}$)	t_{RSL}	20	—	ns	—
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	ns	—
$\overline{CAS}$ hold time	t_{CSH}	60	—	ns	—
$\overline{OE}$ lead time ($\overline{RAS}$)	t_{ROL}	0	—	ns	—
Output data disable time ($\overline{CAS}$)	t_{OFF}	—	20	ns	—
Output data disable time ($\overline{OE}$)	t_{OEZ}	—	20	ns	—
Output data hold time ($\overline{CAS}$)	t_{SOH}	0	—	ns	—
Output data hold time ($\overline{OE}$)	t_{OOH}	0	—	ns	—
Read command set-up time ($\overline{CAS}$)	t_{RCS}	0	—	ns	—
Read command hold time ($\overline{CAS}$)	t_{RCH}	0	—	ns	8
Read command hold time ($\overline{RAS}$ ↑)	t_{RRH}	10	—	ns	8
Transition time (rise and fall)	t_T	3	50	ns	—
Refresh time interval	t_{REF}	—	8	ms	—

FAST PAGE MODE CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Fast page mode cycle time	t_{PC}	40	—	ns	—
$\overline{CAS}$ precharge time	t_{CP}	10	—	ns	—
$\overline{CAS}$ precharge access time	t_{CACP}	—	35	ns	—
Read-write cycle time (page mode)	t_{PRWC}	95	—	ns	7

WRITE CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
(Early Write)					
Write command setup time ($\overline{CAS}$)	t_{WCS}	0	—	ns	7
Write command hold time ($\overline{CAS}$)	t_{WCH}	15	—	ns	—
Data input set-up time	t_{DS}	0	—	ns	—
Data input hold time	t_{DH}	15	—	ns	—
($\overline{OE}$ Controlled)					
$\overline{CAS}$ set-up time	t_{CWS}	0	—	—	7
Write command lead time ($\overline{RAS}$)	t_{RWL}	20	—	ns	—
Write command lead time ($\overline{CAS}$)	t_{CWL}	20	—	ns	—
Write pulse width ($\overline{WE}$)	t_{WP}	10	—	ns	—
$\overline{OE}$ hold time ($\overline{WE}$)	t_{OED}	20	—	ns	—

READ-WRITE CYCLE/READ-MODIFY-WRITE CYCLE

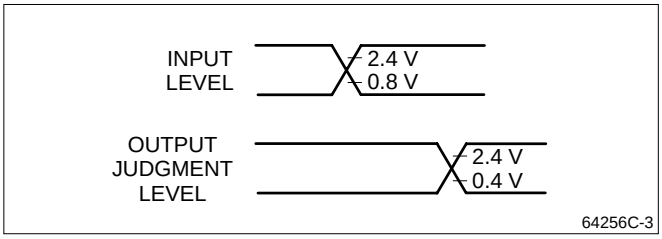
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Read-write cycle time	t_{RWC}	170	—	ns	7
$\overline{WE}$ delay time ($\overline{RAS}$)	t_{RWD}	85	—	ns	7
Column address delay time ($\overline{WE}$)	t_{AWD}	55	—	ns	7
$\overline{WE}$ delay time ($\overline{CAS}$)	t_{CWD}	45	—	ns	7
$\overline{OE}$ hold time	t_{OED}	20	—	ns	—

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE/HIDDEN REFRESH CYCLE

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
$\overline{CAS}$ setup time ($\overline{RAS}$)	t_{CSR}	10	—	ns	—
$\overline{CAS}$ hold time ($\overline{RAS}$)	t_{CHR}	15	—	ns	—
$\overline{RAS}$ to $\overline{CAS}$ precharge time ($\overline{RAS}$ ↑)	t_{RPCP}	10	—	ns	—
$\overline{WE}$ precharge time ($\overline{RAS}$)	t_{WRP}	0	—	ns	—

NOTES:

1. For properly functioning the memory, it is necessary to pause at least 200 µs after power-on and followed by several dummy cycles. When $\overline{RAS} = V_{IH}$ is continued for more than 8 ms, the above dummy cycles should be given. Usually eight (8) ordinary refresh cycles should be given.
2. The current consumption (I_{CC}) during power on is dependent on the input level or $\overline{RAS}$. If $\overline{RAS}$ is V_{IL} during power on, the device goes into an active cycle automatically, and I_{CC} exhibits large current transients. It is recommended that $\overline{RAS}$ tracks with V_{CC} or be held at a valid V_{IH} during power on.
3. AC characteristics assume $t_T = 5$ ns.
4. AC characteristics assume the following condition.



5. t_{RAD} (MAX.) is the maximum point for t_{RAD} where t_{RAC} (MAX.) is ensured, and does not represent a limit of operation. If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time comes under the control of t_{AA}.
6. t_{RCD} (MAX.) is the maximum point for t_{RCD} where t_{RAC} (MAX.) is ensured, and does not represent a limit of operation. If $t_{RCD} \geq t_{RCD}$ (MAX.), the access time is controlled by t_{CAC}.
7. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CWD} are the restrictive operating parameters and do not represent a limit of operation. If $t_{WCS} \geq t_{WCS}$ (MIN.), the cycle is an early write cycle and the data out buffers will remain inactive until $\overline{CAS}$ rises up again. If $t_{CWD} \geq t_{CWD}$ (MIN.), $t_{RWD} \geq t_{RWD}$ (MIN.), and $t_{AWD} \geq t_{AWD}$ (MIN.) the cycle is a read modify write cycle and the data output will be the information of the selected cell. Except for the above timing, the output data will be indefinite.
8. The operation is ensured when either t_{RRH} or t_{RCH} is satisfied.
9. Measured with a load equivalent to: 2 TTL (-1 mA, +4 mA) + C load (100 pF) (Including the scope and the jig).

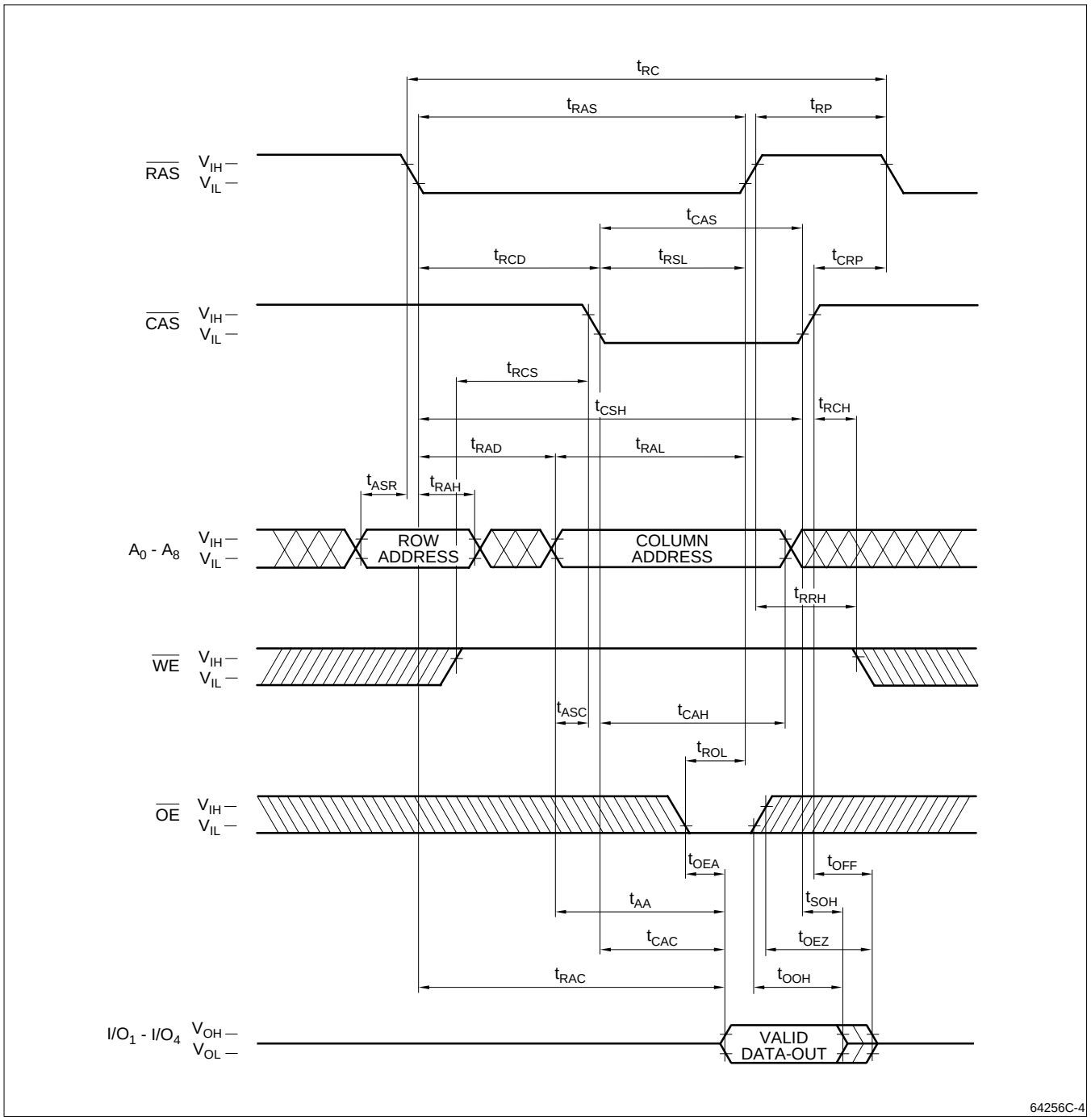


Figure 3. Timing Chart

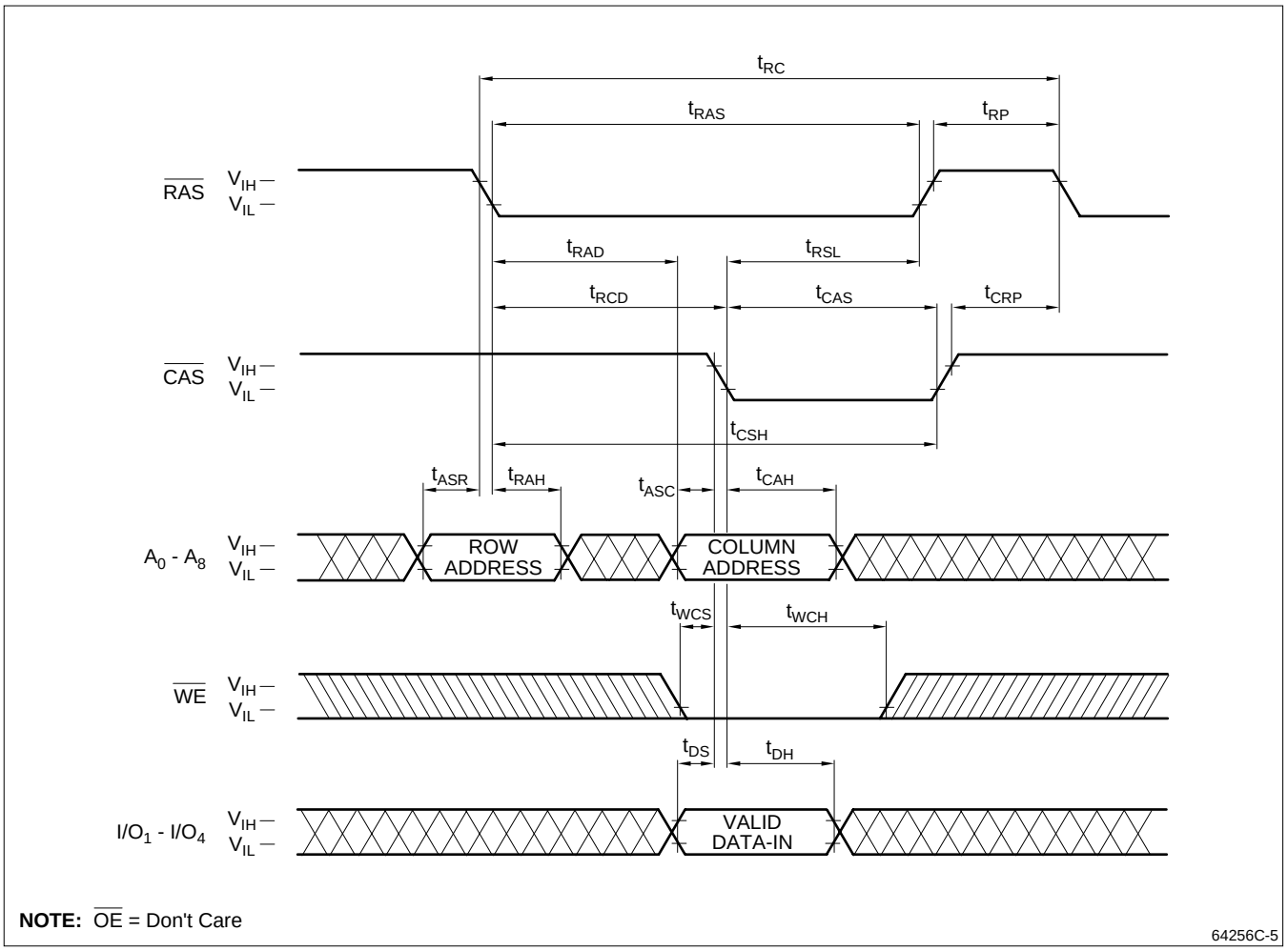


Figure 4. Write Cycle (Early Write)

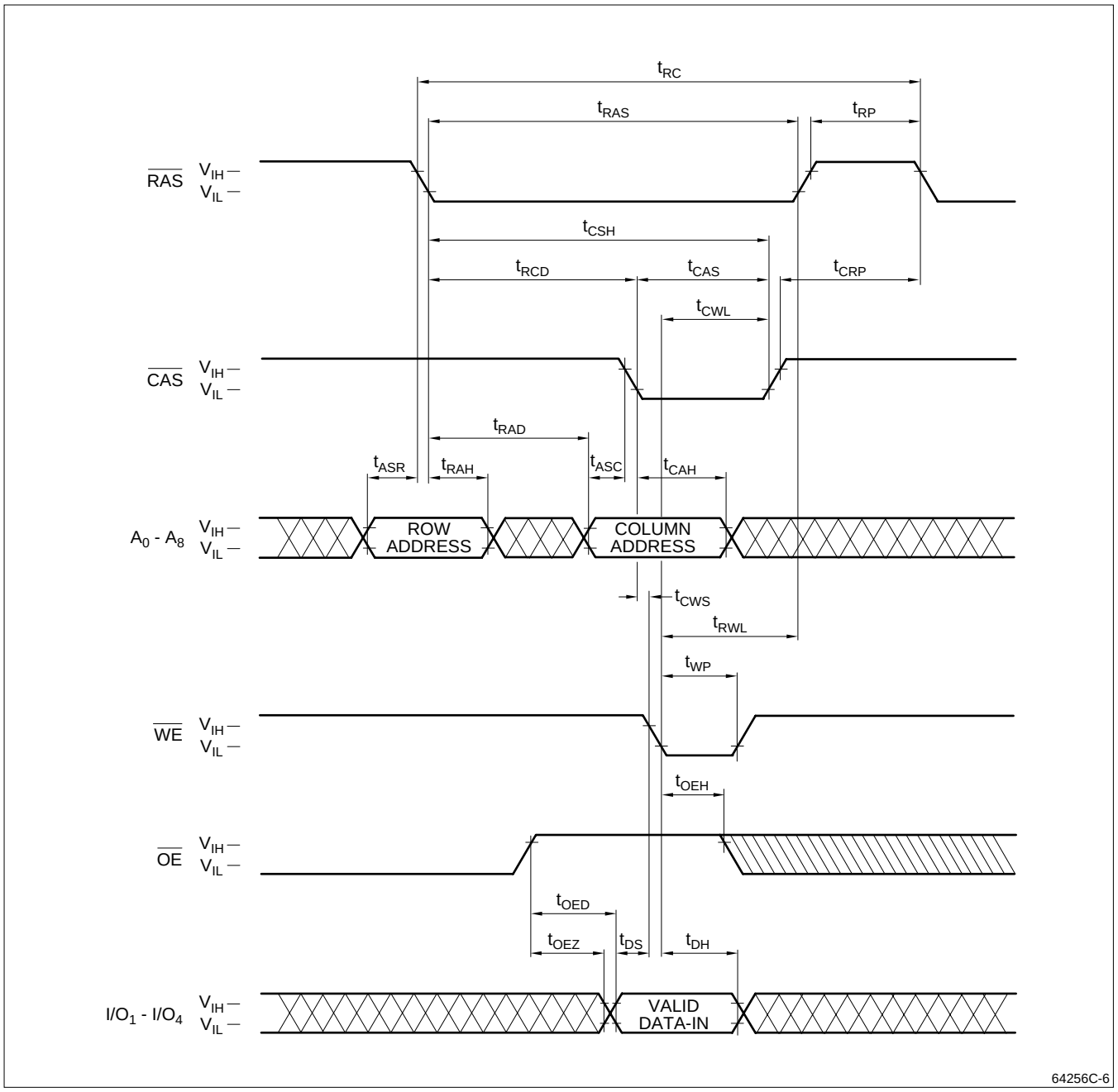


Figure 5. Write Cycle (OE Controlled Write)

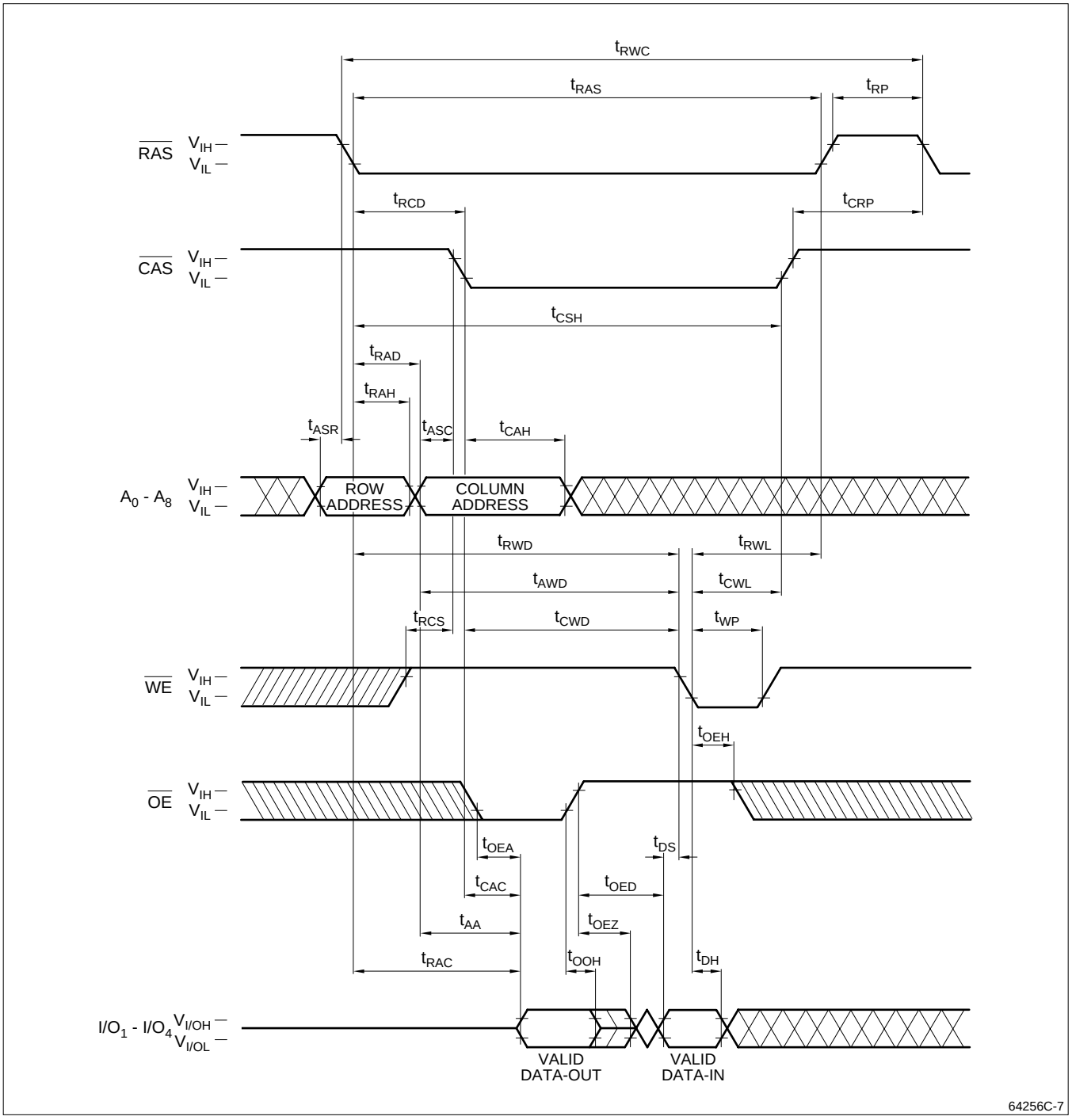


Figure 6. Read-Write Cycle

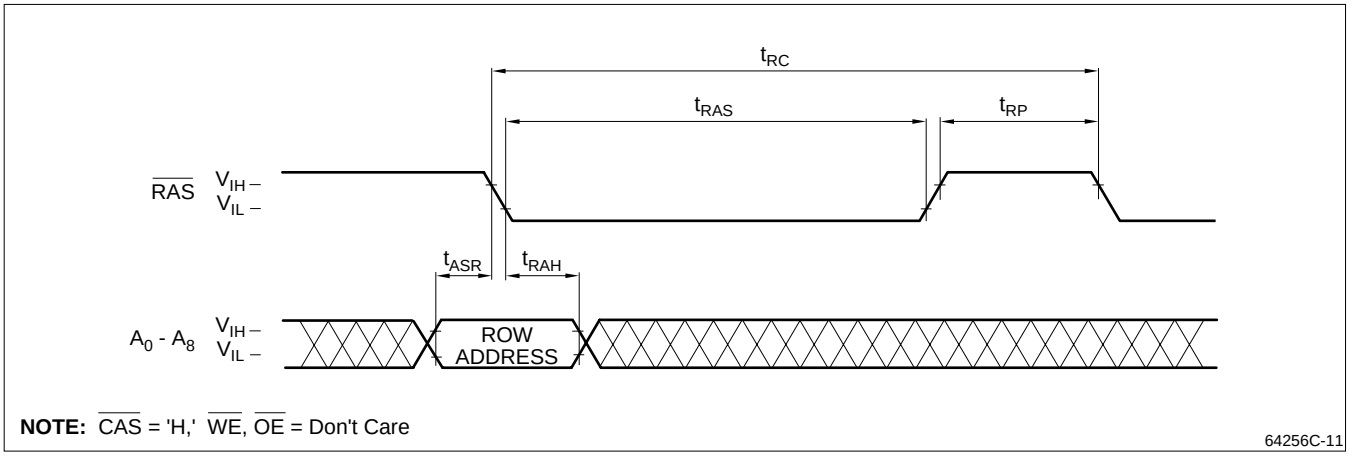


Figure 7. $\overline{RAS}$ Only Refresh Cycle

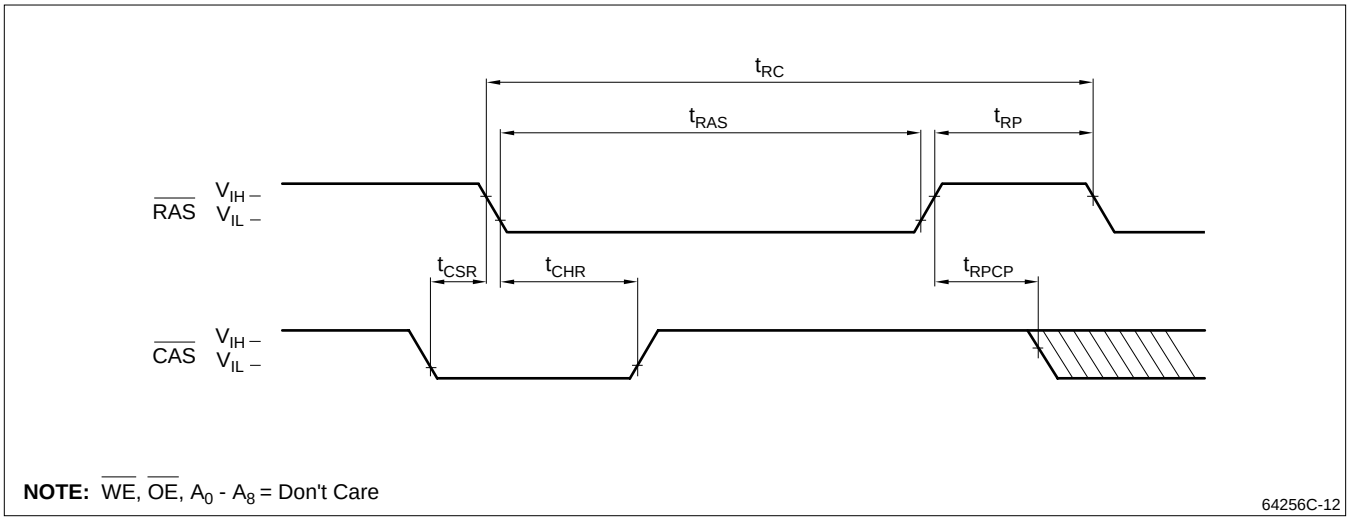


Figure 8. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

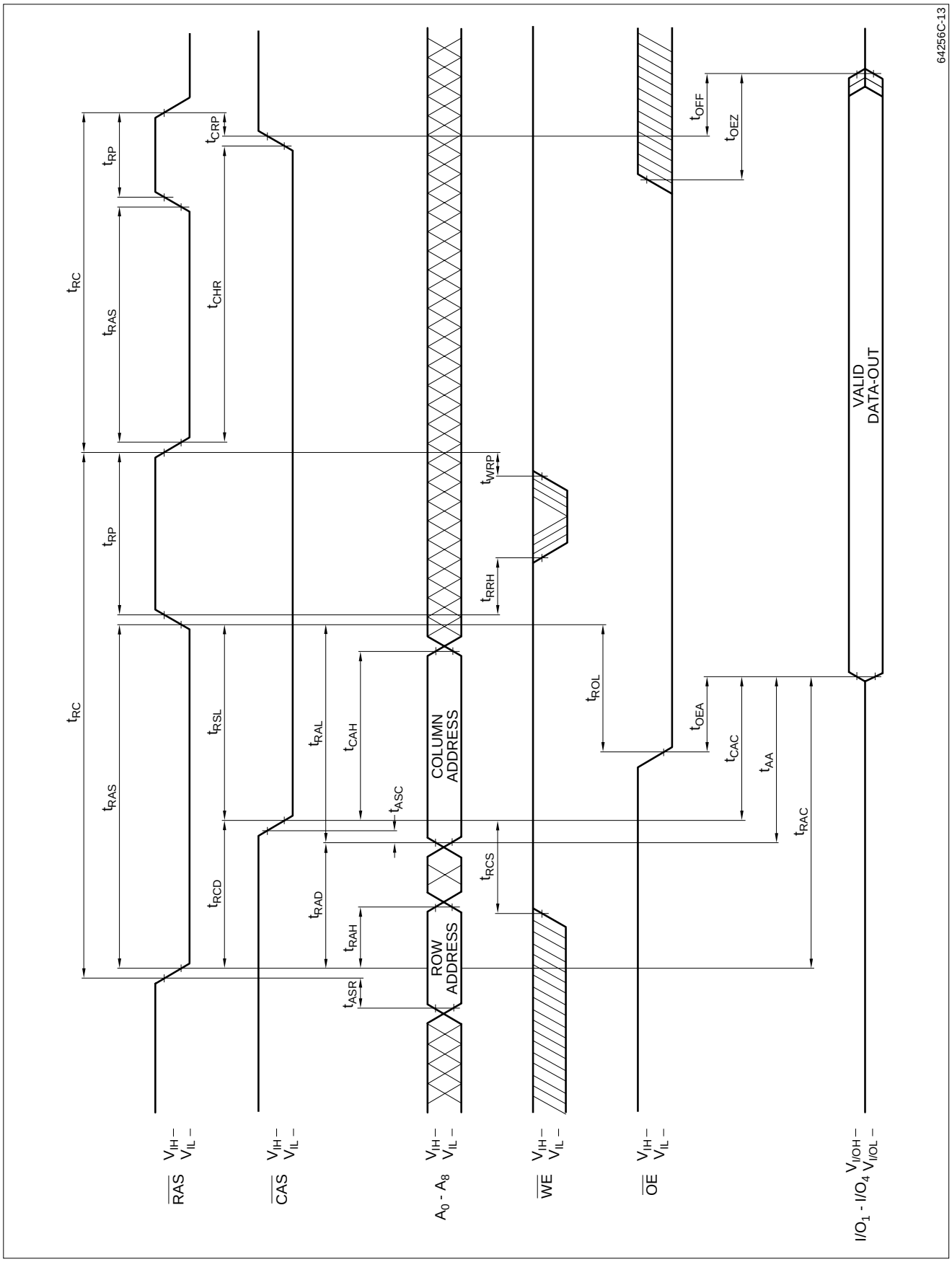


Figure 9. Hidden Refresh Cycle

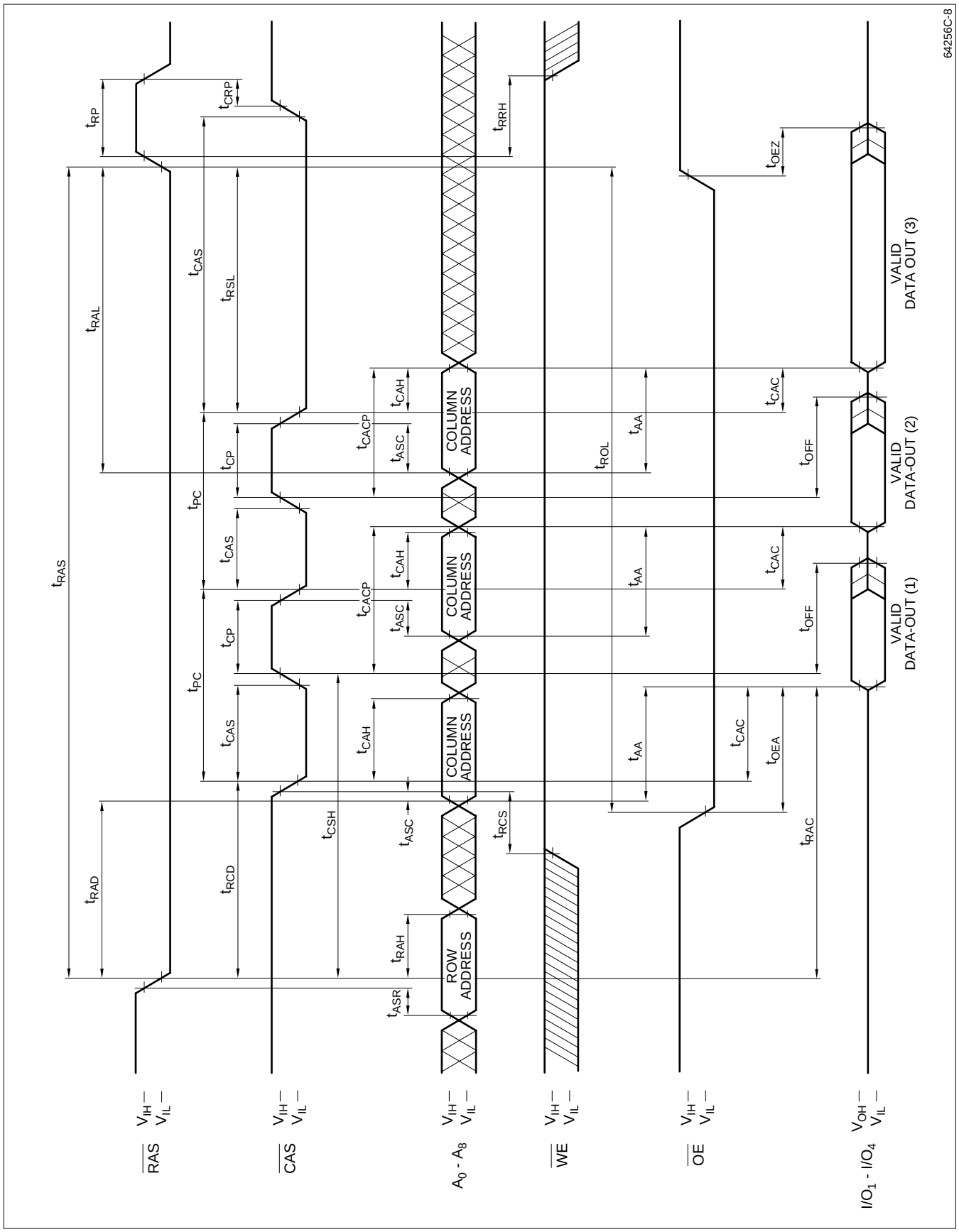


Figure 10. Fast Page Mode Read Cycle

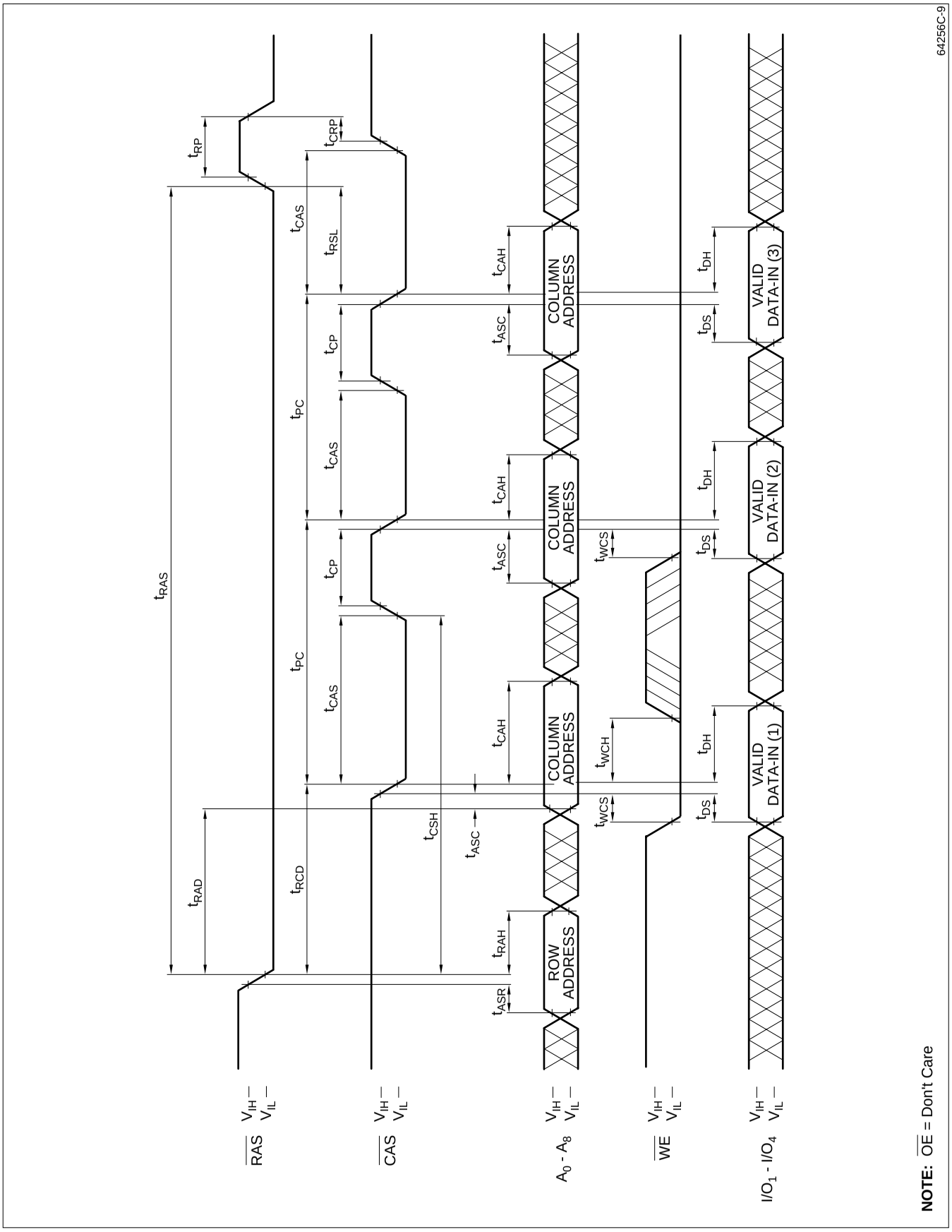


Figure 11. Fast Page Mode Write Cycle

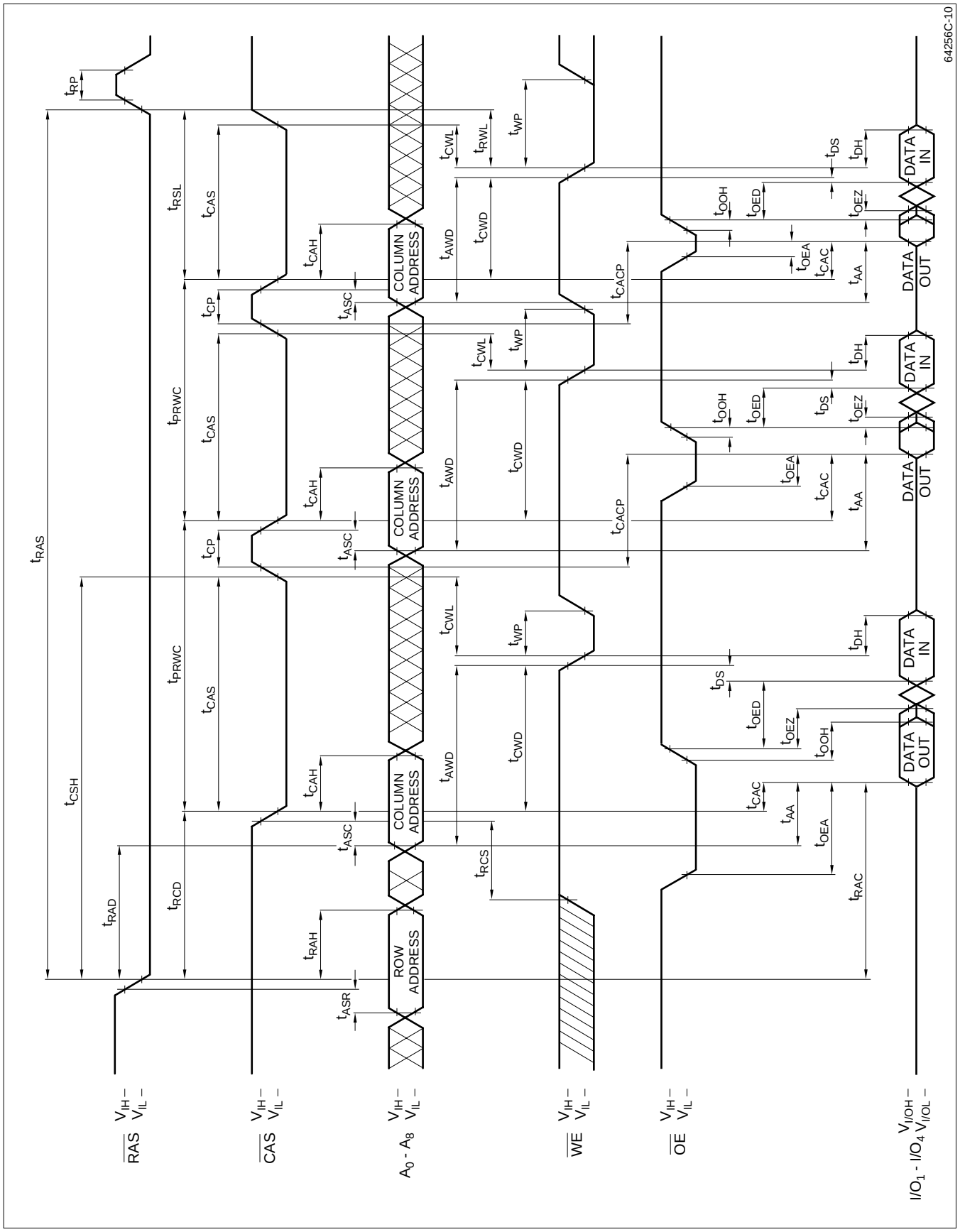
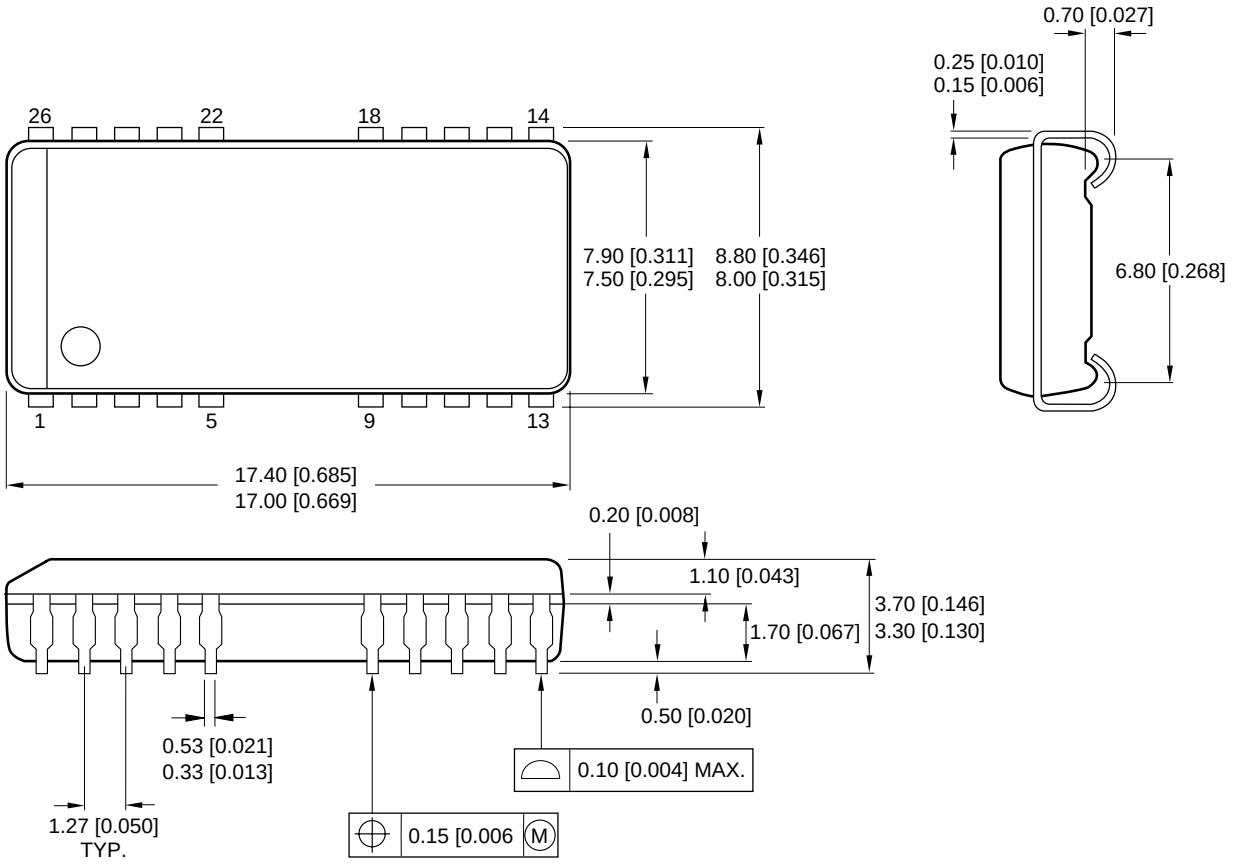


Figure 12. Fast Page Mode Read-Write Cycle

PACKAGE DIAGRAMS

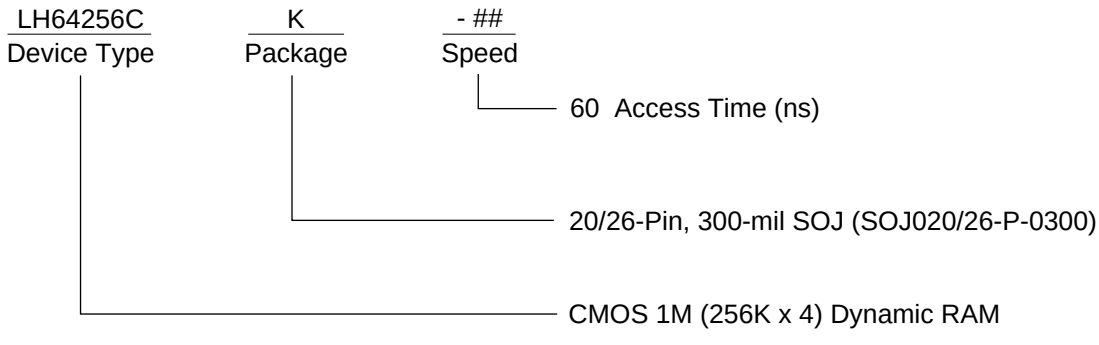
26SOJ (SOJ026-P-0300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

26SOJ-3

ORDERING INFORMATION



Example: LH64256C-60 (CMOS 1M (256K x 4) Dynamic RAM, 60 ns, 20-Pin, 300-mil SOJ)

64256C-14