LH543601

256 × 36 × 2 Bidirectional FIFO

FEATURES

- Fast Cycle Times: 20/25/30/35 ns
- Pin-Compatible and Functionally-Compatible 0.7µ-Technology Replacement for Sharp LH5420
- Two 256 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B
- Independently-Synchronized ('Fully-Asynchronous') Operation of Port A and Port B
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/$\overline{W}$, Enable, Request, and Address Control Inputs are Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into a Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- Five Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full Flag and Almost-Empty Flag are Programmable
- Mailbox Registers with Synchronized Flags
- Data-Bypass Function
- Data-Retransmit Function
- Automatic Byte Parity Checking
- 8 mA-I_{OL} High-Drive Three-State Outputs with Built-In Series Resistor
- TTL/CMOS-Compatible I/O
- Space-Saving PQFP and TQFP Packages
- PQFP to PGA Package Conversion [1]

FUNCTIONAL DESCRIPTION

The LH543601 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 256 by 36 bits. The LH543601 is ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH543601 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the LH543601 is a fully-static part.

Conceptually, the port clocks CK_A and CK_B are free-running, periodic 'clock' waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these 'clock' waveforms *must* be periodic. An 'asynchronous' mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and enough aperiodic 'clock' pulses of suitable duration are generated by external logic to cause all necessary actions to occur.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/ acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 or fewer words may be retransmitted any desired number of times.

NOTE:

1. For PQFP-to-PGA conversion for thru-hole board designs, Sharp recommends ITT Pomona Electronics' SMT/PGA Generic Converter model #5853.® This converter maps the LH543601 132-pin PQFP to a generic 13 × 13, 132-pin PGA (100-mil pitch). For more information, contact Sharp or ITT Pomona Electronics at 1500 East Ninth Street, Pomona, CA 91766, (909) 469-2900.

FUNCTIONAL DESCRIPTION (cont'd)

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A Byte Parity Check Flag at each port monitors data integrity. Control-Register bit 0 (zero) selects the parity mode, odd or even. This bit is initialized for odd data parity at reset; but it may be reprogrammed for even parity, or back again to odd parity, as desired.

PIN CONNECTIONS

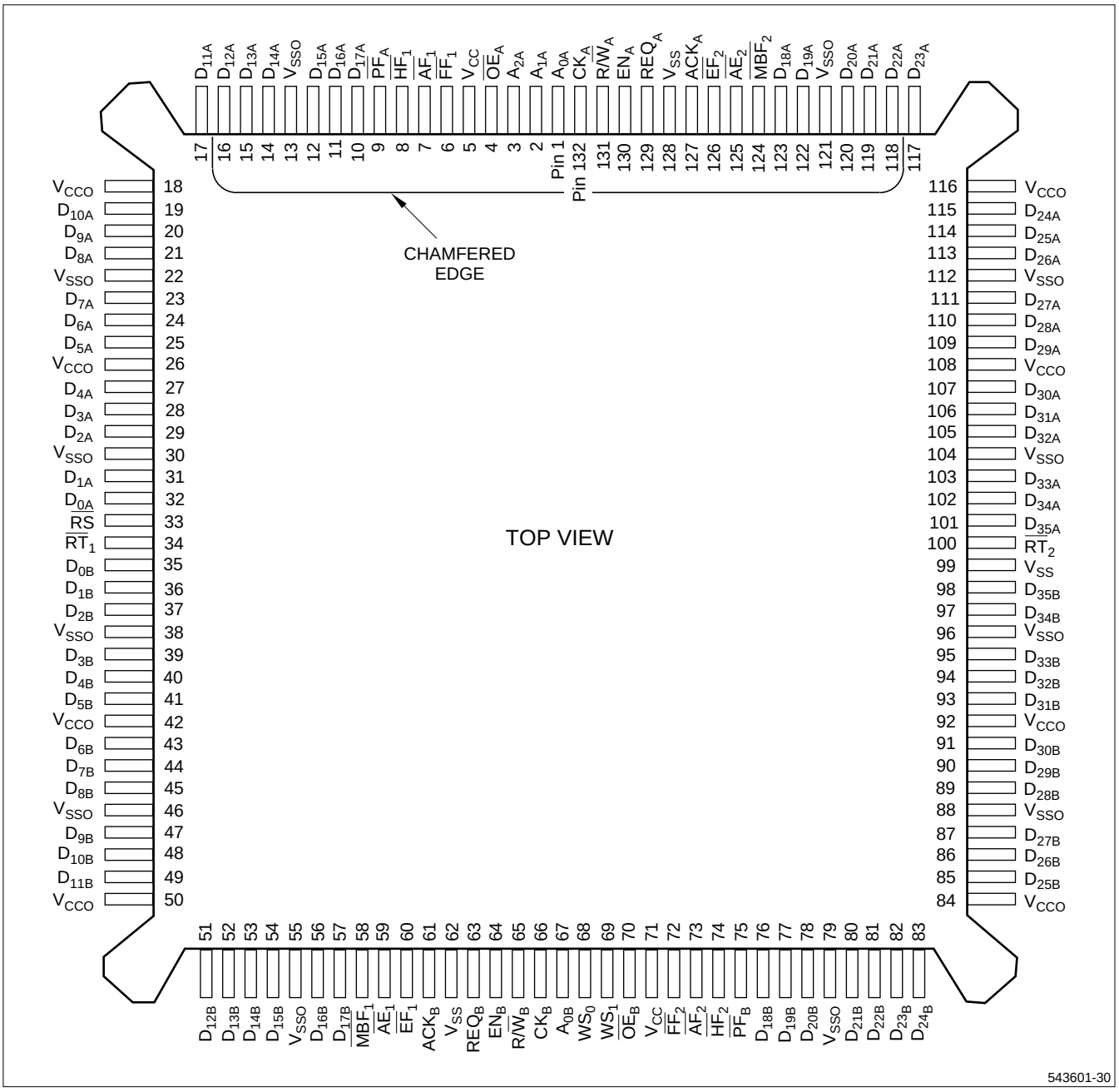


Figure 1. Pin Connections for 132-Pin PQFP Package (Top View)

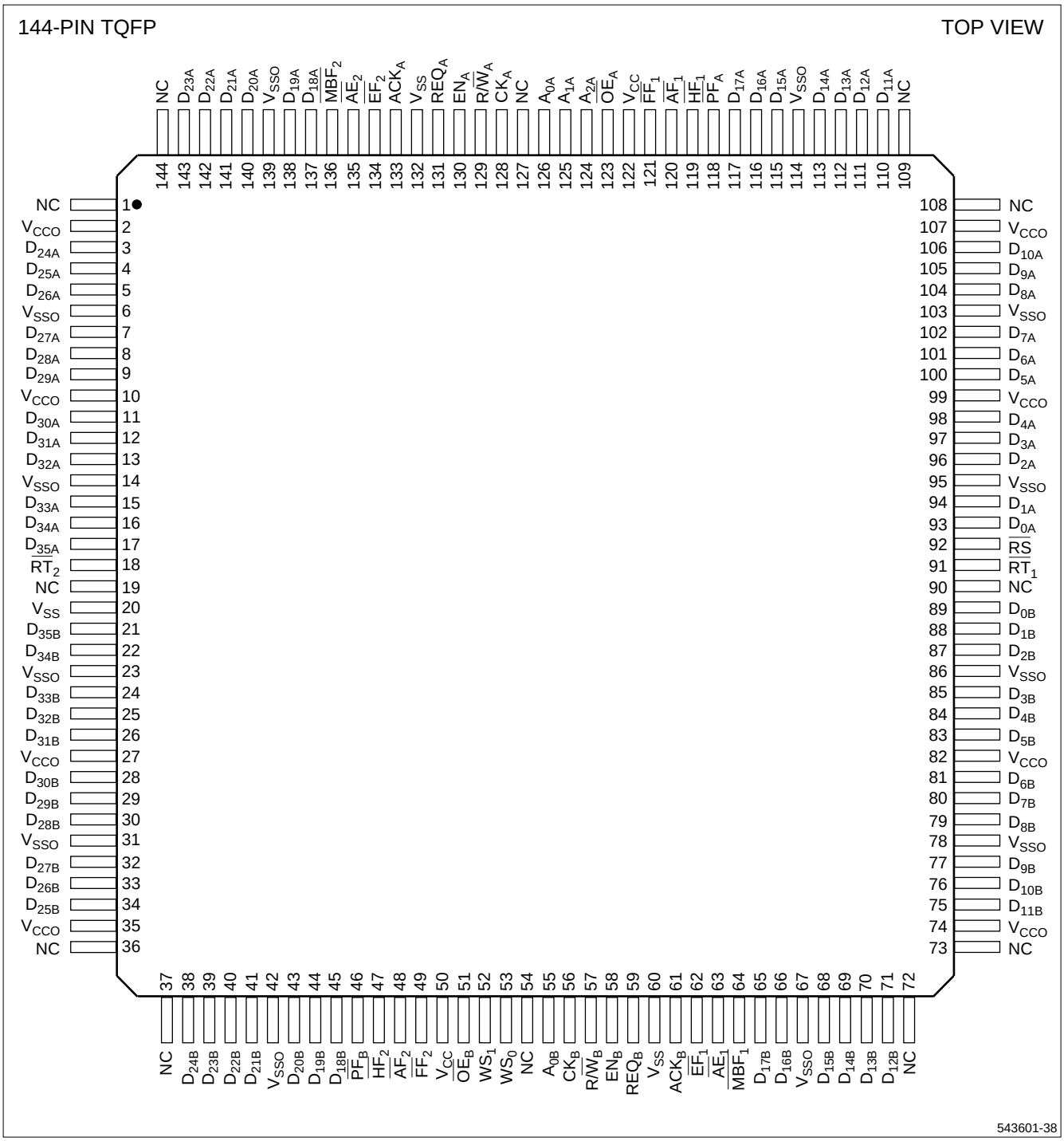


Figure 2. Pin Connections for 144-Pin TQFP Package (Top View)

PIN LIST

SIGNAL NAME	PQFP PIN NO.	TQFP PIN NO.
A_{0A}	1	126
A_{1A}	2	125
A_{2A}	3	124
$\overline{OE}_A$	4	123
$\overline{FF}_1$	6	121
$\overline{AF}_1$	7	120
$\overline{HF}_1$	8	119
$\overline{PF}_A$	9	118
D_{17A}	10	117
D_{16A}	11	116
D_{15A}	12	115
D_{14A}	14	113
D_{13A}	15	112
D_{12A}	16	111
D_{11A}	17	110
D_{10A}	19	106
D_{9A}	20	105
D_{8A}	21	104
D_{7A}	23	102
D_{6A}	24	101
D_{5A}	25	100
D_{4A}	27	98
D_{3A}	28	97
D_{2A}	29	96
D_{1A}	31	94
D_{0A}	32	93
$\overline{RS}$	33	92
$\overline{RT}_1$	34	91
D_{0B}	35	89
D_{1B}	36	88
D_{2B}	37	87
D_{3B}	39	85
D_{4B}	40	84
D_{5B}	41	83
D_{6B}	43	81
D_{7B}	44	80
D_{8B}	45	79
D_{9B}	47	77
D_{10B}	48	76
D_{11B}	49	75
D_{12B}	51	71
D_{13B}	52	70
D_{14B}	53	69
D_{15B}	54	68

SIGNAL NAME	PQFP PIN NO.	TQFP PIN NO.
D_{16B}	56	66
D_{17B}	57	65
$\overline{MBF}_1$	58	64
$\overline{AE}_1$	59	63
$\overline{EF}_1$	60	62
ACK_B	61	61
REQ_B	63	59
EN_B	64	58
$R/\overline{W}_B$	65	57
CK_B	66	56
A_{0B}	67	55
WS_0	68	53
WS_1	69	52
$\overline{OE}_B$	70	51
$\overline{FF}_2$	72	49
$\overline{AF}_2$	73	48
$\overline{HF}_2$	74	47
$\overline{PF}_B$	75	46
D_{18B}	76	45
D_{19B}	77	44
D_{20B}	78	43
D_{21B}	80	41
D_{22B}	81	40
D_{23B}	82	39
D_{24B}	83	38
D_{25B}	85	34
D_{26B}	86	33
D_{27B}	87	32
D_{28B}	89	30
D_{29B}	90	29
D_{30B}	91	28
D_{31B}	93	26
D_{32B}	94	25
D_{33B}	95	24
D_{34B}	97	22
D_{35B}	98	21
$\overline{RT}_2$	100	18
D_{35A}	101	17
D_{34A}	102	16
D_{33A}	103	15
D_{32A}	105	13
D_{31A}	106	12
D_{30A}	107	11
D_{29A}	109	9

SIGNAL NAME	PQFP PIN NO.	TQFP PIN NO.
D_{28A}	110	8
D_{27A}	111	7
D_{26A}	113	5
D_{25A}	114	4
D_{24A}	115	3
D_{23A}	117	143
D_{22A}	118	142
D_{21A}	119	141
D_{20A}	120	140
D_{19A}	122	138
D_{18A}	123	137
$\overline{MBF}_2$	124	136
$\overline{AE}_2$	125	135
$\overline{EF}_2$	126	134
ACK_A	127	133
REQ_A	129	131
EN_A	130	130
$R/\overline{W}_A$	131	129
CK_A	132	128
V_{CC}	5	122
V_{SSO}	13	114
NC		109
NC		108
V_{CCO}	18	107
V_{SSO}	22	103
V_{CCO}	26	99
V_{SSO}	30	95
NC		90
V_{SSO}	38	86
V_{CCO}	42	82
V_{SSO}	46	78
V_{CCO}	50	74
NC		73
NC		72
V_{SSO}	55	67
V_{SS}	62	60
NC		54
V_{CC}	71	50
V_{SSO}	79	42
NC		37
NC		36
V_{CCO}	84	35
V_{SSO}	88	31
V_{CCO}	92	27

NOTE:

PINS	COMMENTS
V_{CC}	Supply internal logic. Connected to each other.
V_{CCO}	Supply output drivers only. Connected to each other.

PINS	COMMENTS
V_{SS}	Supply internal logic. Connected to each other.
V_{SSO}	Supply output drivers only. Connected to each other.

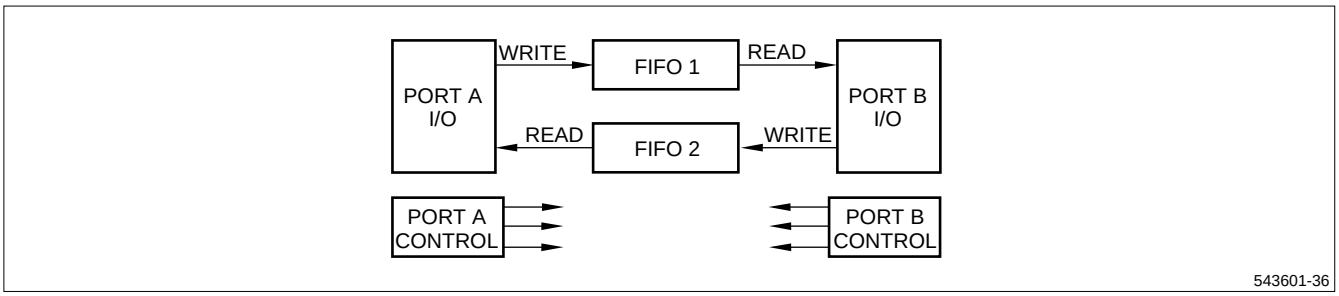


Figure 3a. Simplified LH543601 Block Diagram

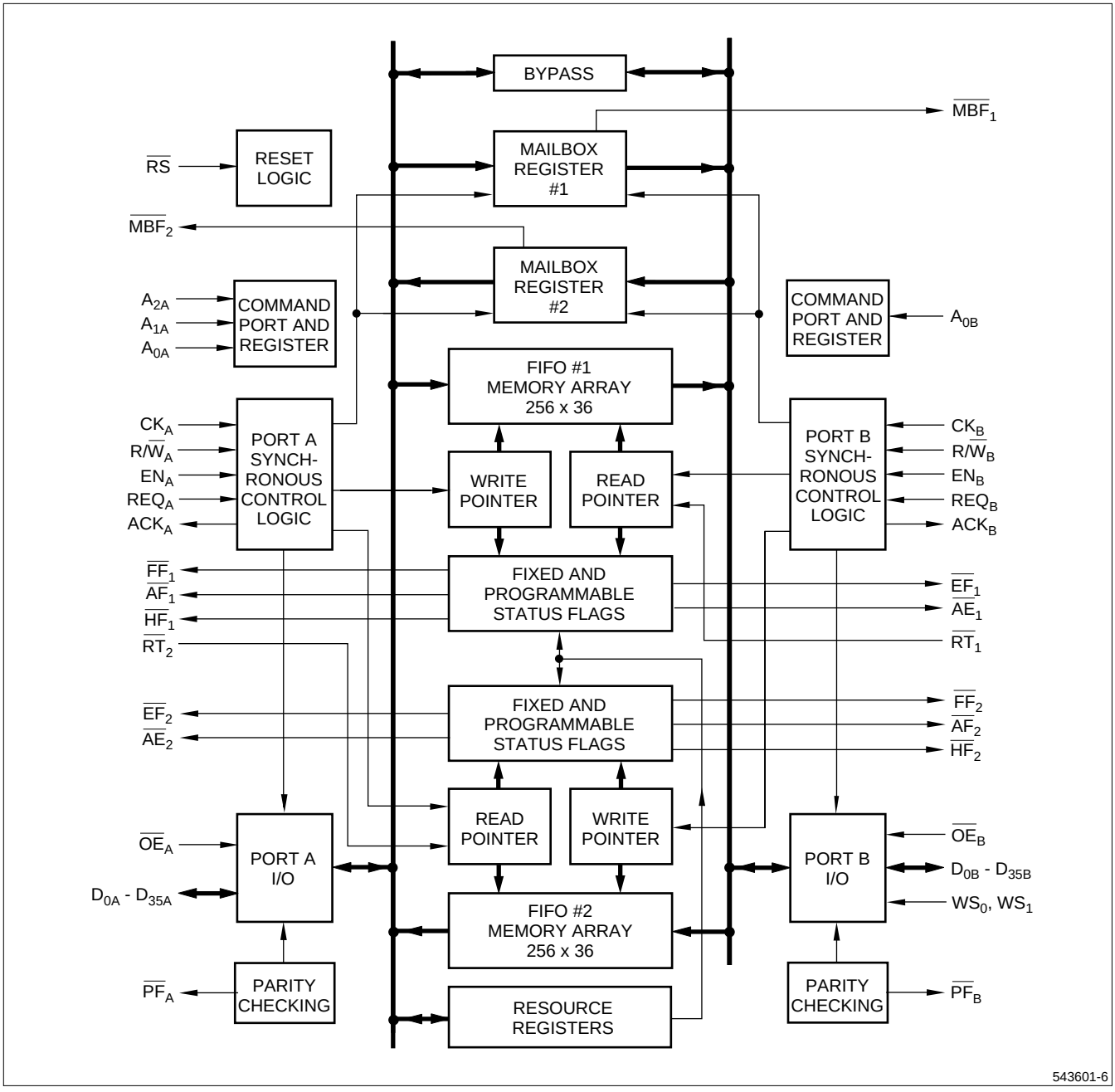


Figure 3b. Detailed LH543601 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE [1]	DESCRIPTION
		GENERAL
V_{CC}, V_{SS}	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CK_A	I	Port A Free-Running Clock
$R/\overline{W}_A$	I	Port A Edge-Sampled Read/Write Control
EN_A	I	Port A Edge-Sampled Enable
A_{0A}, A_{1A}, A_{2A}	I	Port A Edge-Sampled Address Pins
$\overline{OE}_A$	I	Port A Level-Sensitive Output Enable
REQ_A	I	Port A Request/Enable
$\overline{RT}_2$	I	FIFO #2 Retransmit
$D_{0A} – D_{35A}$	I/O/Z	Port A Bidirectional Data Bus
$\overline{FF}_1$	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}_1$	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_1$	O	FIFO #1 Half-Full Flag
$\overline{AE}_2$	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_2$	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}_2$	O	New-Mail-Alert Flag for Mailbox #2
$\overline{PF}_A$	O	Port A Parity Flag
ACK_A	O	Port A Acknowledge
		PORT B
CK_B	I	Port B Free-Running Clock
$R/\overline{W}_B$	I	Port B Edge-Sampled Read/Write Control
EN_B	I	Port B Edge-Sampled Enable
A_{0B}	I	Port B Edge-Sampled Address Pin
$\overline{OE}_B$	I	Port B Level-Sensitive Output Enable
WS_0, WS_1	I	Port B Word-Width Select
REQ_B	I	Port B Request/Enable
$\overline{RT}_1$	I	FIFO #1 Retransmit
$D_{0B} – D_{35B}$	I/O/Z	Port B Bidirectional Data Bus
$\overline{FF}_2$	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}_2$	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_2$	O	FIFO #2 Half-Full Flag
$\overline{AE}_1$	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_1$	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}_1$	O	New-Mail-Alert Flag for Mailbox #1
$\overline{PF}_B$	O	Port B Parity Flag
ACK_B	O	Port B Acknowledge

NOTE:
1. I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	–0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	–0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	–0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

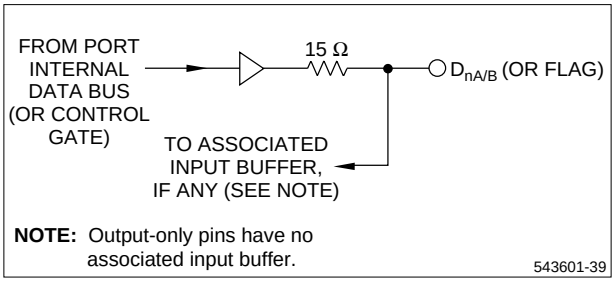


Figure 4. Structure of Series Resistor Input/Output Interface

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	–10		10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	–10		10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 8.0 mA			0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = –8.0 mA	2.4			V
I_{CC}	Average Supply Current [1, 2]	Measured at f_{CC} = max		180	280	mA
I_{CC2}	Average Standby Supply Current [1, 3]	All Inputs = V_{IHMIN} (Clocks idle)		13	25	mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC} – 0.2 V (Clocks idle)		0.002	0.4	mA
I_{CC4}	Power-Down Supply Current [1, 3]	All Inputs = V_{CC} – 0.2 V (Clocks at fcc = max)		6	10	mA

NOTES:

1. I_{CC}, I_{CC2}, I_{CC3}, and I_{CC4} are dependent upon actual output loading, and I_{CC} and I_{CC4} are also dependent on cycle rates. Specified values are with outputs open (for I_{CC}: C_L = 0 pF); and, for I_{CC} and I_{CC4}, operating at minimum cycle times.
2. I_{CC} (MAX.) using worst case conditions and data pattern. I_{CC} (TYP.) using V_{CC} = 5 V and and 'average' data pattern.
3. I_{CC2} (TYP.) and I_{CC4} (TYP.) using V_{CC} = 5 V and T_A = 25°C.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 5

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{OUT} (Output Capacitance)	8 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

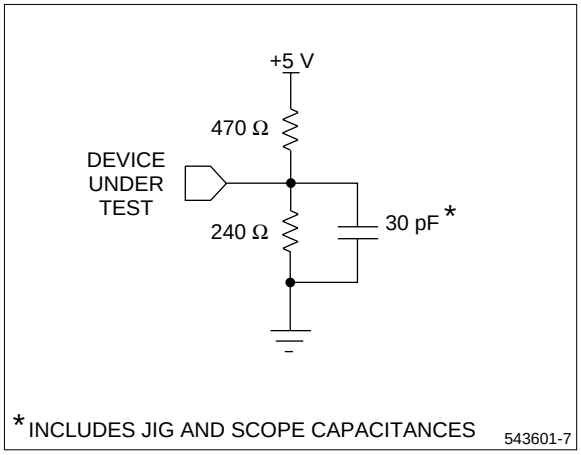


Figure 5. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DECRIPTION	–20		–25		–30		–35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{CC}	Clock Cycle Frequency	—	50	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	20	—	25	—	30	—	35	—	ns
t_{CH}	Clock HIGH Time	8	—	10	—	12	—	15	—	ns
t_{CL}	Clock LOW Time	8	—	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	10	—	12	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time	10.4	—	13	—	15	—	15	—	ns
t_{EH}	Enable Hold Time	0	—	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	10.4	—	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time	12	—	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time	0	—	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [6]	12	—	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [6]	0	—	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	12.8	—	16	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time	—	12	—	15	—	20	—	25	ns
t_{OH}	Output Hold Time	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to $D_0 – D_{35}$ Low-Z [2]	1.5	—	2.0	—	3.0	—	3.0	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to $D_0 – D_{35}$ High-Z [2]	—	9	—	12	—	15	—	20	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	17.6	—	22	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	17.6	—	22	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	17.6	—	22	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	16	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	16	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	12	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	13.6	—	17	—	20	—	25	ns
t_{RS}	Reset/Retransmit Pulse Width [7]	32/20	—	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [3]	16	—	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [3]	8	—	10	—	15	—	20	—	ns
t_{RF}	Reset LOW to Flag Valid	—	28	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [4]	20	—	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [5]	20	—	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	12	—	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	3	—	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	18	—	20	—	25	—	30	ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken LOW, and at least one rising edge and one falling edge of both CK_A and CK_B occur while $\overline{RS}$ is LOW. A reset operation is required after power-up, before the first write operation may occur. The LH543601 is fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFO's first physical memory locations. If the respective outputs are enabled, the initial contents of these first locations appear at the outputs. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE}_1/\overline{AE}_2$ flags get asserted within eight locations of an empty condition, and the $\overline{AF}_1/\overline{AF}_2$ flags likewise get asserted within eight locations of a full condition, for FIFO #1/FIFO #2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and cannot perform write or read operations independently on its own during reset.

The direction of the bypass data transmission is determined by th $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. Here, a 'write' operation means passing data from Port A to Port B, and a 'read' operation means passing data from Port B to Port A.

The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox-register access, control-register access (write only), and programmable flag-offset-value-register access. Port B has a single address input, A_{0B}, to select between FIFO access or mailbox-register access.

The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Resource-register select-input address definitions are summarized in Table 1.

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected for the address inputs ($A_{2A} – A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins ($D_{0A} – D_{35A}$ or $D_{0B} – D_{35B}$).

Normally, the appropriate Output Enable signal ($\overline{OE}_A$ or $\overline{OE}_B$) is HIGH, to disable the outputs at that port, so that the data word present on the bus from external sources gets stored. However, a 'loopback' mode of operation also is possible, in which the data word supplied by the outputs of one internal FIFO is 'turned around' at the port and read back into the other FIFO. In this mode, the outputs at the port are not disabled. To remain within specification for all timing parameters, the Clock Cycle Frequency must be reduced slightly below the value which otherwise would be permissible for that speed grade of LH543601.

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

FIFO Read

Port A reads from FIFO #2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; the FIFO address is selected for the address inputs ($A_{2A} – A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Read data

Table 1. Resource-Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offsets Register (36-Bit Mode)
H	L	L	Control Register (Parity Mode)
L	H	H	$\overline{AE}_1$ Flag Offset Register
L	H	L	$\overline{AF}_1$ Flag Offset Register
L	L	H	$\overline{AE}_2$ Flag Offset Register
L	L	L	$\overline{AF}_2$ Flag Offset Register
A_{0B}			RESOURCE
PORT B			
H			FIFO
L			Mailbox

OPERATIONAL DESCRIPTION (cont'd)

becomes valid on the data-bus pins (D_{0A} – D_{35A} or D_{0B} – D_{35B}) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous, Output Enable control input signals. Their effect is only to enable or disable the output drivers of the respective port. Disabling the outputs does *not* disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data words are retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for Full ($\overline{FF}_1$ and $\overline{FF}_2$), Half-Full ($\overline{HF}_1$ and $\overline{HF}_2$), and Empty ($\overline{EF}_1$ and $\overline{EF}_2$). $\overline{FF}_1$, $\overline{HF}_1$, and $\overline{EF}_1$ indicate the status of FIFO #1; and $\overline{FF}_2$, $\overline{HF}_2$, and $\overline{EF}_2$ indicate the status of FIFO #2.

A Full Flag is asserted following the first subsequent rising clock edge for a write operation which fills the FIFO. A Full Flag is deasserted following the first subsequent falling clock edge for a read operation to a full FIFO. A Half-Full Flag is updated following the first subsequent rising clock edge of a read or write operation to a FIFO which changes its 'half-full' status. An Empty Flag is asserted following the first subsequent rising clock edge for a read operation which empties the FIFO. An Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for Almost-Full ($\overline{AF}_1$ and $\overline{AF}_2$), and two for Almost-Empty ($\overline{AE}_1$ and $\overline{AE}_2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

An Almost-Full Flag is asserted following the first subsequent rising clock edge after a write operation which has partially filled the FIFO up to the 'almost-full' offset point. An Almost-Full Flag is deasserted following the first subsequent falling clock edge after a read operation which has partially emptied the FIFO down past the 'almost-full' offset point. An Almost-Empty Flag is asserted following the first subsequent rising clock edge after a read operation which has partially emptied the FIFO down to the 'almost-empty' offset point. An Almost-Empty Flag is deasserted following the first subsequent falling clock edge after a write operation which has partially filled the FIFO up past the 'almost-empty' offset point.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four eight-bit status words. Table 3 illustrates the data format for flag-programming words .

Also, Table 4 defines the meaning of each of the five flags, both the dedicated flags and the programmable flags, for the LH543601.

WARNING: Control inputs which may affect the computation of flag values at a port generally should not change while the clock for that port is HIGH, since some updating of flag values takes place on the *falling* edge of the clock.

Mailbox Operation

Two mailbox registers are provided for passing system hardware or software control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register #1, or reading from Mailbox Register #2, is synchronized to CK_A; and writing to Mailbox Register #2, or reading from Mailbox Register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register accesses. Each mailbox register has its own New-Mail-Alert Flag ($\overline{MBF}_1$ and $\overline{MBF}_2$), which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox-register read or write operations.

Request Acknowledge Handshake

A synchronous request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. The use of this feature is optional. When it is used, the Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does *not* prove that a FIFO write access or a FIFO read access actually took place. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a syn-

OPERATIONAL DESCRIPTION (cont'd)

chronized predictor of the Almost-Full Flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty Flag $\overline{AE}$ for read operations.

Outside the 'almost-full' region and the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every *third* cycle, to prevent an overrun of the FIFO's actual full or empty boundaries and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The 'almost-full region' is defined as 'that region, where the Almost-Full Flag is being asserted'; and the 'almost-empty region' as 'that region, where the Almost-Empty Flag is being asserted.' Thus, the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has *not* programmed them, then these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is *not* asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port *must* be asserted for that port to function at all – for FIFO, mailbox, or data-bypass operation.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated; and a block of up to 256 data words, which previously had been written into and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location, and the FIFO memory location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding Retransmit signal is being asserted.

Parity Checking

The Parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the Port A data bus or the Port B data bus respectively. The inputs to the parity-evaluation logic come directly (via isolation transistors) from the data-bus bonding *pads*, in each case. Thus, $\overline{PF}_A$ and $\overline{PF}_B$ provide parity-error indications for whatever 36-bit words are present at Port A and Port B respectively, regardless of whether those words originated within the LH543601 or in the external system.

The four bytes of a 36-bit data word are grouped as $D_0 – D_8$, $D_9 – D_{17}$, $D_{18} – D_{26}$, and $D_{27} – D_{35}$. The parity of each nine-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed and inverted, to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even parity or for odd parity during operation. Control-Register bit 00 (zero) selects the parity mode, odd or even. (See Table 3.)

All nine bits of each byte are treated alike by the parity logic. The byte parity over the nine bits is compared with the Parity Mode bit in the Control Register, to generate a byte-parity-error indication. Then, the four byte-parity-error signals are NORed together, to compute the assertive-LOW parity-flag value.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_0 and WS_1 control inputs. WS_0 and WS_1 both are tied HIGH for 36-bit access; they both are tied LOW for single-byte access. For double-byte access, WS_0 is tied HIGH and WS_1 is tied LOW. (See Table 2.)

In the single-byte-access or double-byte-access modes, FIFO write operations on Port B essentially pack the data to form 36-bit words, as viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Since the values for each status flag are computed by logic directly associated with one of the two FIFO-memory arrays, and not by logic associated with Port B, *the flag values reflect the array fullness situation in terms of complete 36-bit words*, and not in terms of bytes or double bytes.

However, there is no such restriction for switching from writing to reading, or from reading to writing, at Port B. As long as t_{RWS}, t_{DS}, and t_A are satisfied, $R\overline{W}_B$ may change state after *any* single-byte or double-byte access, and not only after a full 36-bit-word access.

Also, the word-width-matching feature continues to operate properly in 'loopback' mode.

Note that the programmable word-width-matching feature is *only* supported for FIFO accesses. Mailbox and Data Bypass operations do *not* support word-width matching between Port A and Port B. Tables 2, 3, and 4, and Figures 6a, 6b, 7a, and 7b summarize word-width selection for Port B.

Table 2. Port B Word-Width Selection

WS_1	WS_0	PORT B DATA WIDTH
H	H	36-Bit
H	L	(Reserved)
L	H	18-Bit
L	L	9-Bit

Table 3. Resource-Register Programming

RESOURCE-REGISTER ADDRESS			RESOURCE-REGISTER CONTENTS															
A_{2A}	A_{1A}	A_{0A}																
			NORMAL FIFO OPERATION															
			D_{35A}															D_{0A}
H	H	H	X...															...X
			MAILBOX															
			D_{35A}															D_{0A}
H	H	L	X...															...X
			$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ **FLAG OFFSETS REGISTER (36-BIT MODE)**															
			D_{35A}	D_{34A} . . . D_{27A}		D_{26A}	D_{25A} . . . D_{18A}		D_{17A}	D_{16A} . . . D_{9A}		D_{8A}	D_{7A} . . . D_{0A}					
H	L	H	X	$\overline{AF}_2$ Offset [1]		X	$\overline{AE}_2$ Offset [1]		X	$\overline{AF}_1$ Offset [1]		X	$\overline{AE}_1$ Offset [1]					
			CONTROL REGISTER: (WRITE-ONLY) PARITY EVEN/ODD															
			D_{35A}									D_{1A}	D0A					
H	L	L	X...									...X	Parity Mode [2]					
			8-BIT $\overline{AE}_1$ FLAG OFFSET REGISTER															
			D_{35A}									D_{8A}	D_{7A} . . . D_{0A}					
L	H	H	X...									...X	$\overline{AE}_1$ Offset [1]					
			8-BIT $\overline{AF}_1$ FLAG OFFSET REGISTER															
			D_{35A}									D_{8A}	D_{7A} . . . D_{0A}					
L	H	L	X...									...X	$\overline{AF}_1$ Offset [1]					
			8-BIT $\overline{AE}_2$ FLAG OFFSET REGISTER															
			D_{35A}									D_{8A}	D_{7A} . . . D_{0A}					
L	L	H	X...									...X	$\overline{AE}_2$ Offset [1]					
			8-BIT $\overline{AF}_2$ FLAG OFFSET REGISTER															
			D_{35A}									D_{8A}	D_{7A} . . . D_{0A}					
L	L	L	X...									...X	$\overline{AF}_2$ Offset [1]					

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 4. Flag Definition Table [1]

FLAG	VALID READ CYCLES REMAINING				VALID WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-p	256	0	255-p	0	p	p + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	q	q + 1	256	256-q	256	0	255-q
$\overline{EF}$	0	0	1	256	256	256	0	255

NOTES:

1. q = Programmable-Almost-Empty Offset value. (Default value: q = 8.)
2. p = Programmable-Almost-Full Offset value. (Default value: p = 8.)

PORT B WORD-WIDTH SELECTION

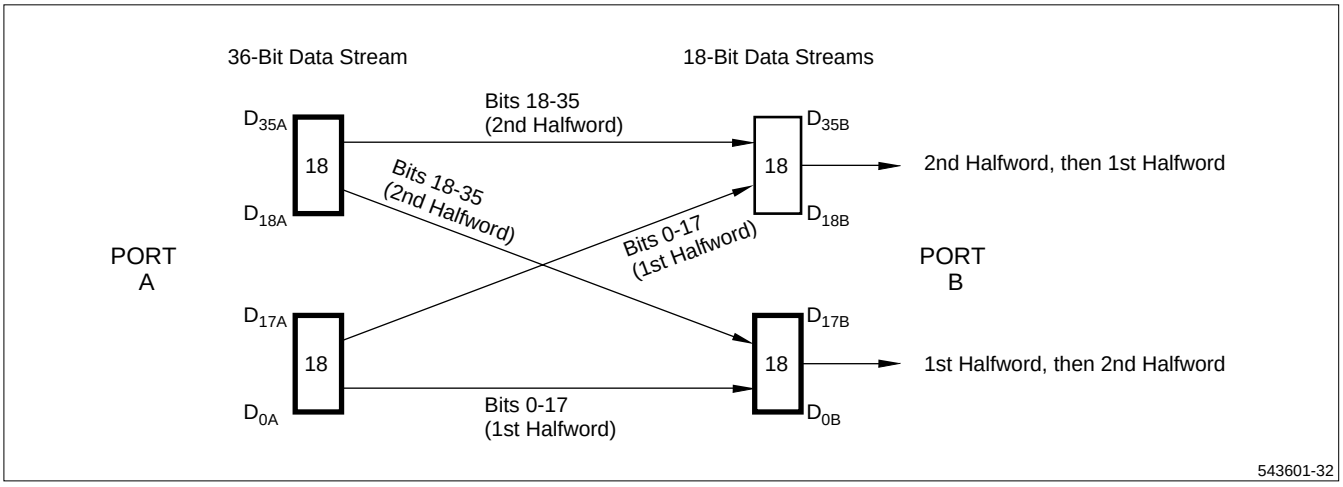


Figure 6a. 36-to-18 Funneling Through FIFO #1

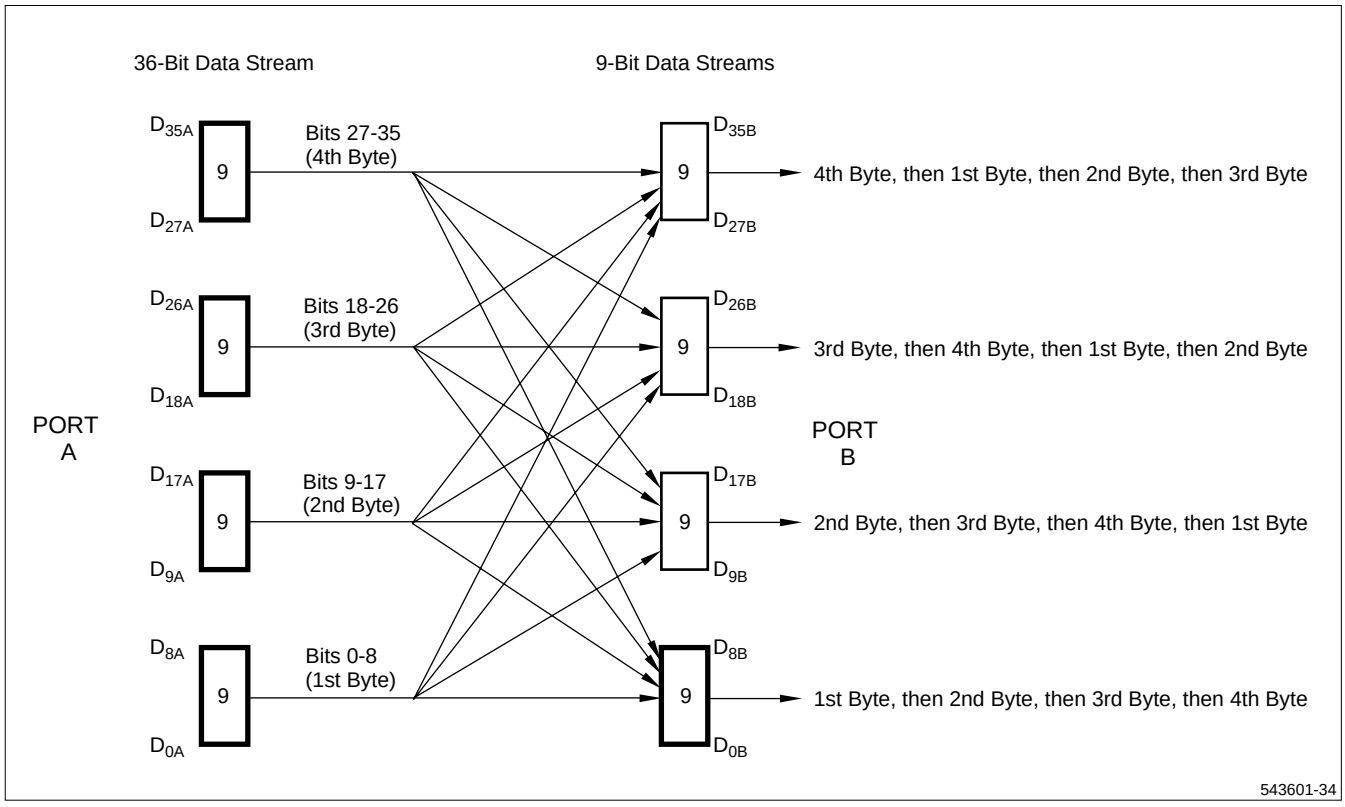


Figure 6b. 36-to-9 Funneling Through FIFO #1

NOTES:

1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to read D_{0B} – D_{35B}, and three dummy words should be passed through initially. Also, incomplete data words may occur, when the word width is changed from shorter to longer at an inappropriate point in the data block passing through the FIFO.

PORT B WORD-WIDTH SELECTION

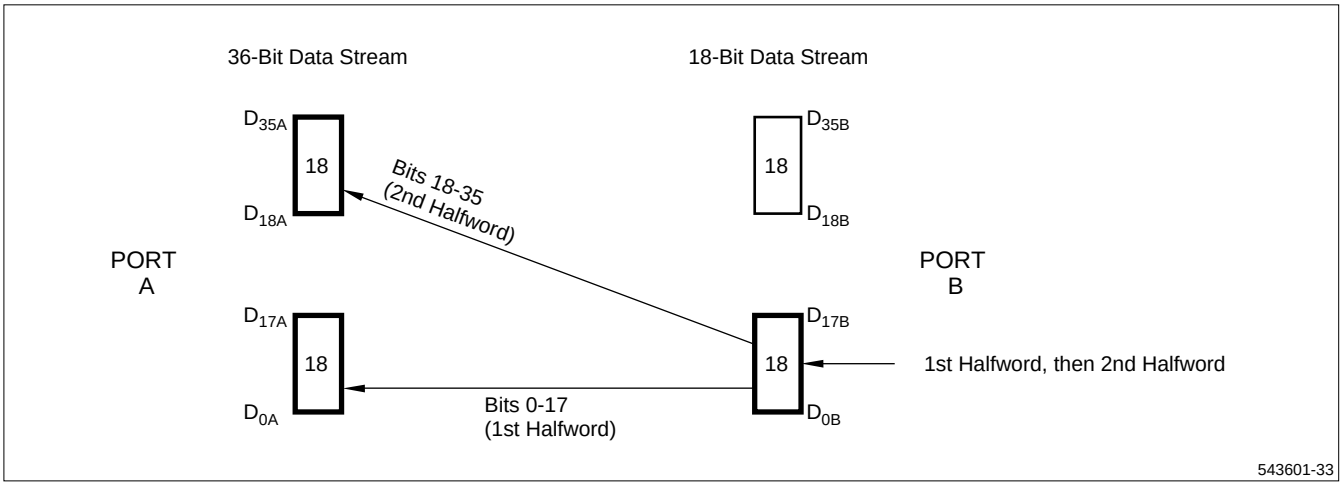


Figure 7a. 18-to-36 Defunneling Through FIFO #2

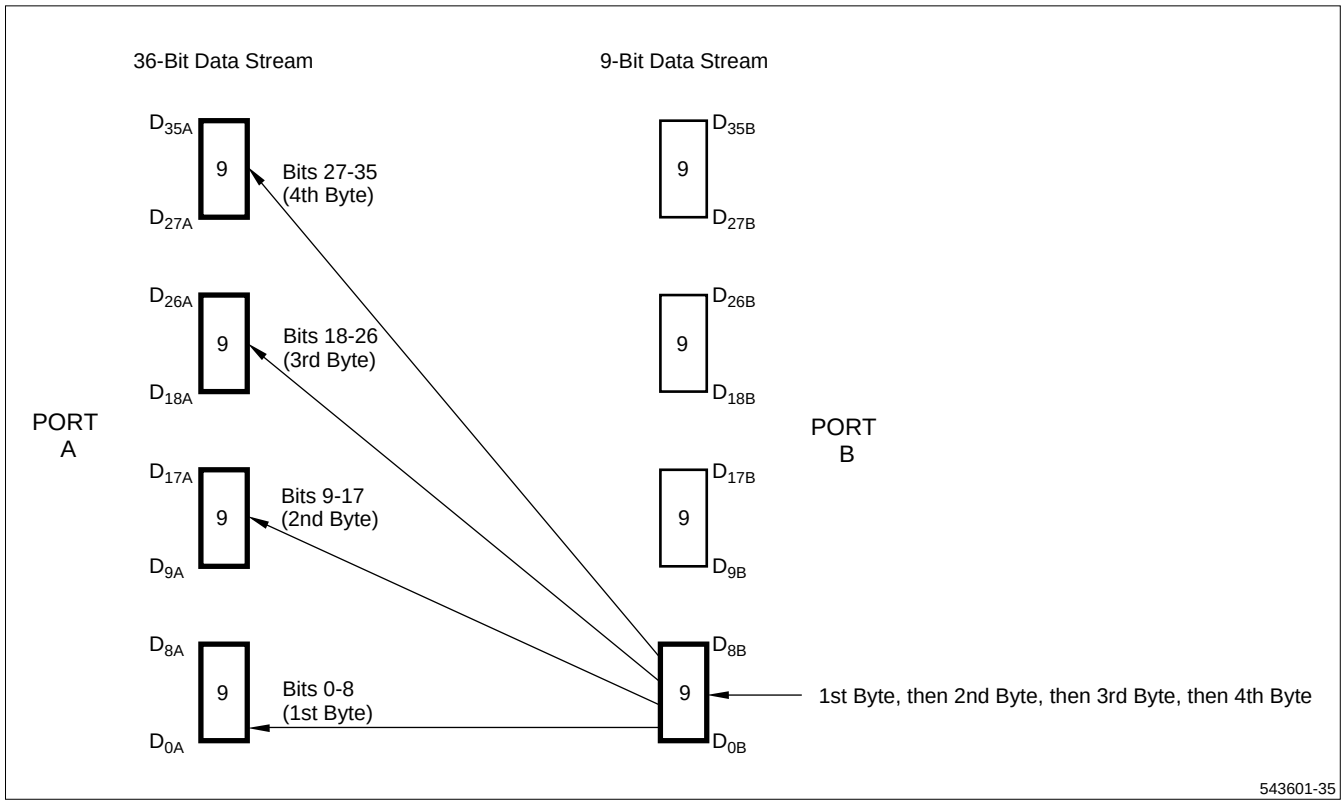
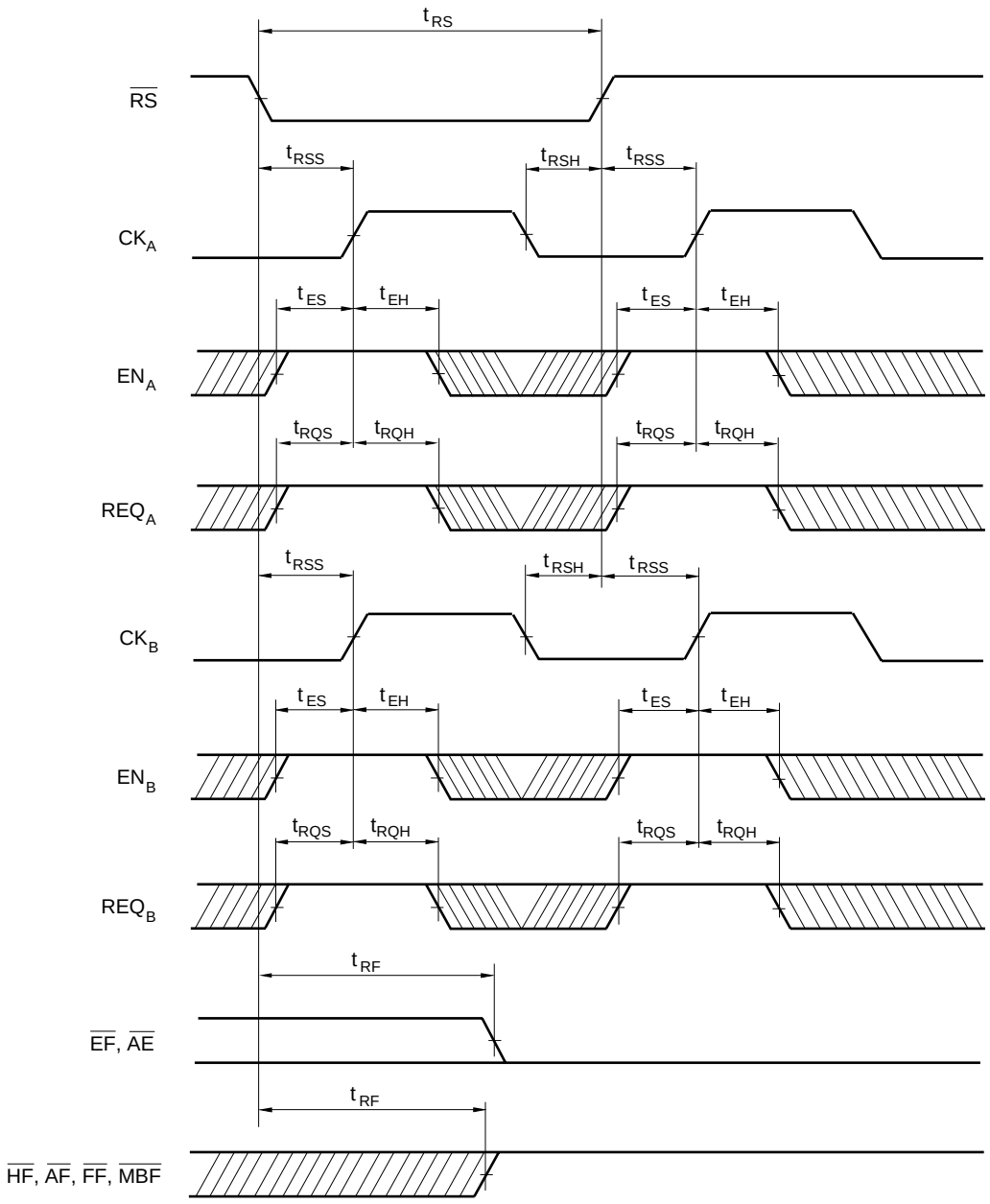


Figure 7b. 9-to-36 Defunneling Through FIFO #2

NOTES:

1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to send data, and three dummy words should be passed through initially. Also, incomplete data words may occur, when the word width is changed from shorter to longer at an inappropriate point in the data block passing through the FIFO.

TIMING DIAGRAMS



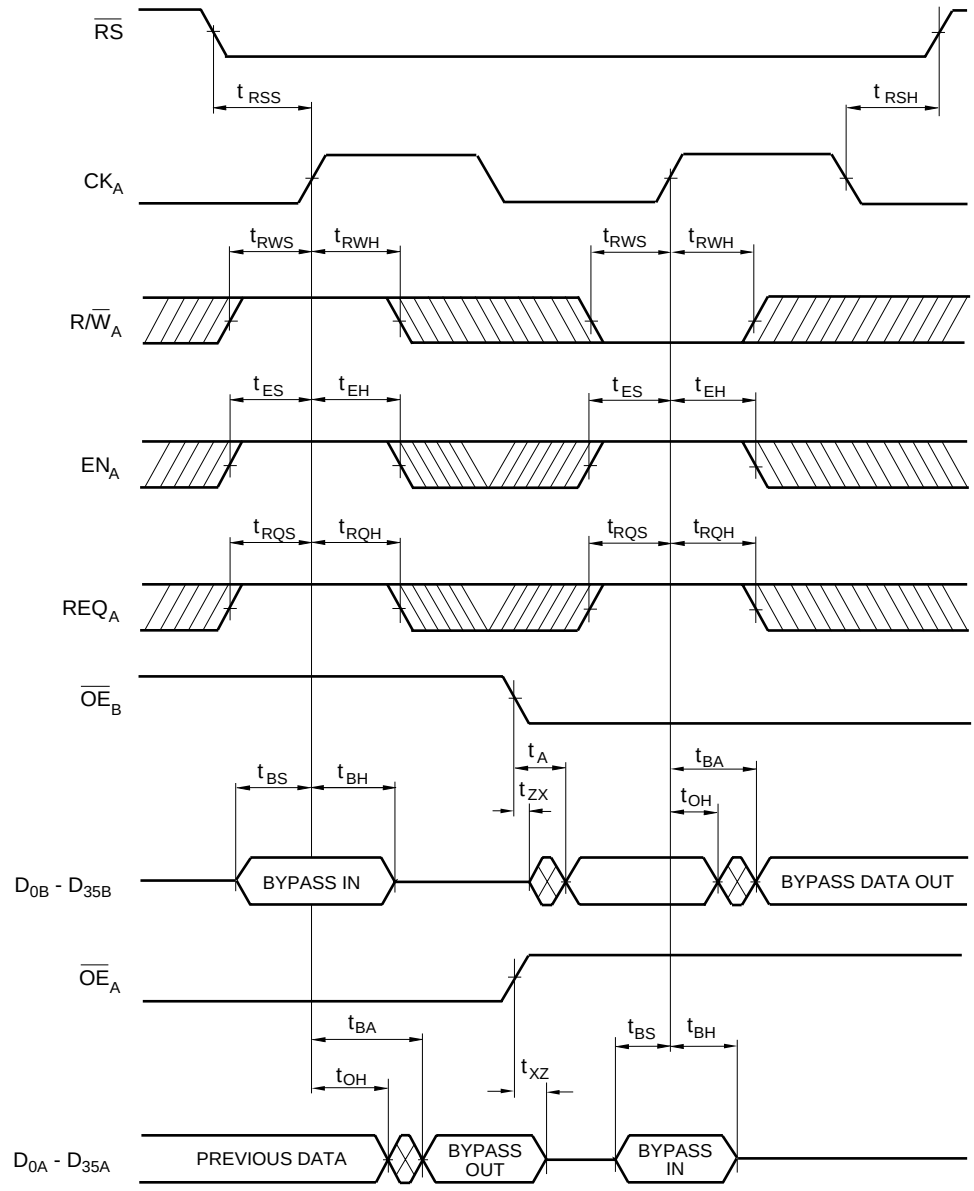
NOTES:

1. $\overline{RS}$ overrides all other input signals, except for $R/\overline{W}_A$, EN_A, and REQ_A. It operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted. However, at least one rising edge and one falling edge of both CK_A and CK_B must occur while $\overline{RS}$ is being asserted (is LOW), with timing as defined by t_{RSS} and t_{RSH}.
2. Otherwise, t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity-check even/odd selection (Control Register bit 00) is initialized to odd byte parity at reset (HIGH).
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

543601-26

Figure 8. Reset Timing

TIMING DIAGRAMS (cont'd)



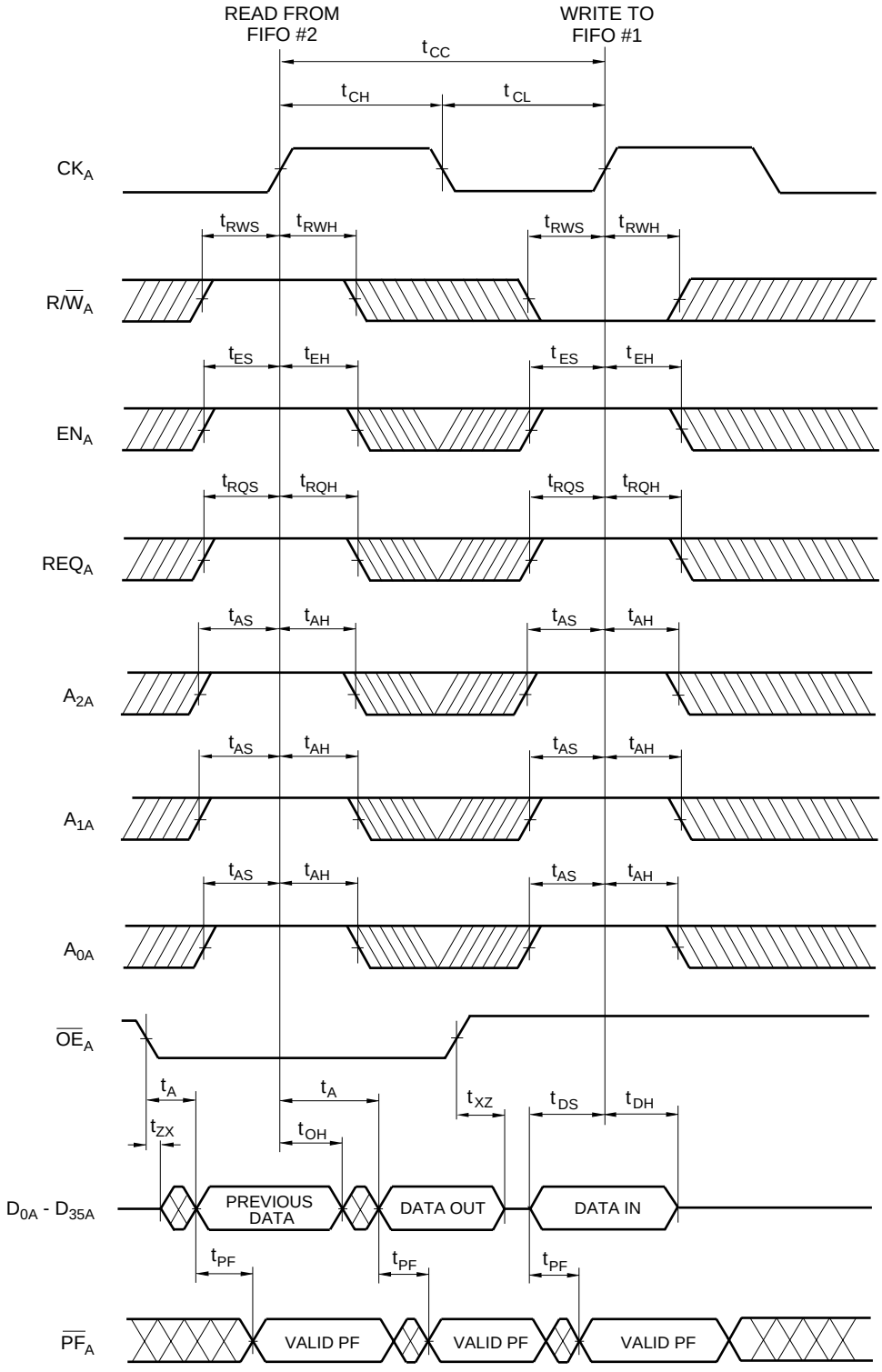
NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, EN_A, and REQ_A control the transmission of data between ports at reset.

543601-27

Figure 9. Data Bypass Timing

TIMING DIAGRAMS (cont'd)



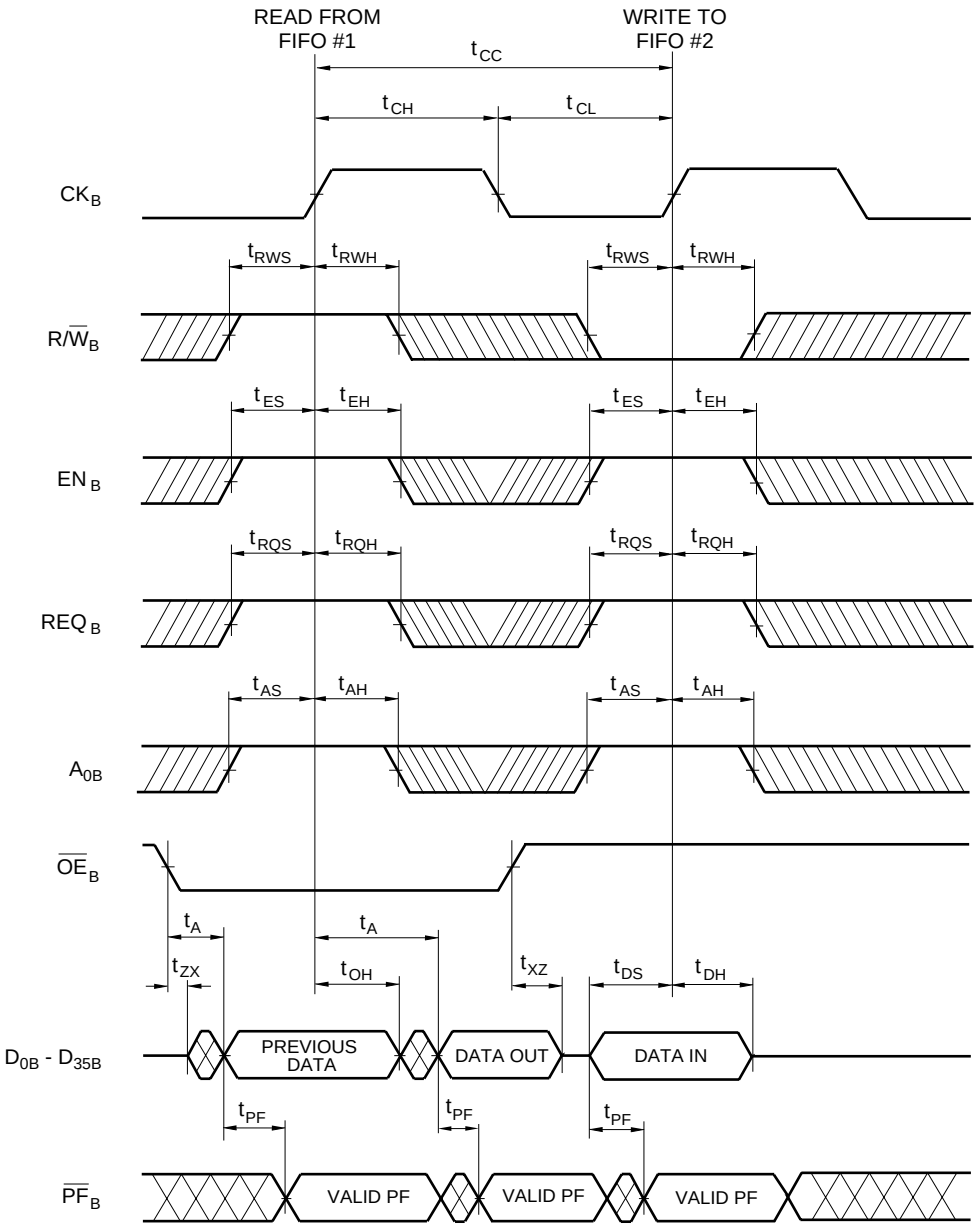
NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

543601-24

Figure 10. Port A FIFO Read/Write

TIMING DIAGRAMS (cont'd)



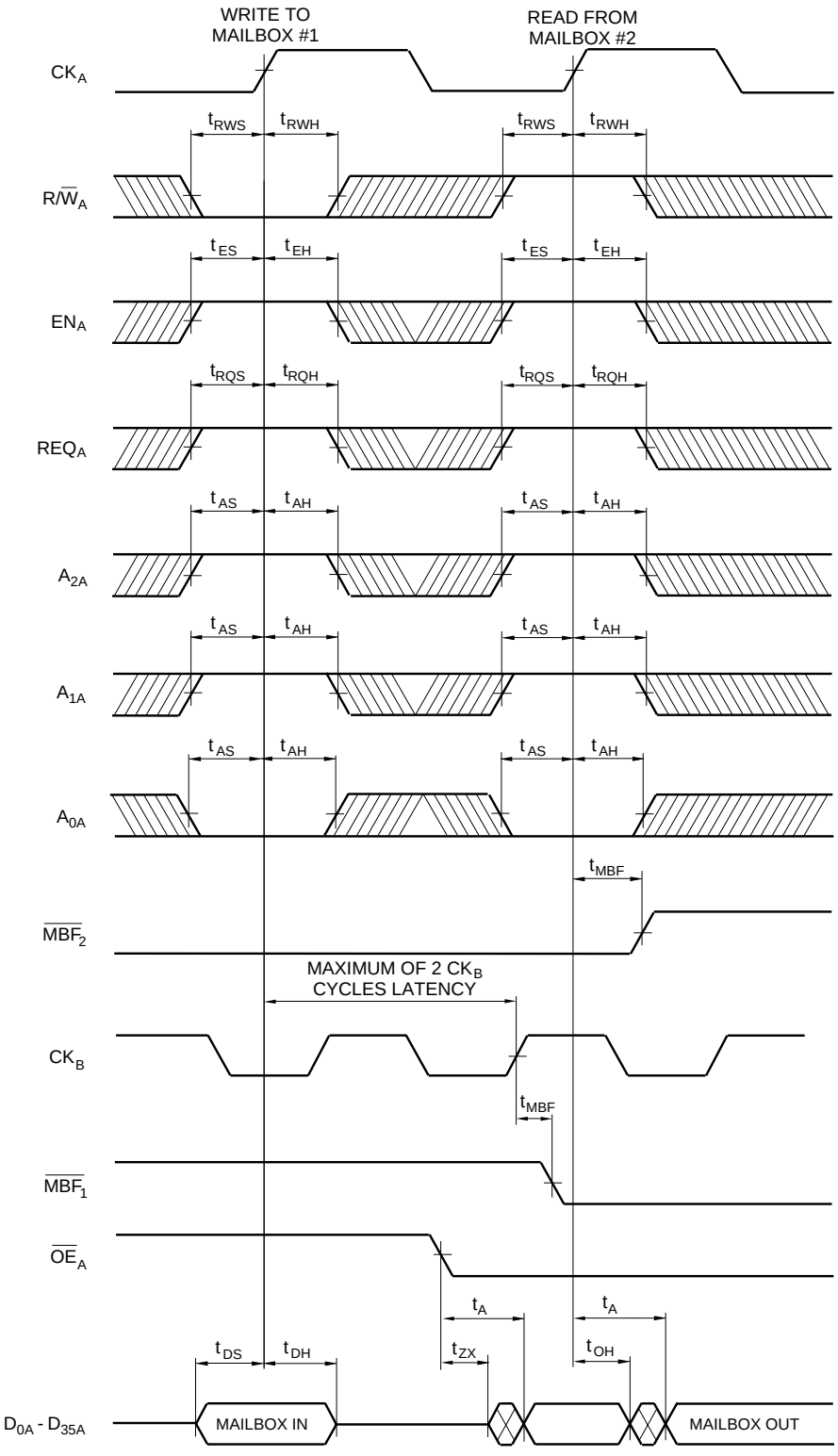
NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

543601-25

Figure 11. Port B FIFO Read/Write

TIMING DIAGRAMS (cont'd)



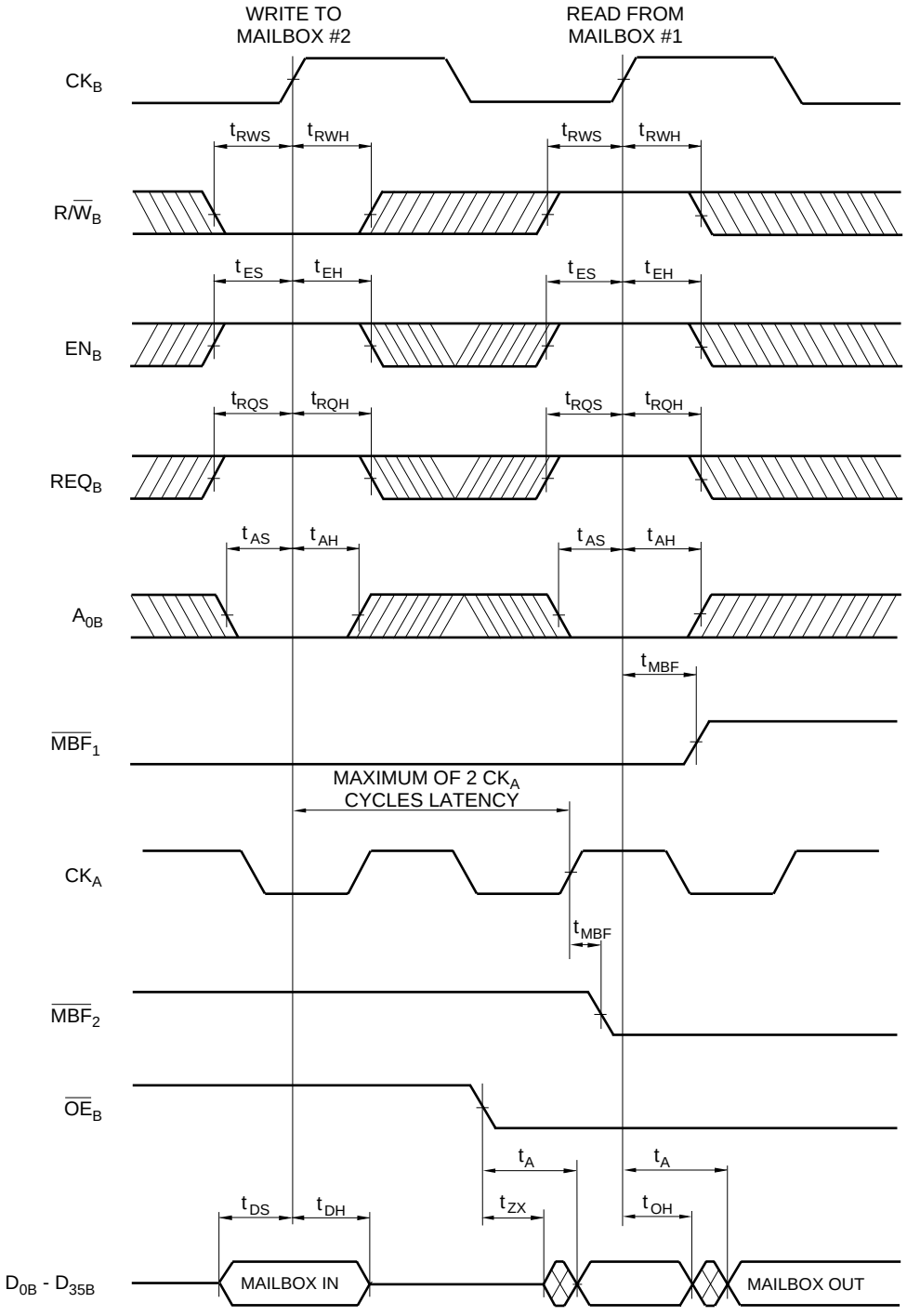
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF}_1$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

543601-22

Figure 12. Port A Mailbox Access

TIMING DIAGRAMS (cont'd)



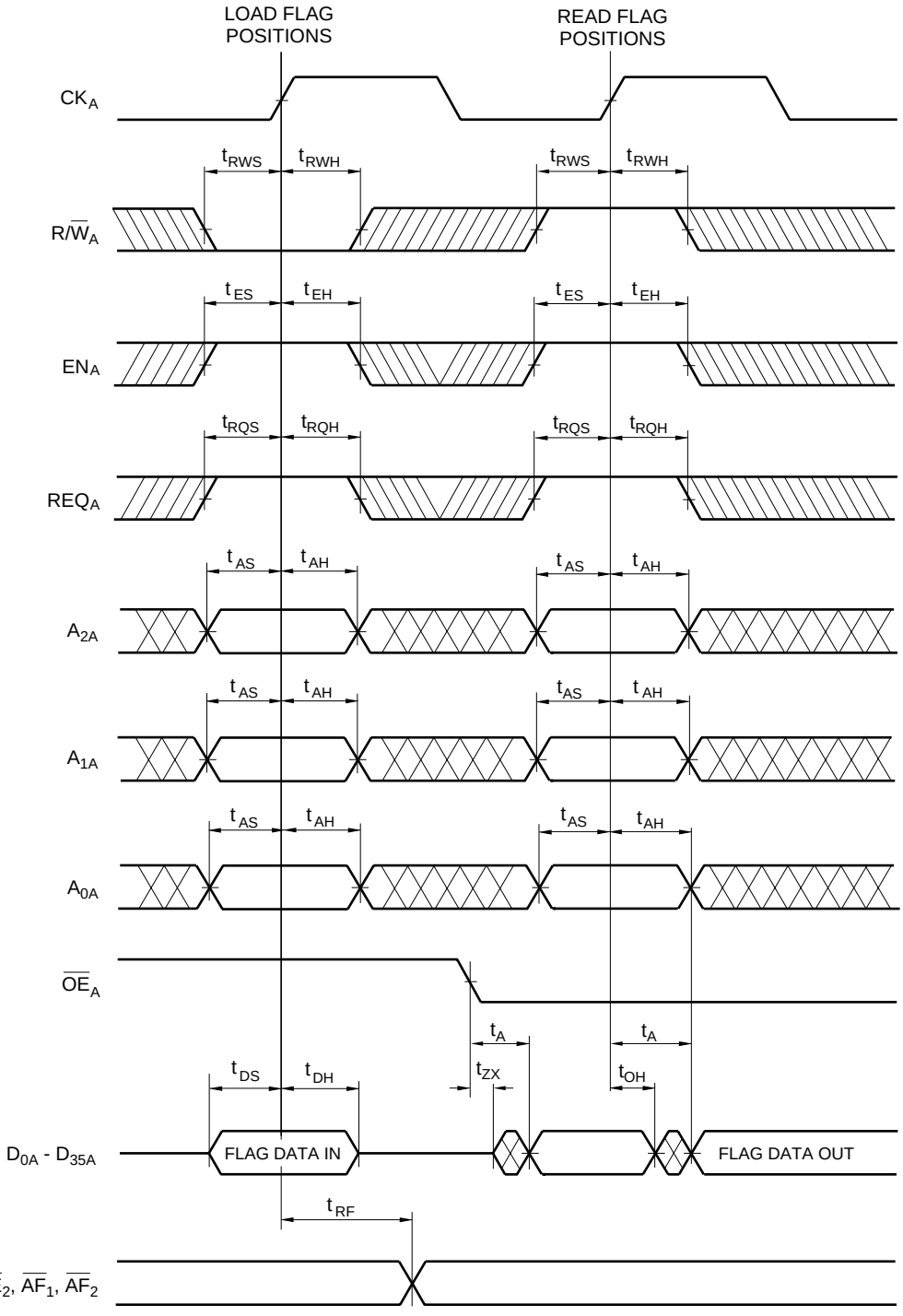
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

543601-23

Figure 13. Port B Mailbox Access

TIMING DIAGRAMS (cont'd)



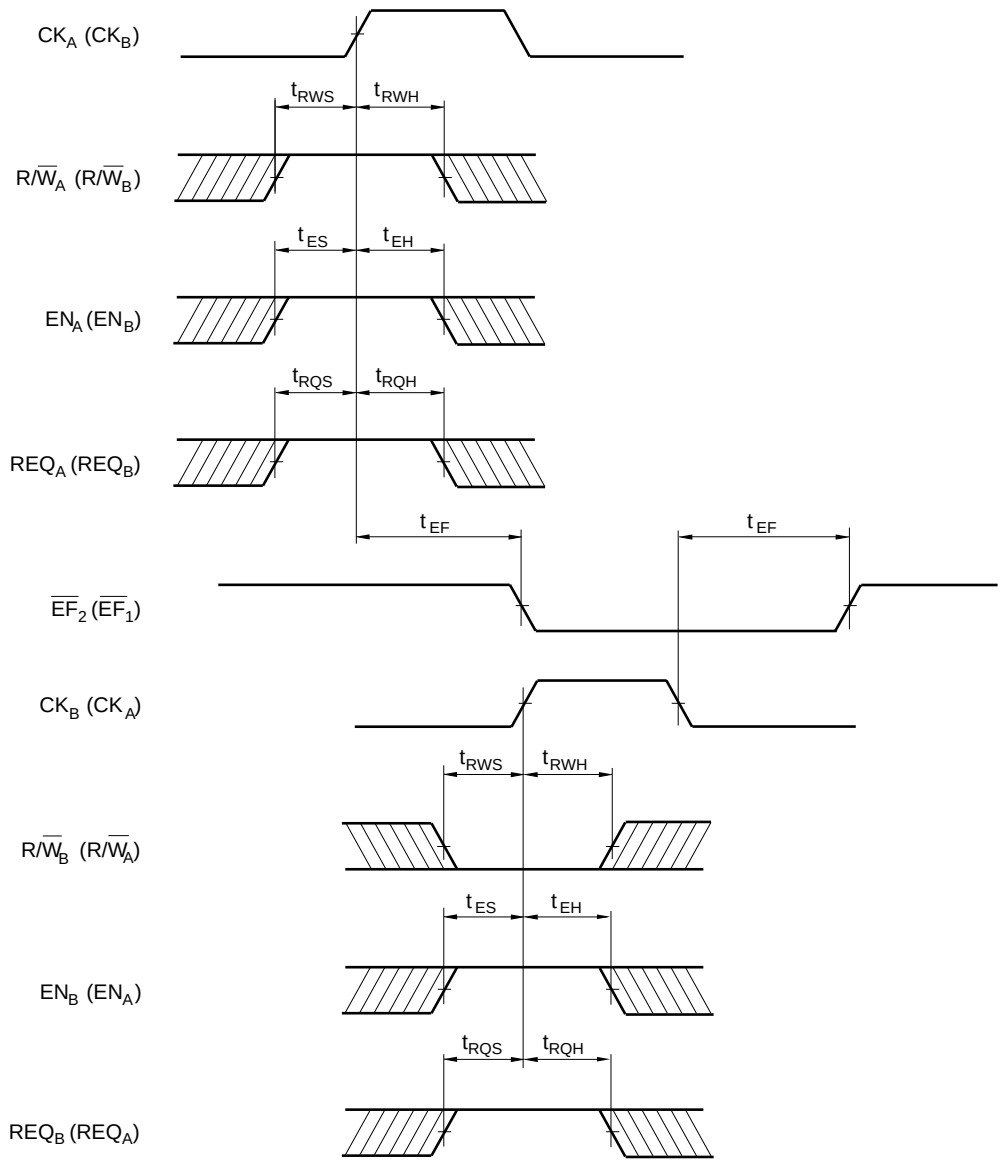
NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.
3. The Control Register may be loaded as shown here, with A_{2A}, A_{1A}, A_{0A} = HLL. However, it is not available for reading back.

543601-18

Figure 14. Flag Programming

TIMING DIAGRAMS (cont'd)

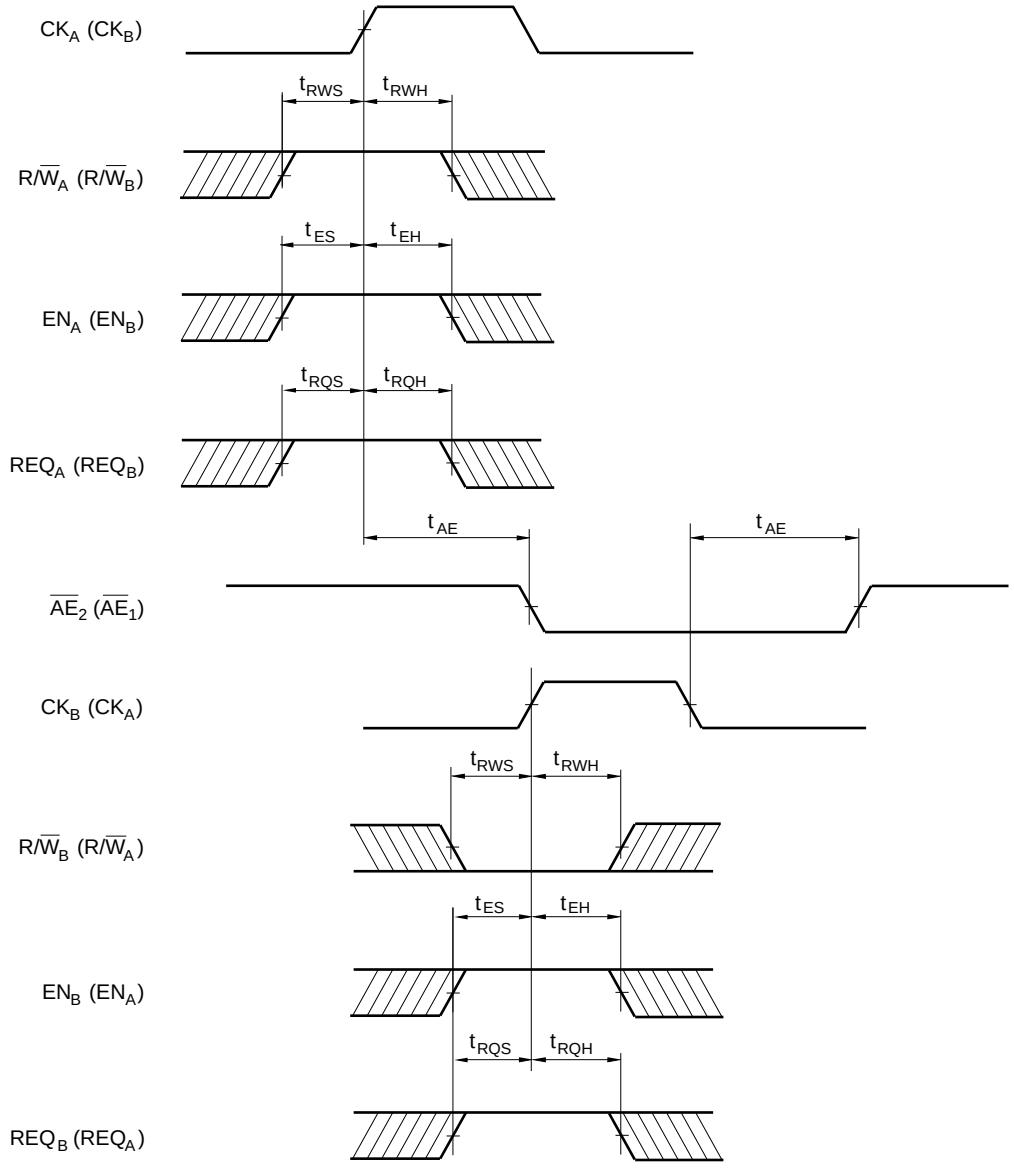


NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Empty Flags is controlled by rising clock edges, whereas deassertion of the Empty Flags is controlled by falling clock edges.

543601-1

Figure 15. Empty Flag Timing

TIMING DIAGRAMS (cont'd)



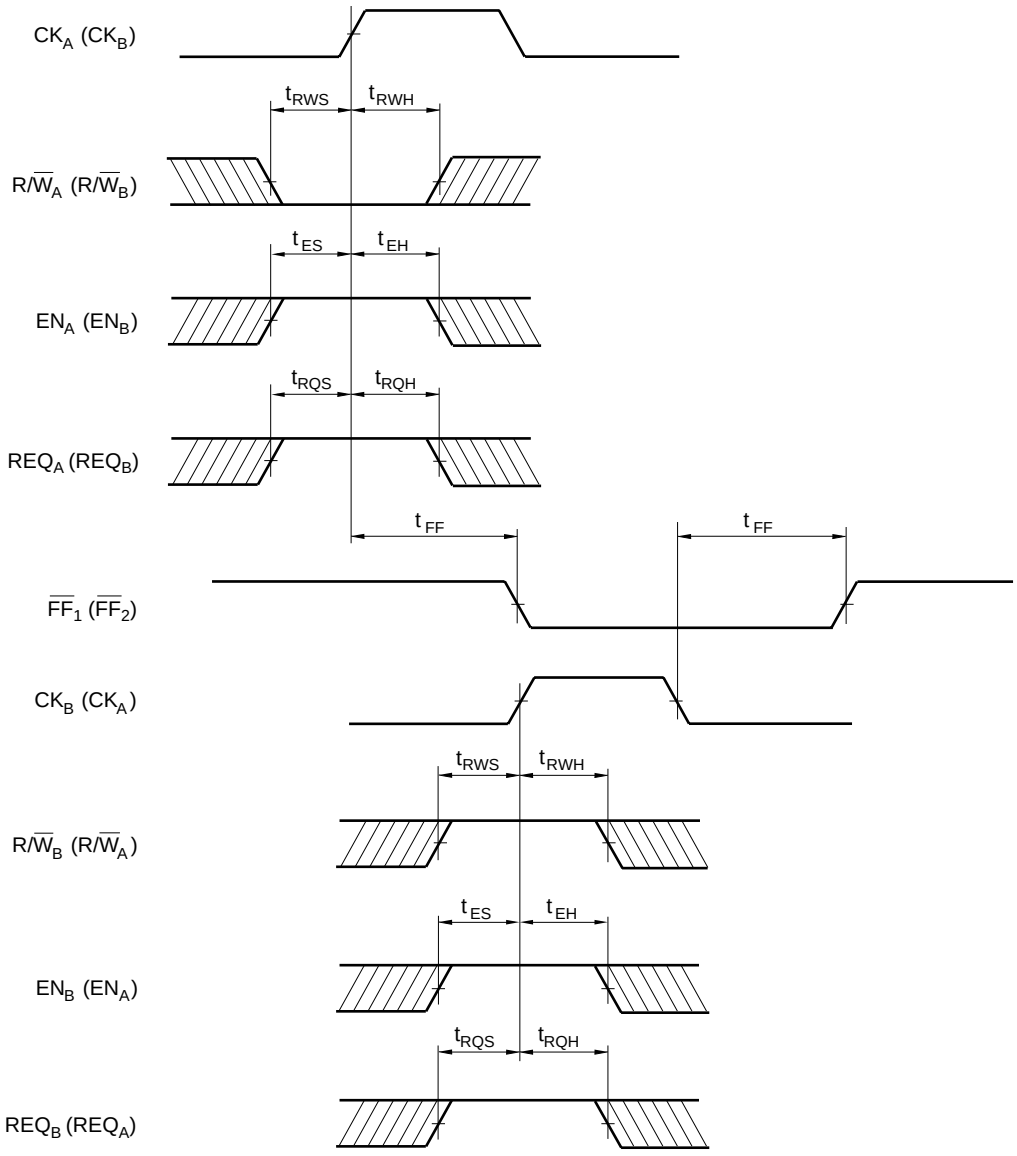
NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #2 operation. Parameters with parentheses apply to FIFO #1 operation.
3. Assertion of the Almost-Empty Flags is controlled by rising clock edges, whereas deassertion of the Almost-Empty Flags is controlled by falling clock edges.

543601-2

Figure 16. Almost-Empty Flag Timing

TIMING DIAGRAMS (cont'd)

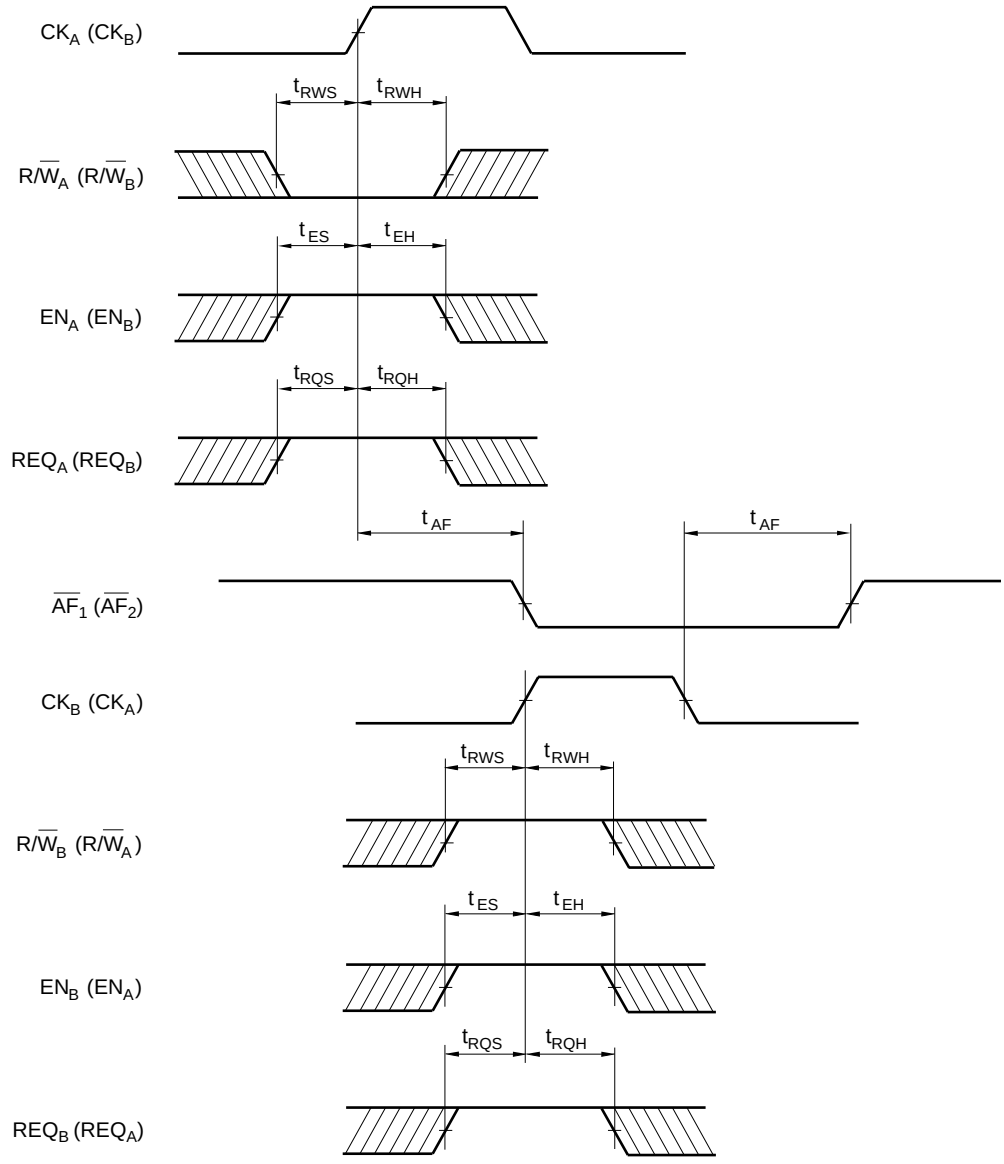


NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Full Flags is controlled by rising clock edges, whereas deassertion of the Full Flags is controlled by falling clock edges.

543601-3

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

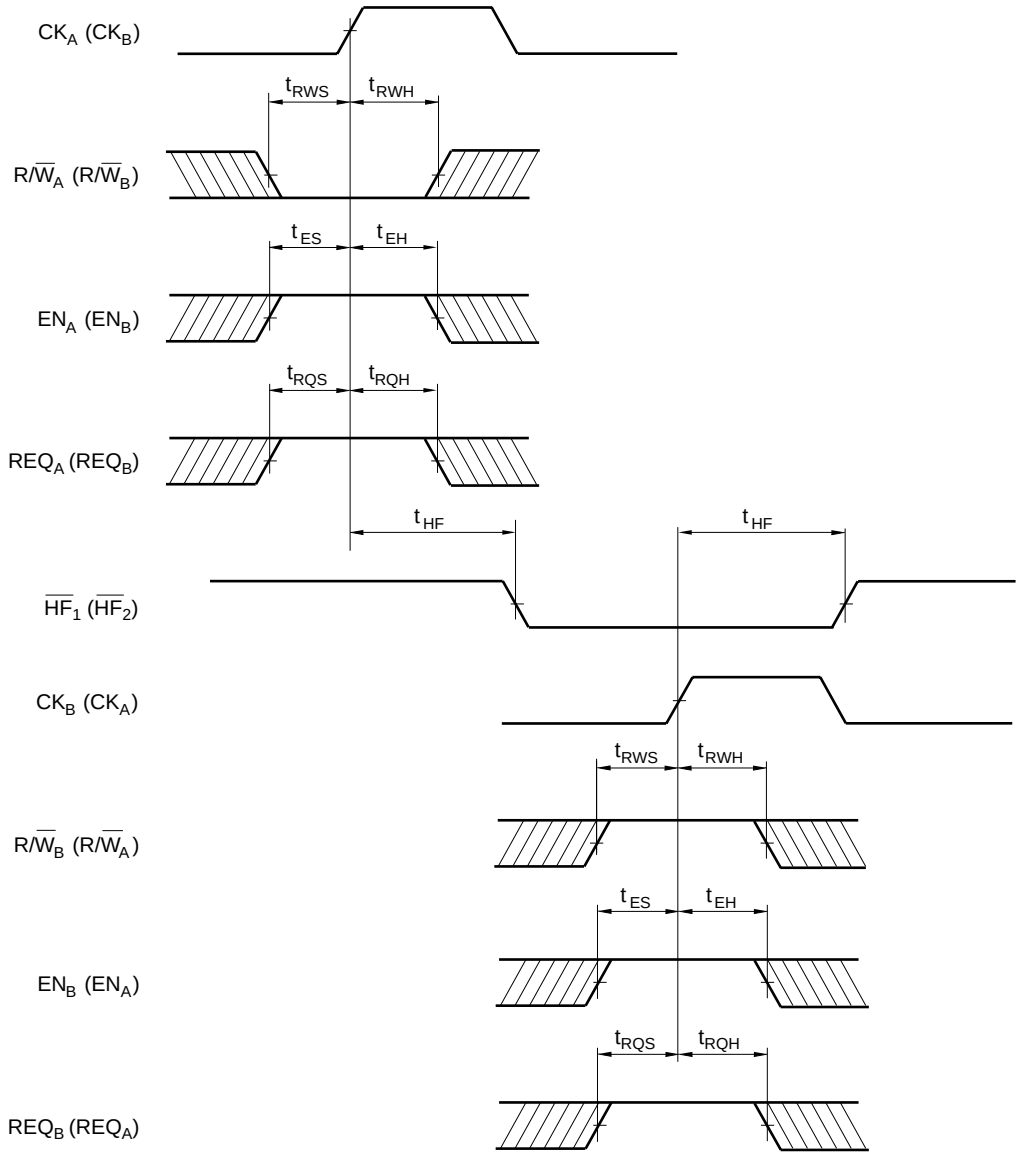


NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Assertion of the Almost-Full Flags is controlled by rising clock edges, whereas deassertion of the Almost-Full Flags is controlled by falling clock edges.

543601-4

Figure 18. Almost-Full Flag Timing

TIMING DIAGRAMS (cont'd)

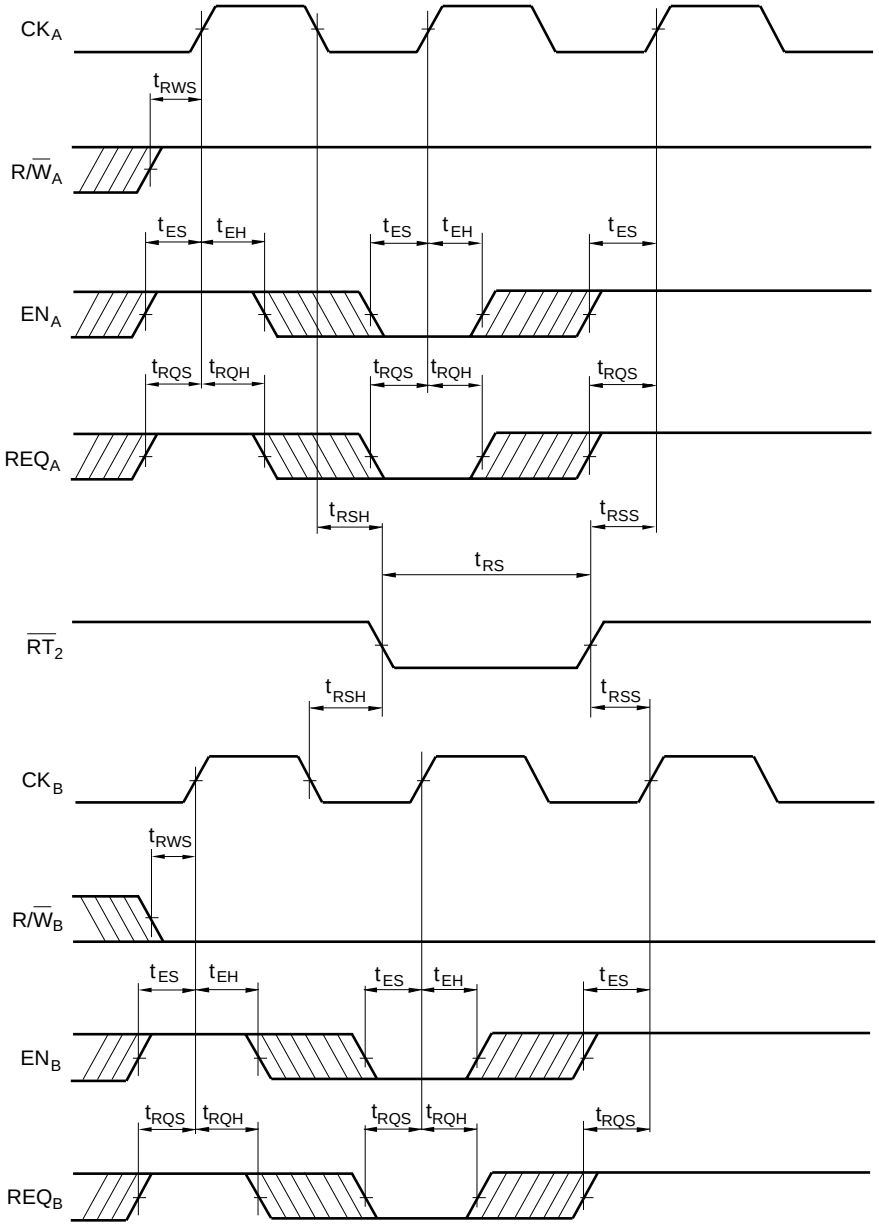


NOTES:
1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. Parameters without parentheses apply to FIFO #1 operation. Parameters with parentheses apply to FIFO #2 operation.
3. Both assertion and deassertion of the Half-Full Flags are controlled entirely by rising clock edges, rather than by falling clock edges.

543601-5

Figure 19. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



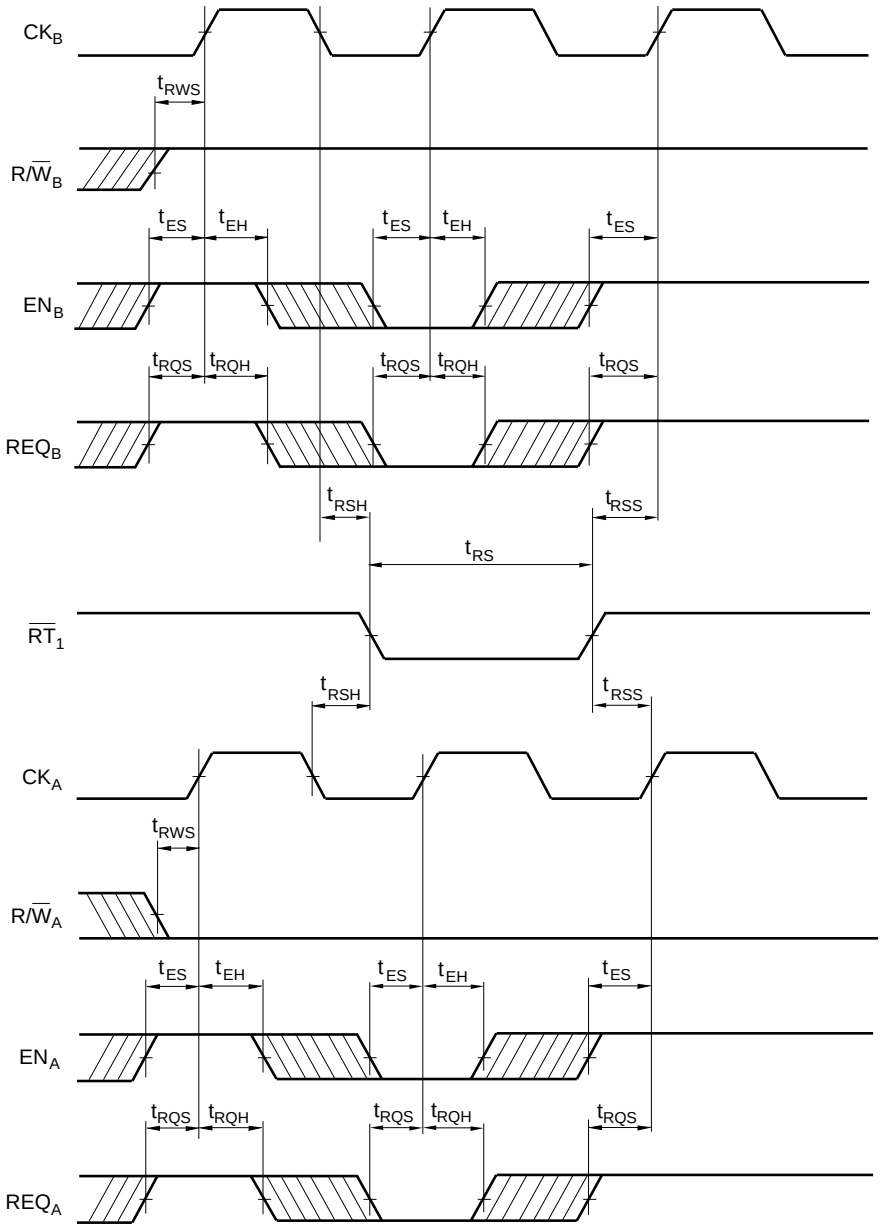
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.
4. Read and write operations to FIFO #2 should be disabled while $\overline{RT}_2$ is being asserted.

543601-20

Figure 20. FIFO #2 Retransmit

TIMING DIAGRAMS (cont'd)



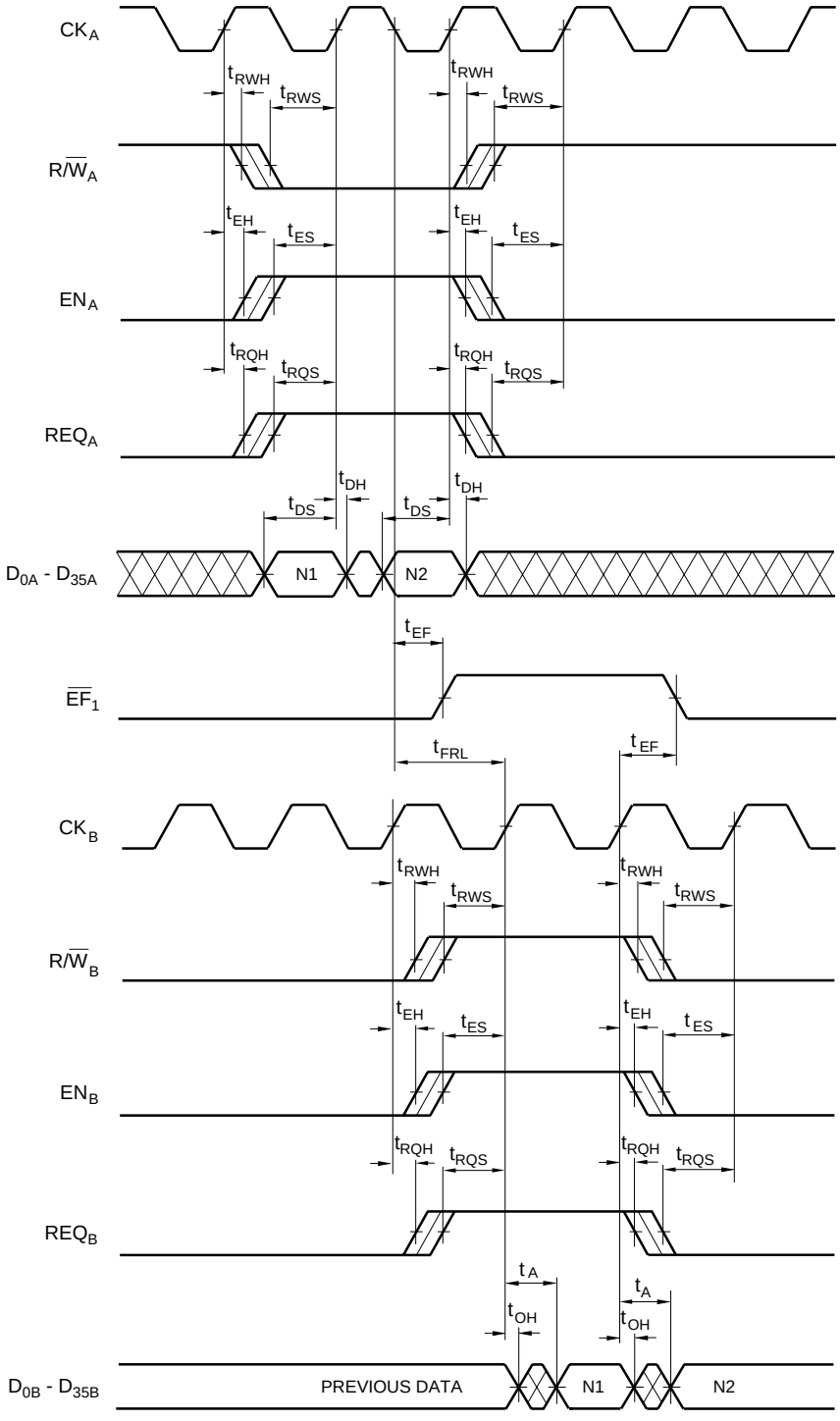
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.
4. Read and write operations to FIFO #1 should be disabled while $\overline{RT}_1$ is being asserted.

543601-21

Figure 21. FIFO #1 Retransmit

TIMING DIAGRAMS (cont'd)



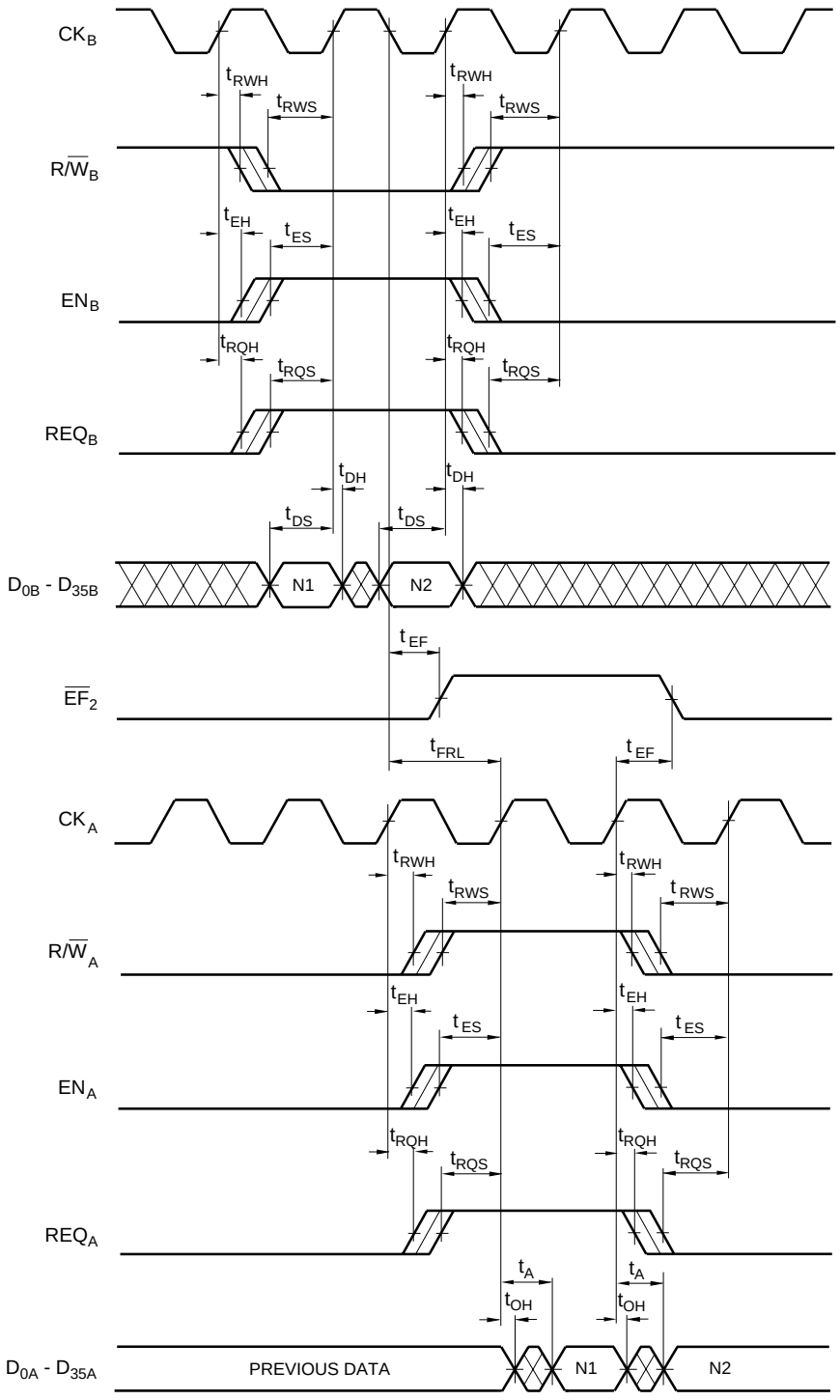
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

543601-16

Figure 22. FIFO #1 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



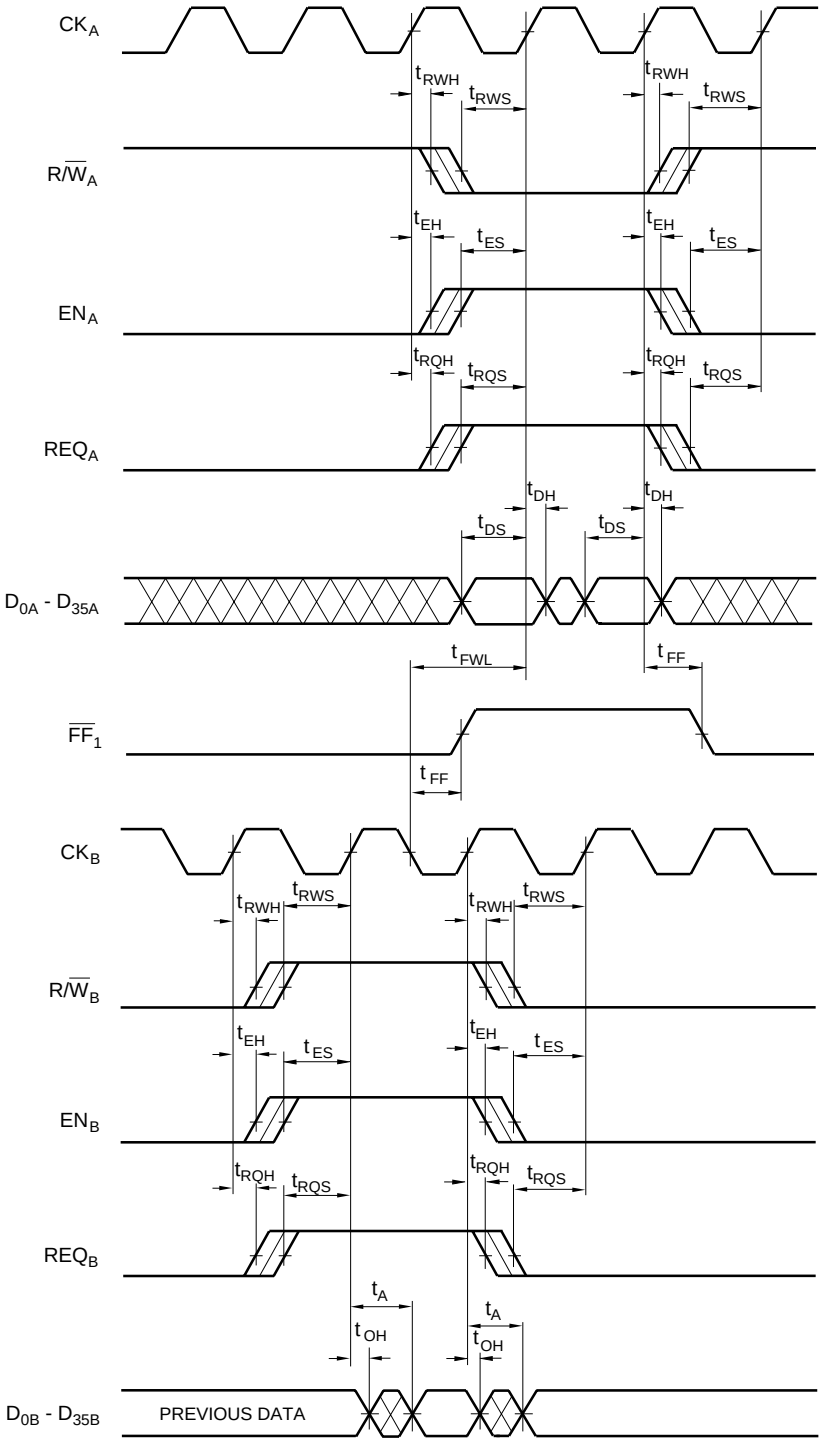
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. $\overline{OE}_A$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

543601-17

Figure 23. FIFO #2 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



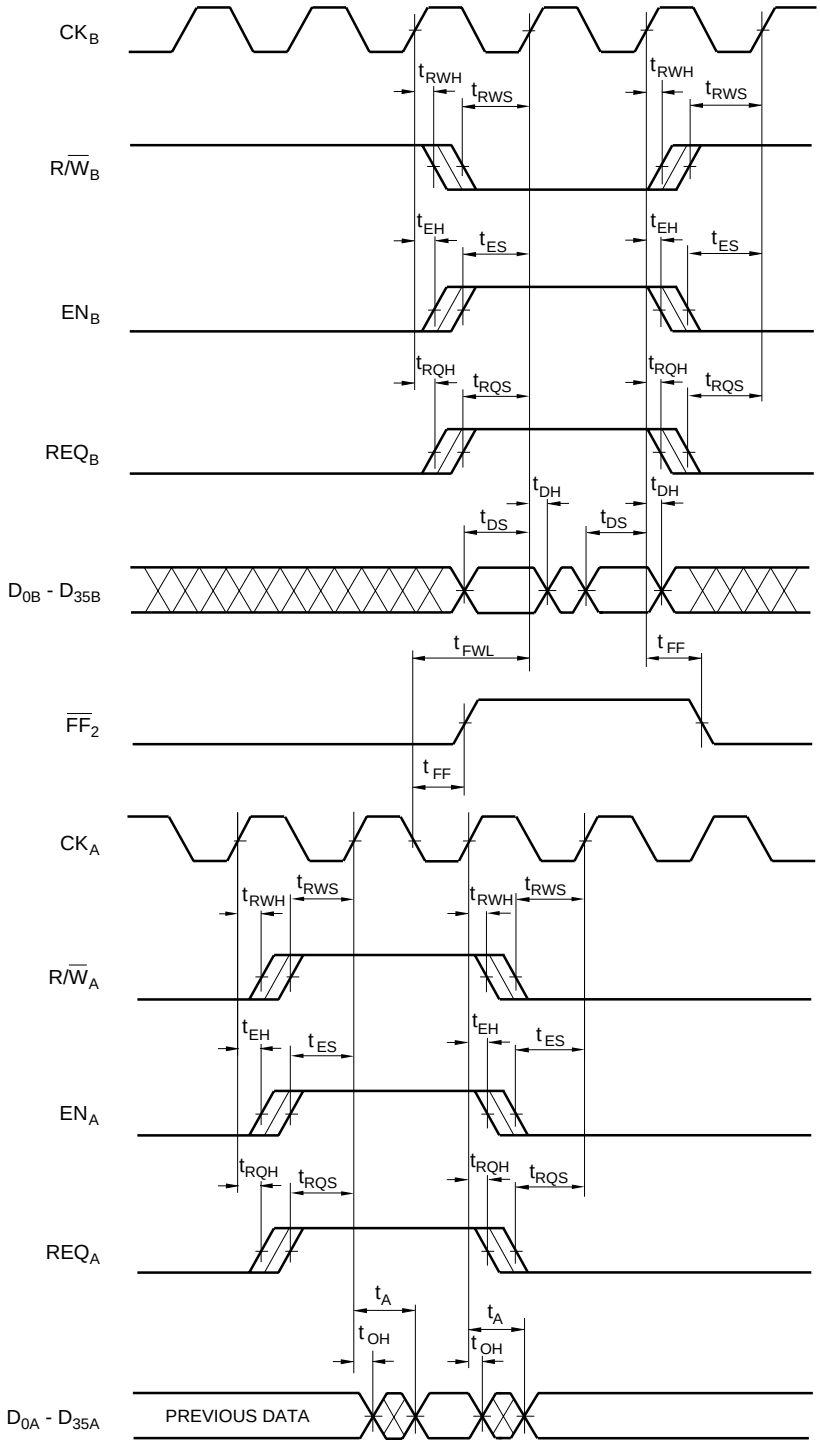
NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. $\underline{A_{0B}}$ is held HIGH for FIFO access at Port B.
2. $\underline{OE_A}$ is held HIGH.
3. $\overline{OE_B}$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

543601-14

Figure 24. FIFO #1 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



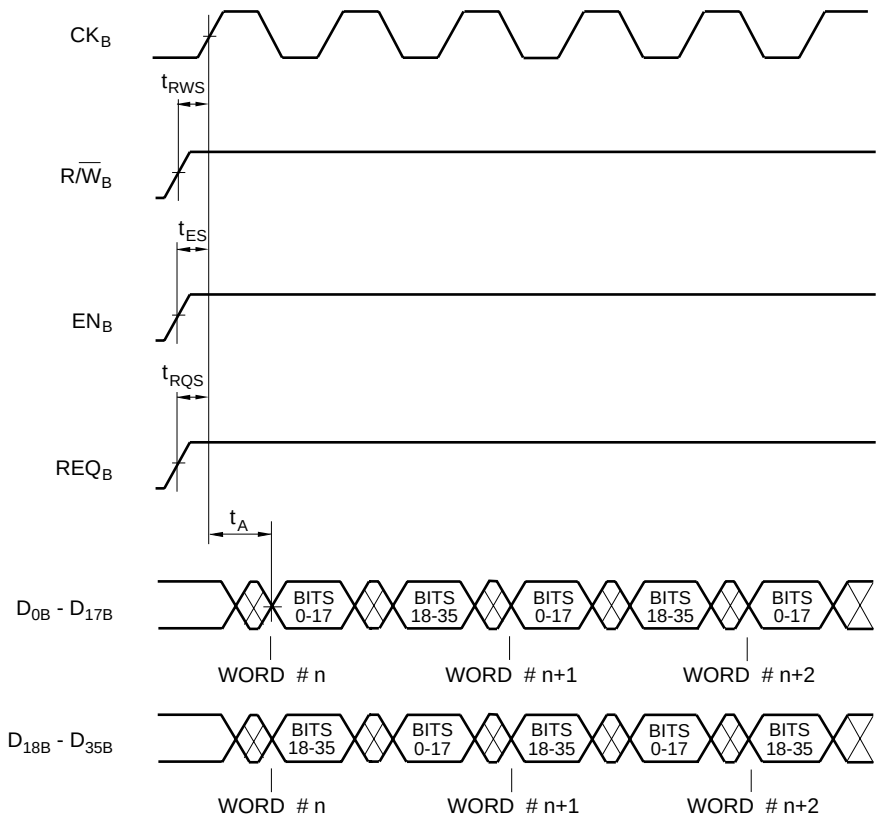
NOTES:

1. A_{2A}, A_{1A}, and A_{0A} all are held HIGH for FIFO access at Port A. A_{0B} is held HIGH for FIFO access at Port B.
2. $\overline{OE}_B$ is held HIGH.
3. $\overline{OE}_A$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

543601-15

Figure 25. FIFO #2 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



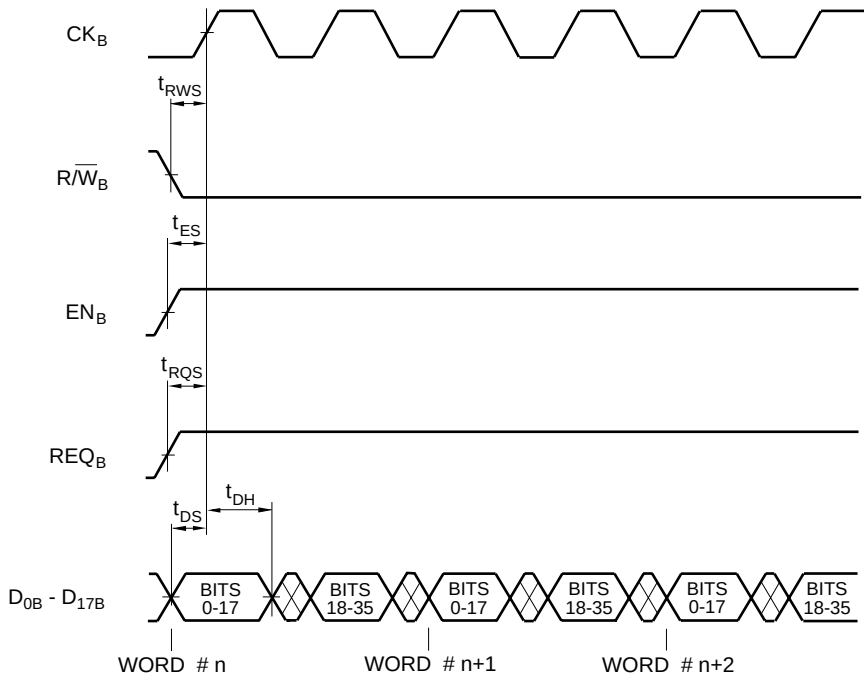
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.
4. Data-access time t_A, after the rising edge of CK_B, shown for the first read cycle, applies similarly for all subsequent read cycles.

543601-13

Figure 26. Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

TIMING DIAGRAMS (cont'd)



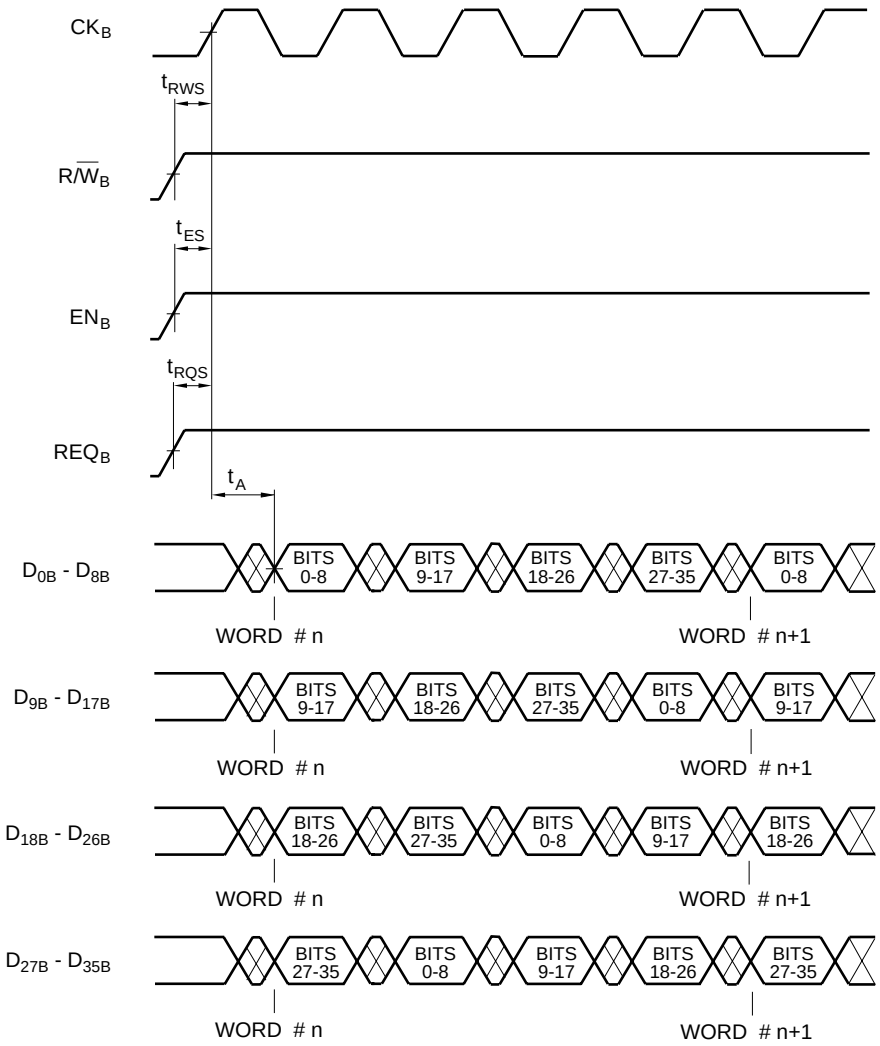
NOTES:

1. $\underline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.
4. Data-setup time t_{DS} and data-hold time t_{DH}, before and after the rising edge of CK_B, shown for the first write cycle, apply similarly for all subsequent write cycles.

543601-12

Figure 27. Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

TIMING DIAGRAMS (cont'd)



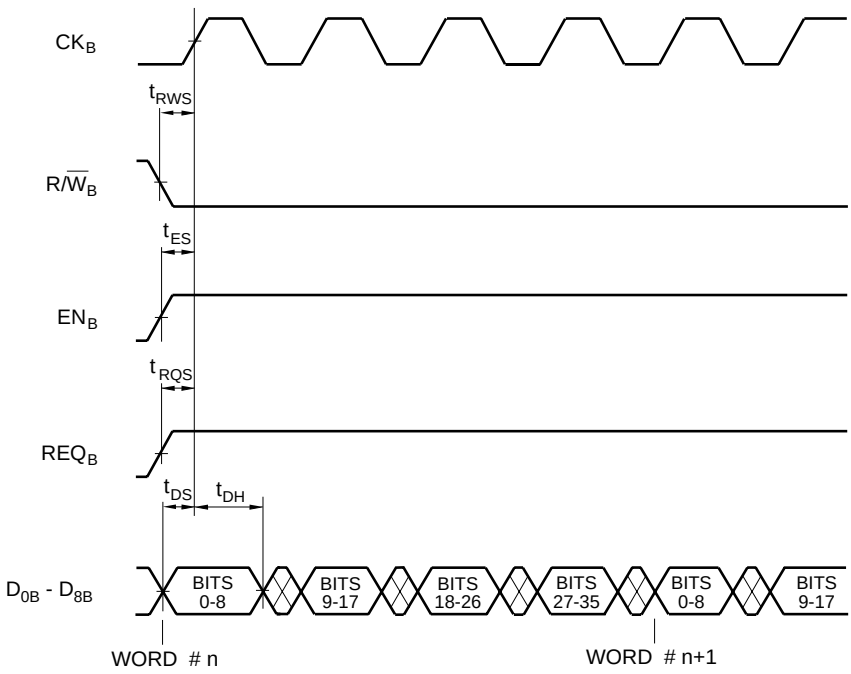
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 and WS_1 both are held LOW for single-byte access.
4. Data-access time t_A, after the rising edge of CK_B, shown for the first read cycle, applies similarly for all subsequent read cycles.

543601-11

Figure 28. Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

TIMING DIAGRAMS (cont'd)



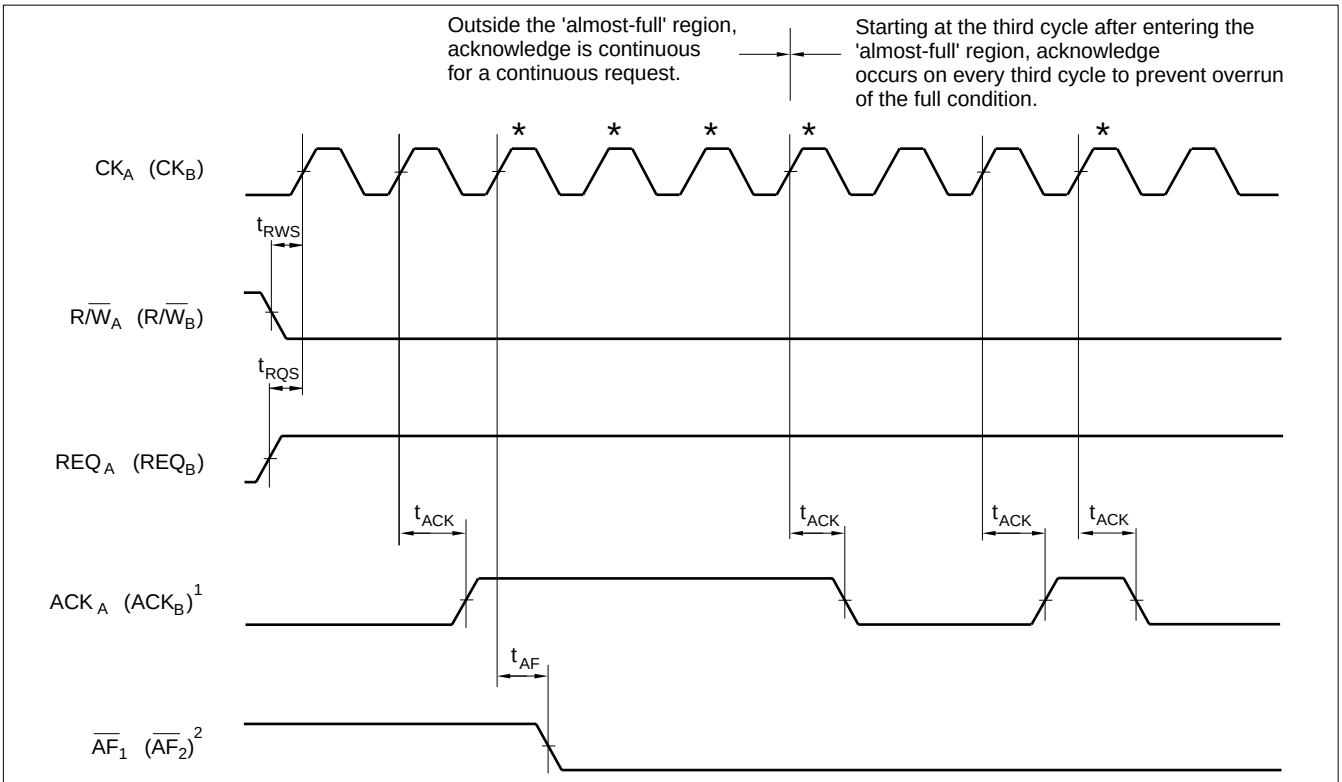
NOTES:

1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.
4. Data-setup time t_{DS} and data-hold time t_{DH}, before and after the rising edge of CK_B, shown for the first write cycle, apply similarly for all subsequent write cycles.

543601-10

Figure 29. Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

TIMING DIAGRAMS (cont'd)



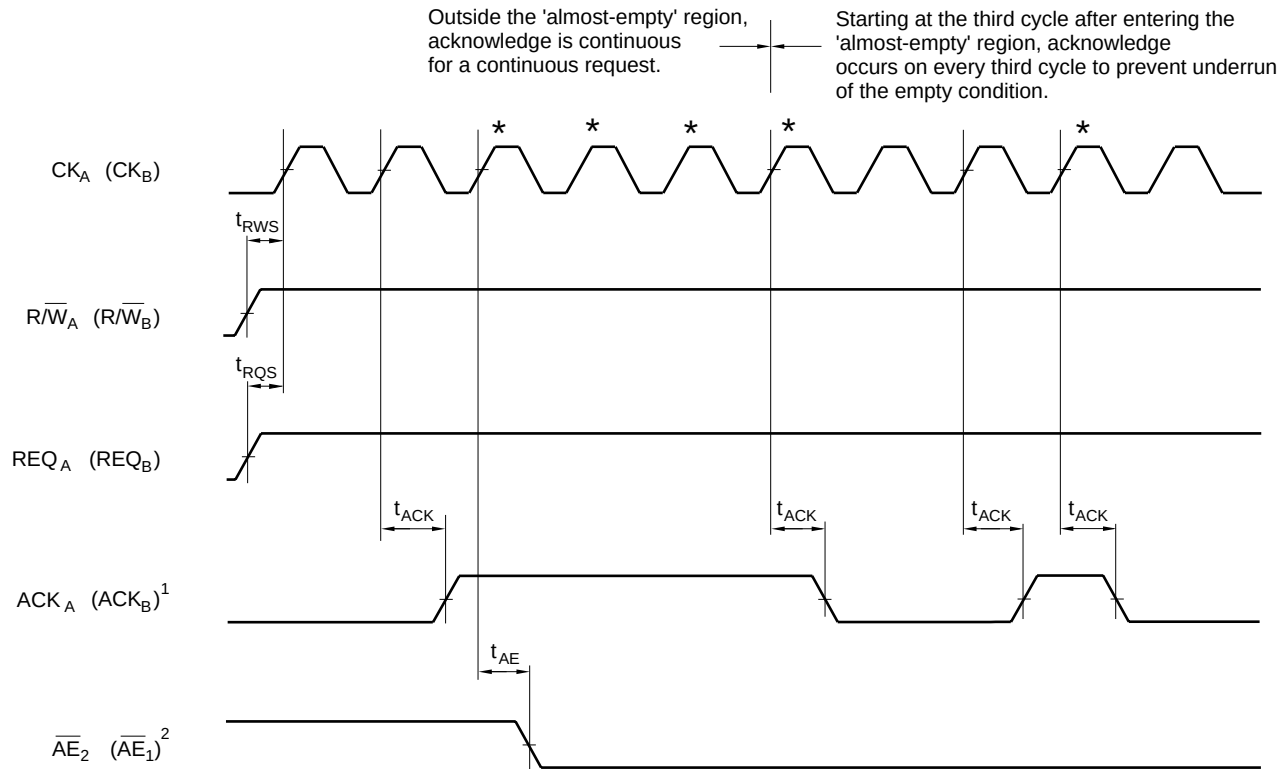
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to Port A. Parameters with parentheses apply to Port B.

543601-8

Figure 30. Write Request/Acknowledge Handshake

TIMING DIAGRAMS (cont'd)



NOTES:

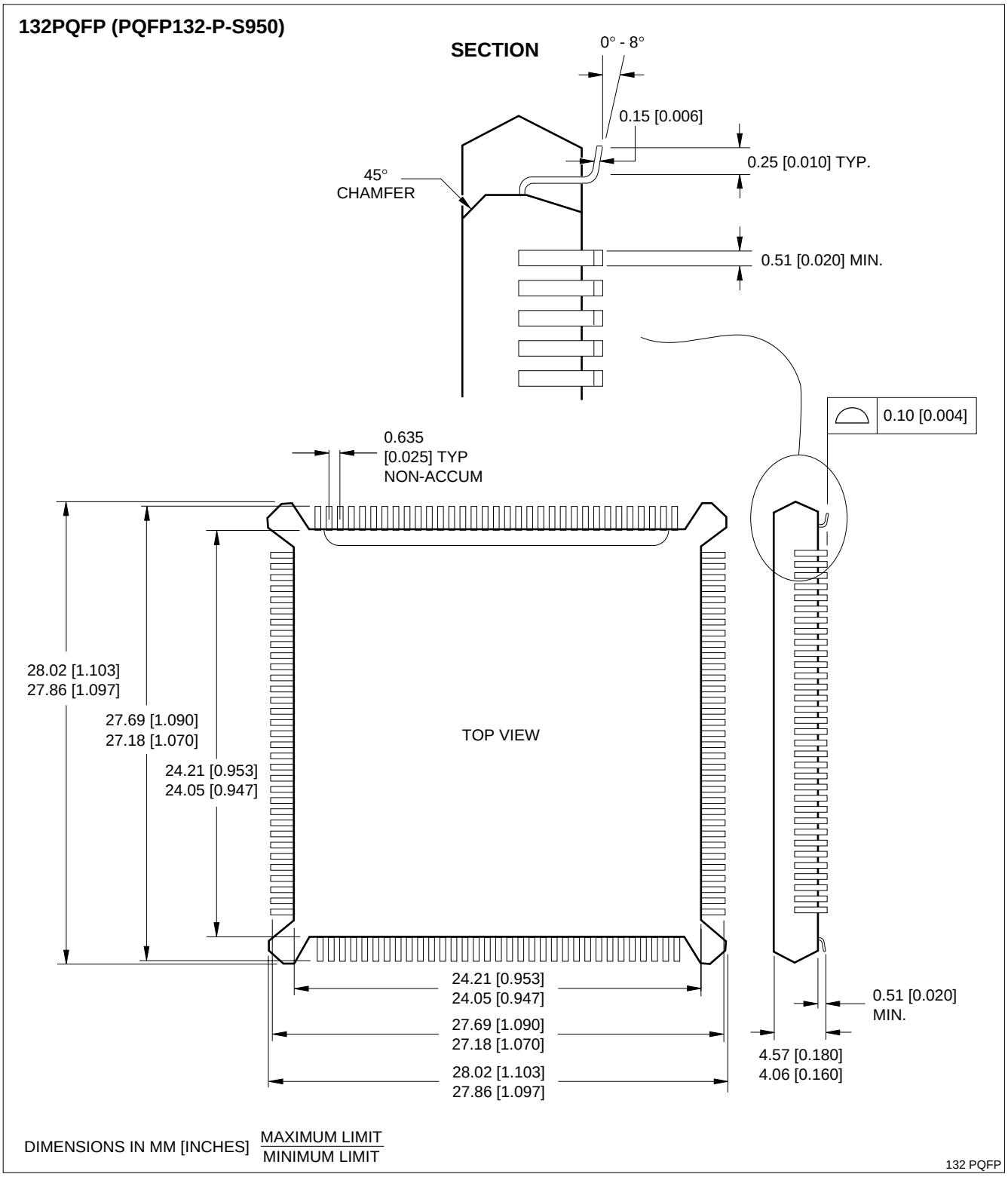
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.
5. Parameters without parentheses apply to Port A. Parameters with parentheses apply to Port B.

543601-9

Figure 31. Read Request/Acknowledge Handshake

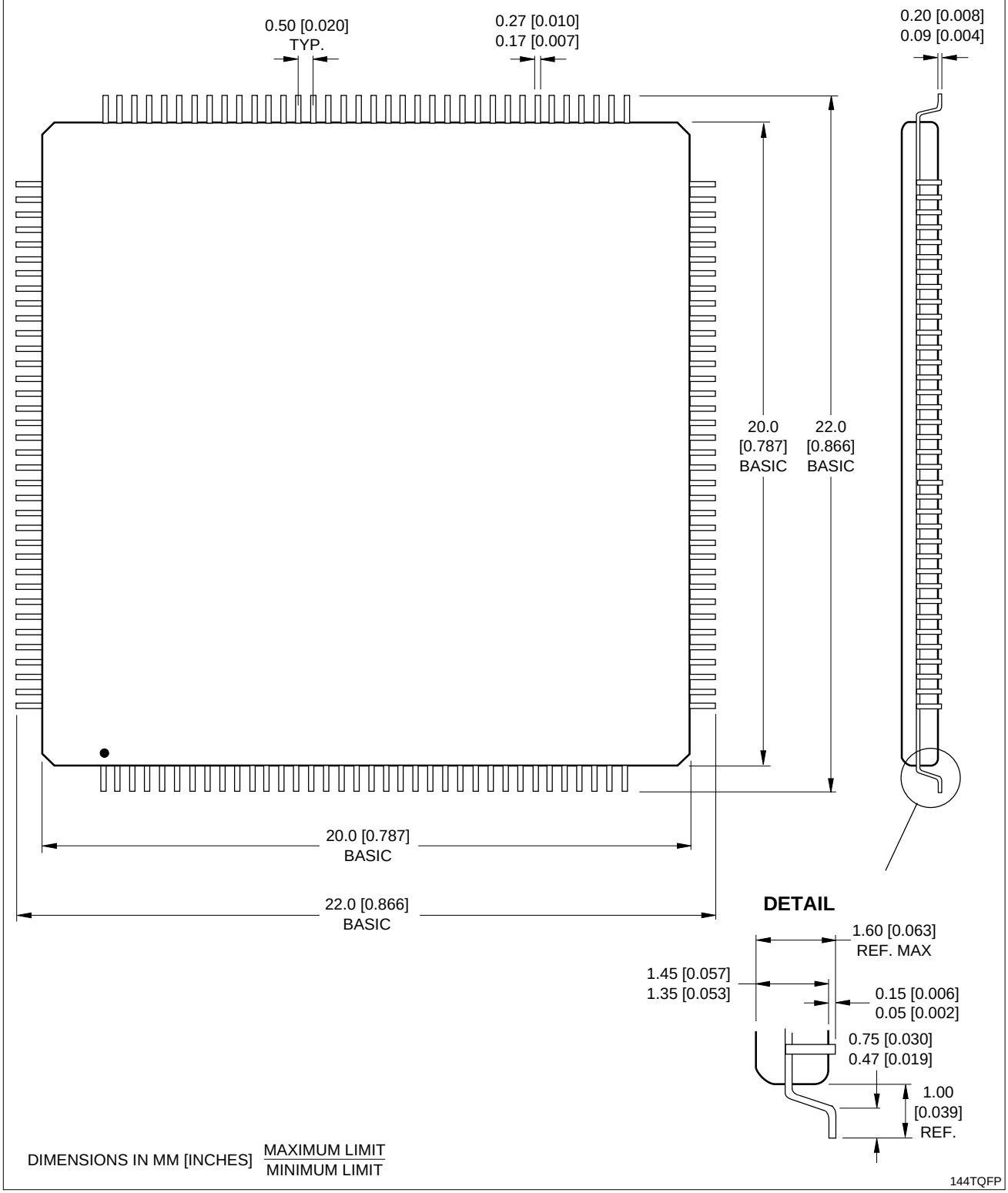
PACKAGE DIAGRAMS

132PQFP (PQFP132-P-S950)



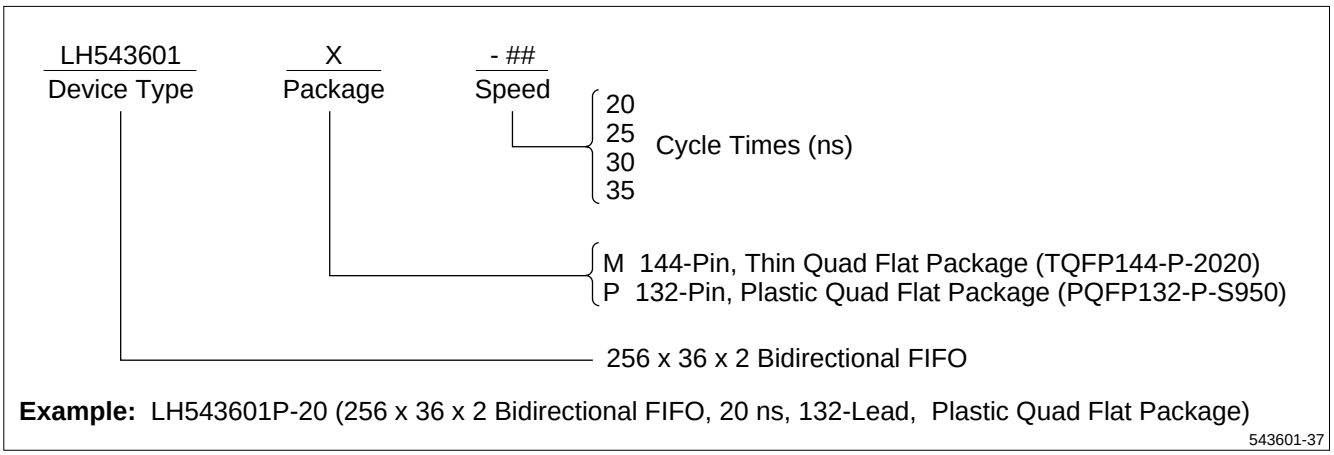
132-pin PQFP

144TQFP (TQFP-144-P-2020)



144-pin TQFP

ORDERING INFORMATION



Example: LH543601P-20 (256 x 36 x 2 Bidirectional FIFO, 20 ns, 132-Lead, Plastic Quad Flat Package)

543601-37