SHARP®

Integrated Circuits Group

APPLICATIONS:
- PDA
- Printer

LH53BV64R00N
64M MROM

FEATURES

- Memory organization
  - 4,194,304 × 16-bit (Word mode: $\overline{W}$ = V_{IL})
  - 2,097,152 × 32-bit (Double word mode: $\overline{W}$ = V_{IH})
- Supply voltage 3.3 V to ±0.3 V
- Static operation
- Three-state output
- Access time 120 ns (MAX.), 50 ns (MAX.) in page mode
- Addressable page: 4 double words or 8 words
- 70-pin SSOP
- Operating current 120 mA (MAX.)
- Standby current 150 µA (MAX.)
- Not programmable
- Not designed or rated as radiation hardened
- CMOS process (P-type silicon substrate)

DESCRIPTION

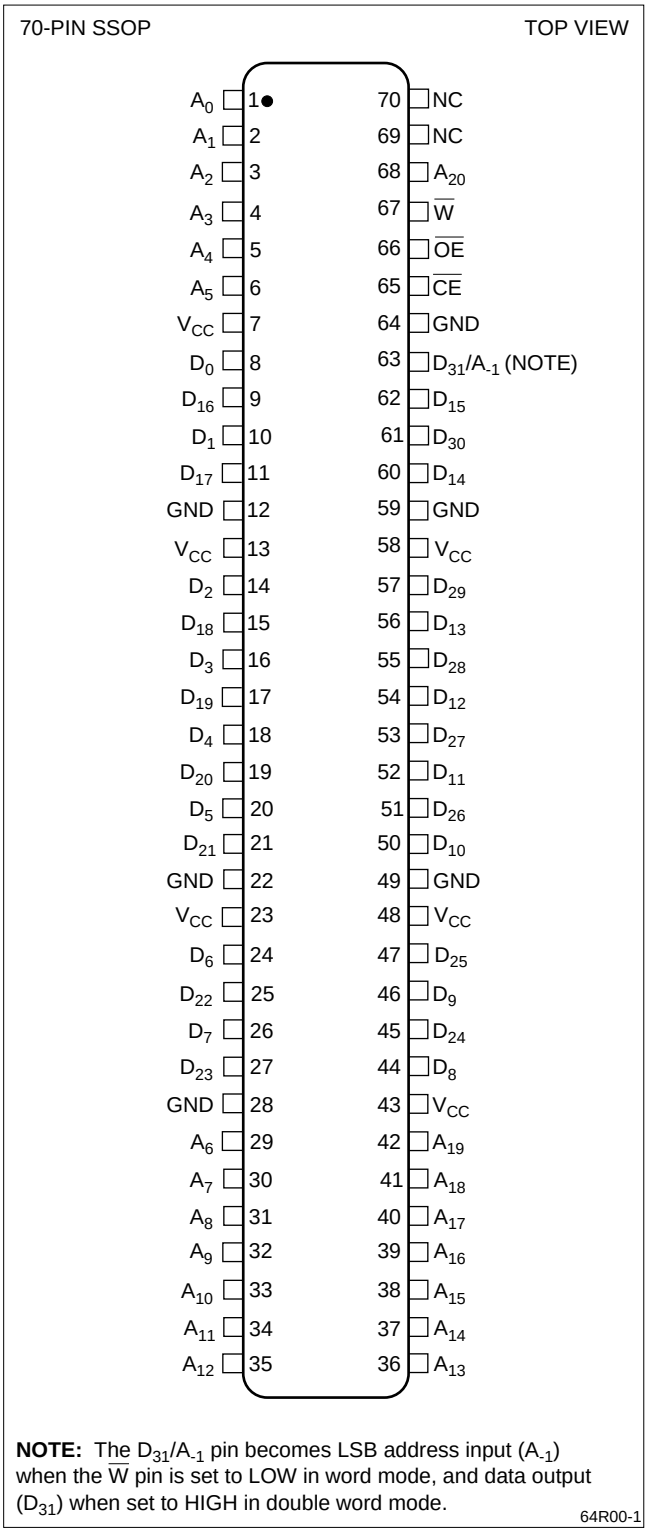
The SHARP LH53BV64R00N is a 64M CMOS mask ROM (mask-programmable read-only memory), producted by the silicon gate CMOS process.

PIN DESCRIPTION

PIN	DESCRIPTION
A_{-1} to A_1	Address Input (Page Mode Operation)
A_2 to A_{20}	Address Input
D_0 to D_{31}	Data Output
$\overline{W}$	× 16-bit/× 32bit Mode Select Input*
$\overline{CE}$	Chip Enable Input*
$\overline{OE}$	Output Enable Input*
V_{CC}	Power Pin (+3.3 V)
GND	Ground
NC	Non Connection

NOTE: *D_{31}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{W}$ pin is set to be low in word mode, and data output (D_{31}) when set to be high in double word mode.

70-PIN SSOP PINOUT



NOTE: The D_{31}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{W}$ pin is set to LOW in word mode, and data output (D_{31}) when set to HIGH in double word mode.

64R00-1

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