

LH5324P00A

PRELIMINARY

CMOS 24M ($3\text{M} \times 8/1.5\text{M} \times 16$)
Mask-Programmable ROM

FEATURES

- 3,145,728 words $\times$ 8 bit organization (Byte mode)
1,572,864 words $\times$ 16 bit organization (Word mode)
- Access time: 120 ns (MAX.)
- Power consumption:
Operating: 440 mW (MAX.)
Standby: 1650 μ W (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Package: 44-pin, 600-mil SOP

DESCRIPTION

The LH5324P00A is a 24M-bit mask-programmable ROM organized as $3,145,728 \times 8$ bits (Byte mode) or $1,572,864 \times 16$ bits (Word mode) that can be selected by a $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

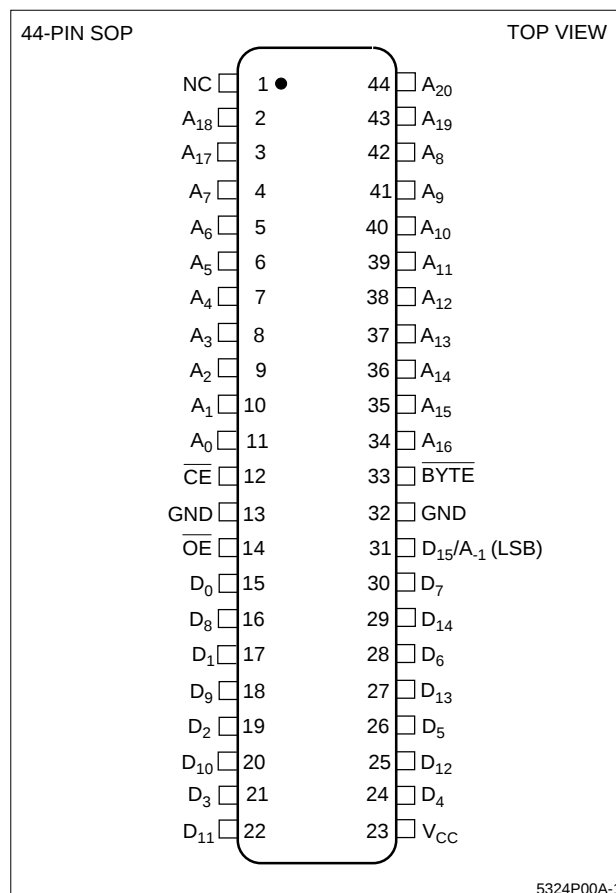


Figure 1. Pin Connections for SOP Package

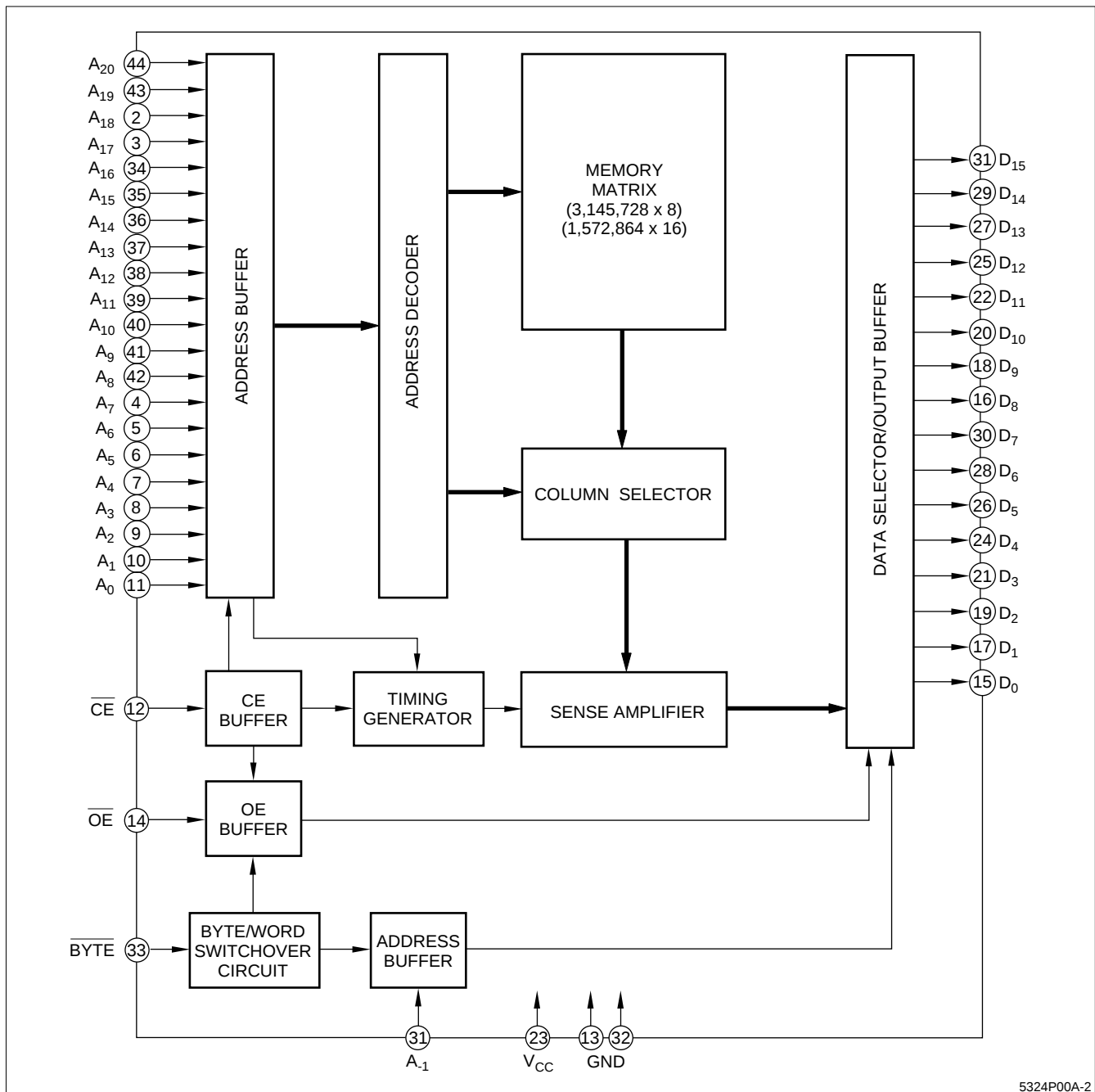


Figure 2. LH5324P00A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A ₁ – A ₂₀	Address input	1
D ₀ – D ₁₅	Data output	1
BYTE	Byte/word mode switch	1
CE	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{\text{OE}}$	Output Enable input	
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	No connection	

NOTE:

1. The D₁₅/A₋₁ pin becomes LSB address input (A₋₁) when the $\overline{\text{BYTE}}$ pin is set to be LOW in byte mode, and data output (D₁₅) when set to be HIGH in word mode.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT	NOTE
				$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB		
H	X	X	X	High-Z	High-Z	—	—	Standby (I_{SB})	1
L	H	X	X	High-Z	High-Z	—	—	Operating (I_{CC})	1
L	L	H	—	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{20}	Operating (I_{CC})	
L	L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{20}	Operating (I_{CC})	
L	L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{20}	Operating (I_{CC})	

NOTE:

1. X = H or L; High-Z = High-impedance

When the address inputs become 'High' to both A_{19} and A_{20} , the data outputs become 'Unspecified' since the data does not exist in this address area.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to $V_{CC} + 0.3$	V
Output voltage	V_{OUT}	−0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		2.2	$V_{CC} + 0.3$	V	
Input 'Low' voltage	V_{IL}		−0.3	0.8	V	
Output 'High' voltage	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4		V	
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\ \text{mA}$		0.4	V	
Input leakage current	$ I_{LI} $	$V_{IN} = 0\text{ V to }V_{CC}$		10	μA	
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\text{ V to }V_{CC}$		10	μA	1
Operating current	I_{CC1}	$t_{RC} = 150\ \text{ns}$		80	mA	2
	I_{CC2}	$t_{RC} = 1\ \mu\text{s}$		70		
Standby current	I_{SB1}	$\overline{CE} = V_{IH}$		3	mA	
	I_{SB2}	$\overline{CE} = V_{CC} - 0.2\text{ V}$		300		
Input capacitance	C_{IN}	$f = 1\ \text{MHz}$		10	pF	
Output capacitance	C_{OUT}	$T_A = 25^{\circ}\text{C}$		10		

NOTES:

1. $\overline{CE}/\overline{OE} = V_{IH}$
 2. $V_{IN} = V_{IH}$ or V_{IL} , $\overline{CE} = V_{IL}$, outputs open

AC CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		ns	
Address access time	t_{AA}		120	ns	
Chip enable access time	t_{ACE}		120	ns	
Output enable delay time	t_{OE}		60	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		50	ns	1
OE to output in High-Z	t_{OHZ}		50	ns	

NOTE:

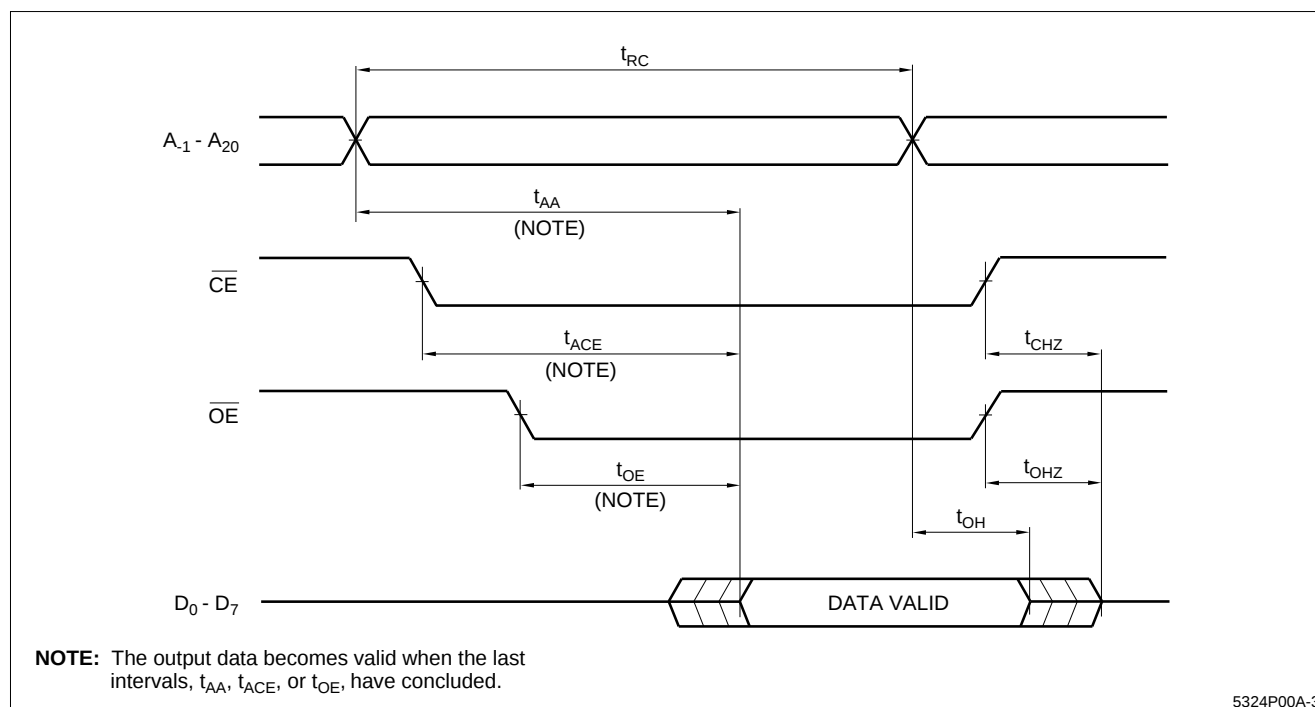
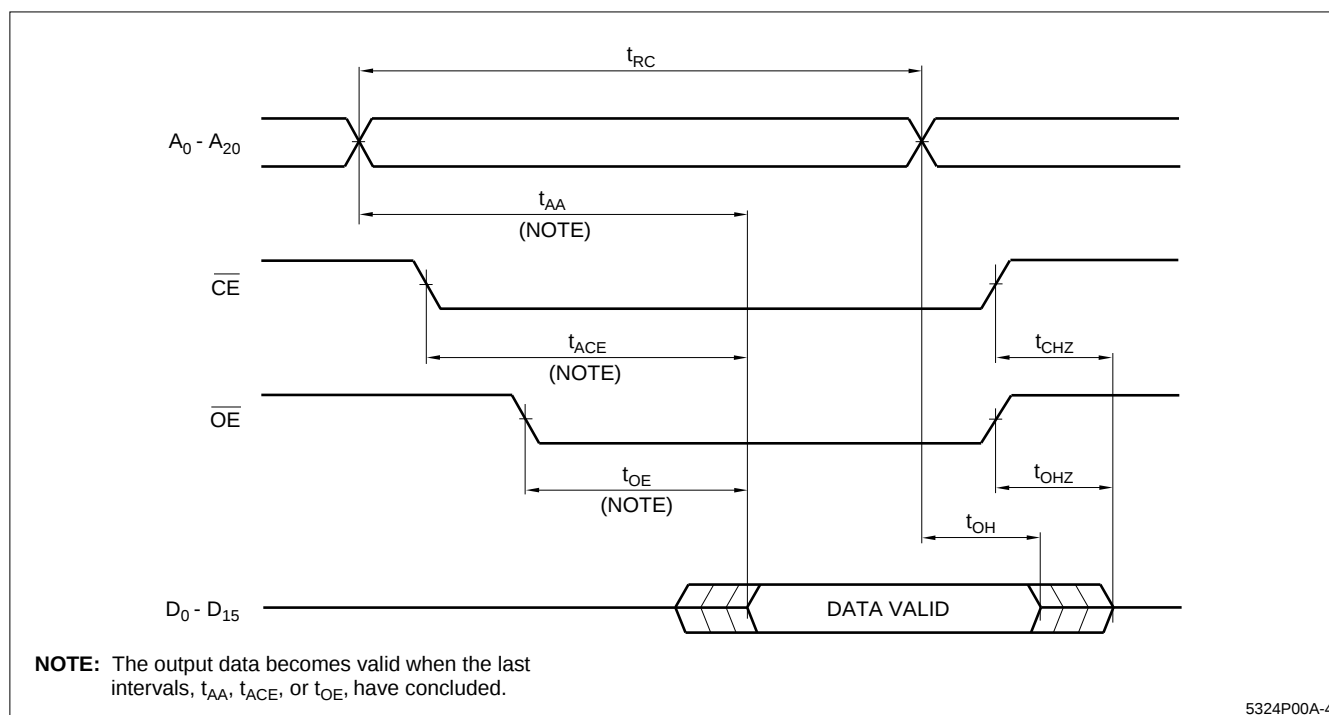
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

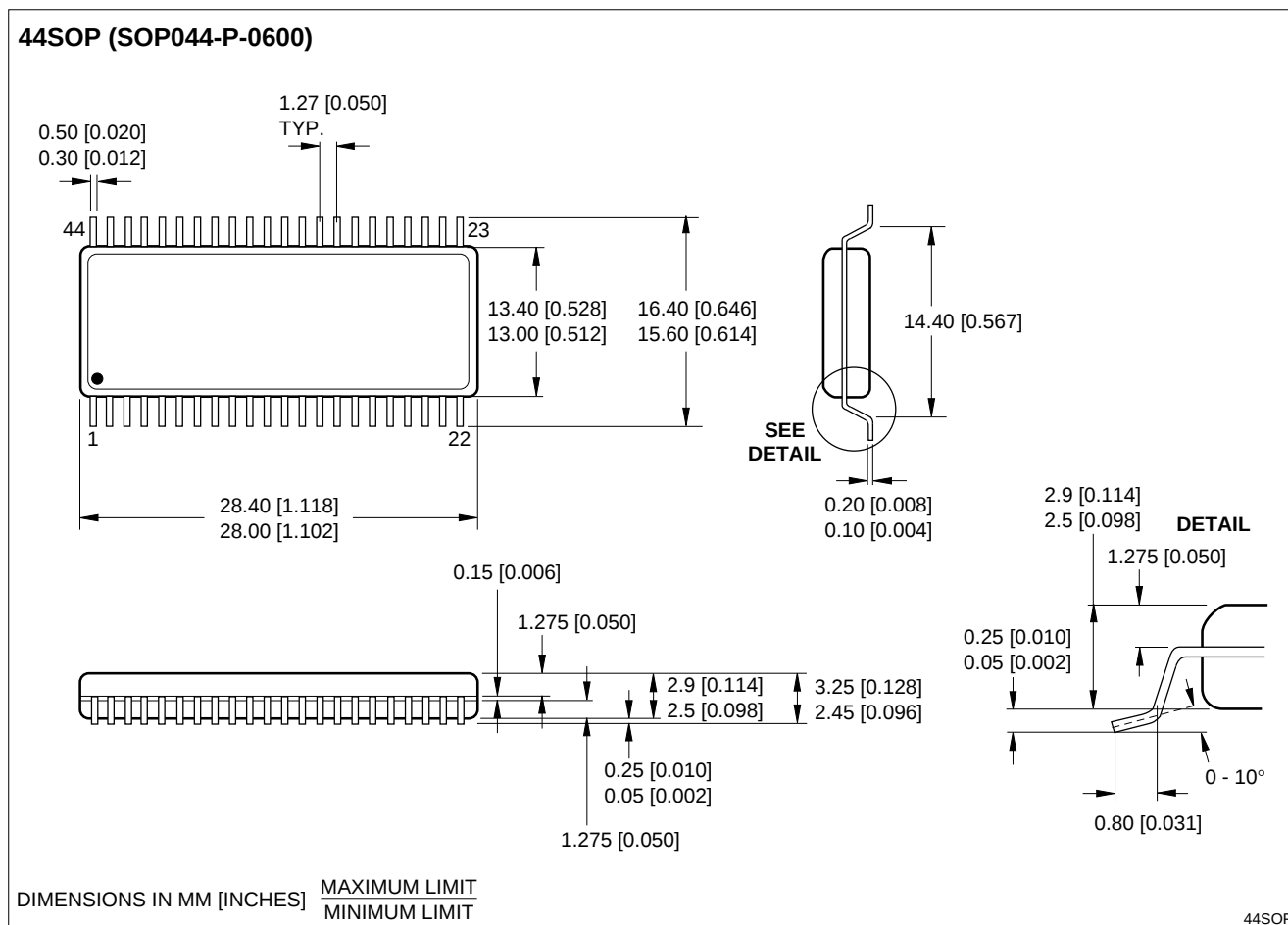
PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

Figure 3. Byte Mode ($\overline{\text{BYTE}} = V_{IL}$)Figure 4. Word Mode ($\overline{\text{BYTE}} = V_{IH}$)

PACKAGE DIAGRAM



44-pin, 600-mil SOP

ORDERING INFORMATION

LH5324P00A
Device Type

N
Package

44-pin, 600-mil SOP (SOP044-P-0600)

CMOS 24M (3M x 8 or 1.5M x 16) Mask-Programmable ROM

Example: LH5324P00AN (CMOS 24M (3M x 8 or 1.5M x 16) Mask-Programmable ROM, 44-pin, 600-mil SOP)

5324P00A-5