LH532000B

CMOS 2M (256K $\times$ 8/128K $\times$ 16) MROM

FEATURES

- 262,144 words $\times$ 8 bit organization
    (Byte mode)
    131,072 words $\times$ 16 bit organization
    (Word mode)

- $\overline{\text{BYTE}}$ input pin selects bit configuration

- Access times: 120/150 ns (MAX.)

- Low-power consumption:
    Operating: 275 mW (MAX.)
    Standby: 550 μW (MAX.)

- Programmable OE/$\overline{\text{OE}}$ and OE$_1$/$\overline{\text{OE}_1}$/DC

- Static operation

- TTL compatible I/O

- Three-state outputs

- Single +5 V power supply

- Packages:
    40-pin, 600-mil DIP
    40-pin, 525-mil SOP
    48-pin, 12 $\times$ 18 mm^2 TSOP (Type I)

- $\times$16 word-wide pinout

DESCRIPTION

  The LH532000B is a 2M-bit mask-programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

40-PIN DIP
40-PIN SOP
TOP VIEW

Pin	Signal		Pin	Signal
1	OE$_1$/$\overline{\text{OE}_1}$/DC		40	A$_8$
2	A$_7$		39	A$_9$
3	A$_6$		48	A$_{10}$
4	A$_5$		37	A$_{11}$
5	A$_4$		36	A$_{12}$
6	A$_3$		35	A$_{13}$
7	A$_2$		34	A$_{14}$
8	A$_1$		33	A$_{15}$
9	A$_0$		32	A$_{16}$
10	$\overline{\text{CE}}$		31	$\overline{\text{BYTE}}$
11	GND		30	GND
12	OE/$\overline{\text{OE}}$		29	D$_{15}$/A$_{-1}$ (LSB)
13	D$_0$		28	D$_7$
14	D$_8$		27	D$_{14}$
15	D$_1$		26	D$_6$
16	D$_9$		25	D$_{13}$
17	D$_2$		24	D$_5$
18	D$_{10}$		23	D$_{12}$
19	D$_3$		22	D$_4$
20	D$_{11}$		21	V$_{CC}$
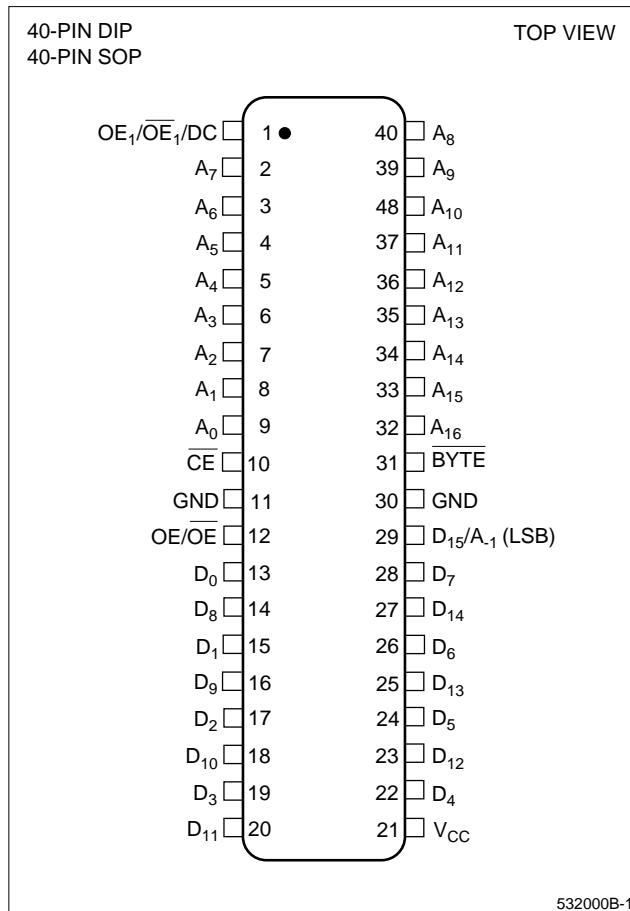
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Figure 1. Pin Connections for DIP and SOP Packages

48-PIN TSOP (Type I)   TOP VIEW

$\overline{BYTE}$	1 ●		48	GND
A_{16}	2		47	GND
A_{15}	3		46	D_{15}/A_{-1}
A_{14}	4		45	D_7
A_{13}	5		44	D_{14}
A_{12}	6		43	D_6
A_{11}	7		42	D_{13}
A_{10}	8		41	D_5
A_9	9		40	D_{12}
A_8	10		39	D_4
NC	11		38	V_{CC}
GND	12		37	V_{CC}
NC	13		36	GND
NC	14		35	D_{11}
$OE_1/\overline{OE}_1/DC$	15		34	D_3
A_7	16		33	D_{10}
A_6	17		32	D_2
A_5	18		31	D_9
A_4	19		30	D_1
A_3	20		29	D_8
A_2	21		28	D_0
A_1	22		27	$OE/\overline{OE}$
A_0	23		26	GND
$\overline{CE}$	24		25	GND

NOTE: Reverse bend available on request.
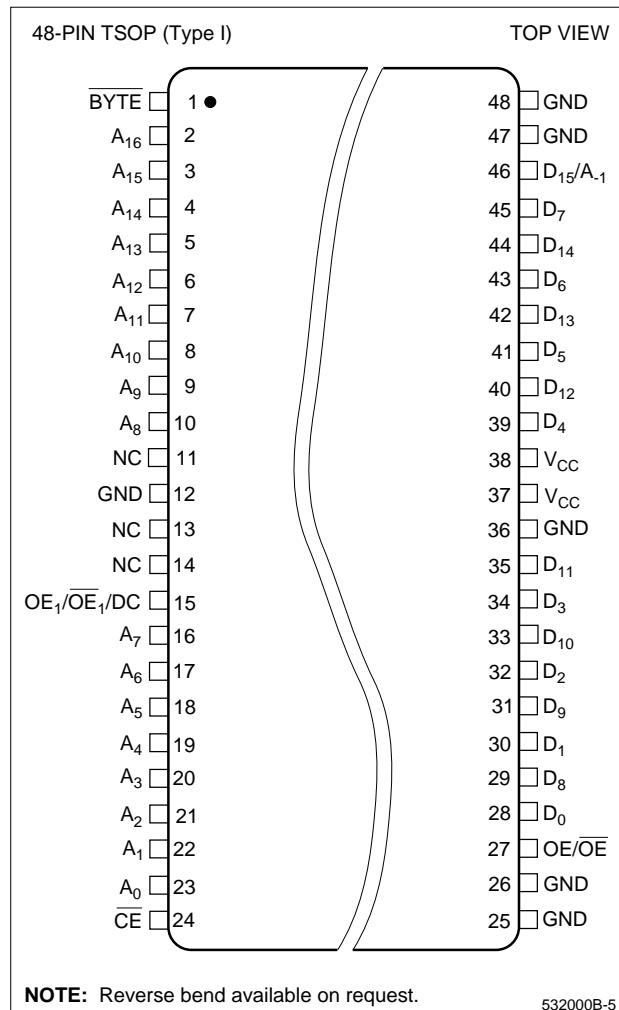
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Figure 2. Pin Connections for TSOP Package
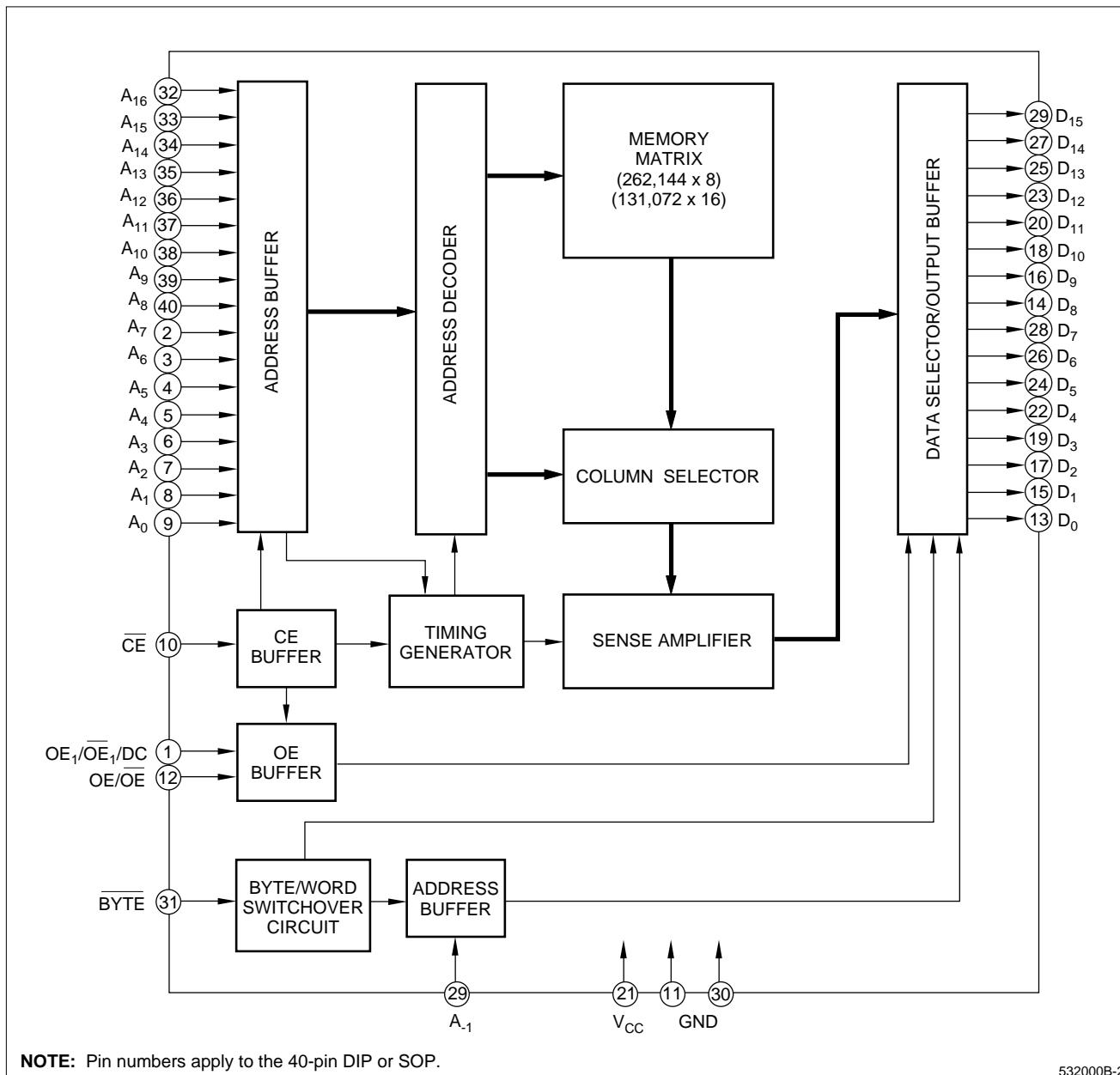
Figure 3. LH532000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
$A_0 - A_{16}$	Address input	
$D_0 - D_{15}$	Data output	1
$\overline{CE}$	Chip enable input	
$OE/\overline{OE}$	Output enable input	2

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE}_1/DC$	Output enable input or Don't care	2
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:
1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. The active levels of $OE/\overline{OE}$ and $OE_1/\overline{OE}_1/DC$ are mask-programmable.
   Selecting DC allows the outputs to be active for both high and low levels applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	OE$_1$/$\overline{OE}_1$	$\overline{BYTE}$	A$_{-1}$ (D$_{15}$)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					D$_0$ – D$_7$	D$_8$ – D$_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby (I$_{SB}$)
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating (I$_{CC}$)
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating (I$_{CC}$)
L	H/L	H/L	H	Input inhibit	D$_0$ – D$_7$	D$_8$ – D$_{15}$	A$_0$	A$_{16}$	Operating (I$_{CC}$)
L	H/L	H/L	L	L	D$_0$ – D$_7$	High-Z	A$_{-1}$	A$_{16}$	Operating (I$_{CC}$)
L	H/L	H/L	L	H	D$_8$ – D$_{15}$	High-Z	A$_{-1}$	A$_{16}$	Operating (I$_{CC}$)

NOTE:
1. X = H or L, High-Z = High-impedance.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V$_{CC}$	−0.3 to +7.0	V
Input voltage	V$_{IN}$	−0.3 to V$_{CC}$ + 0.3	V
Output voltage	V$_{OUT}$	−0.3 to V$_{CC}$ + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T$_A$ = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V$_{CC}$	4.5	5.0	5.5	V

DC CHARACTERISTICS (V$_{CC}$ = 5 V ±10%, T$_A$ = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V$_{IL}$		−0.3		0.8	V	
Input 'High' voltage	V$_{IH}$		2.2		V$_{CC}$ + 0.3	V	
Output 'Low' voltage	V$_{OL}$	I$_{OL}$ = 2.0 mA			0.4	V	
Output 'High' voltage	V$_{OH}$	I$_{OH}$ = −400 µA	2.4			V	
Input leakage current	| I$_{LI}$ |	V$_{IN}$ = 0 V to V$_{CC}$			10	µA	
Output leakage current	| I$_{LO}$ |	V$_{OUT}$ = 0 V to V$_{CC}$			10	µA	1
Operating current	I$_{CC1}$	t$_{RC}$ = t$_{RC}$ (MIN.)			50	mA	2
	I$_{CC2}$	t$_{RC}$ = 1 µs			45		
	I$_{CC3}$	t$_{RC}$ = t$_{RC}$ (MIN.)			45	mA	3
	I$_{CC4}$	t$_{RC}$ = 1 µs			40		
Standby current	I$_{SB1}$	$\overline{CE}$ = V$_{IH}$			3	mA	
	I$_{SB2}$	$\overline{CE}$ = V$_{CC}$ - 0.2 V			100	µA	
Input capacitance	C$_{IN}$	f = 1 MHz			10	pF	
Output capacitance	C$_{OUT}$	T$_A$ = 25°C			10	pF	

NOTES:
1. OE/OE$_1$= V$_{IL}$, $\overline{CE}$/$\overline{OE}$/$\overline{OE}_1$= V$_{IH}$
2. V$_{IN}$ = V$_{IH}$ or V$_{IL}$, $\overline{CE}$ = V$_{IL}$, outputs open
3. V$_{IN}$ = (V$_{CC}$ - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

SHARP

AC CHARACTERISTICS (V_{CC} = 5 V $\pm$10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	120 ns		150 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		55		70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		55		70	ns	1
OE to output in High-Z	t_{OHZ}		55		70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAUTION

   To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

NOTES:
   1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address
       input, chip enable or output enable, respectively have been met.
   2. Applied to byte mode. Signals in parentheses apply to word mode.
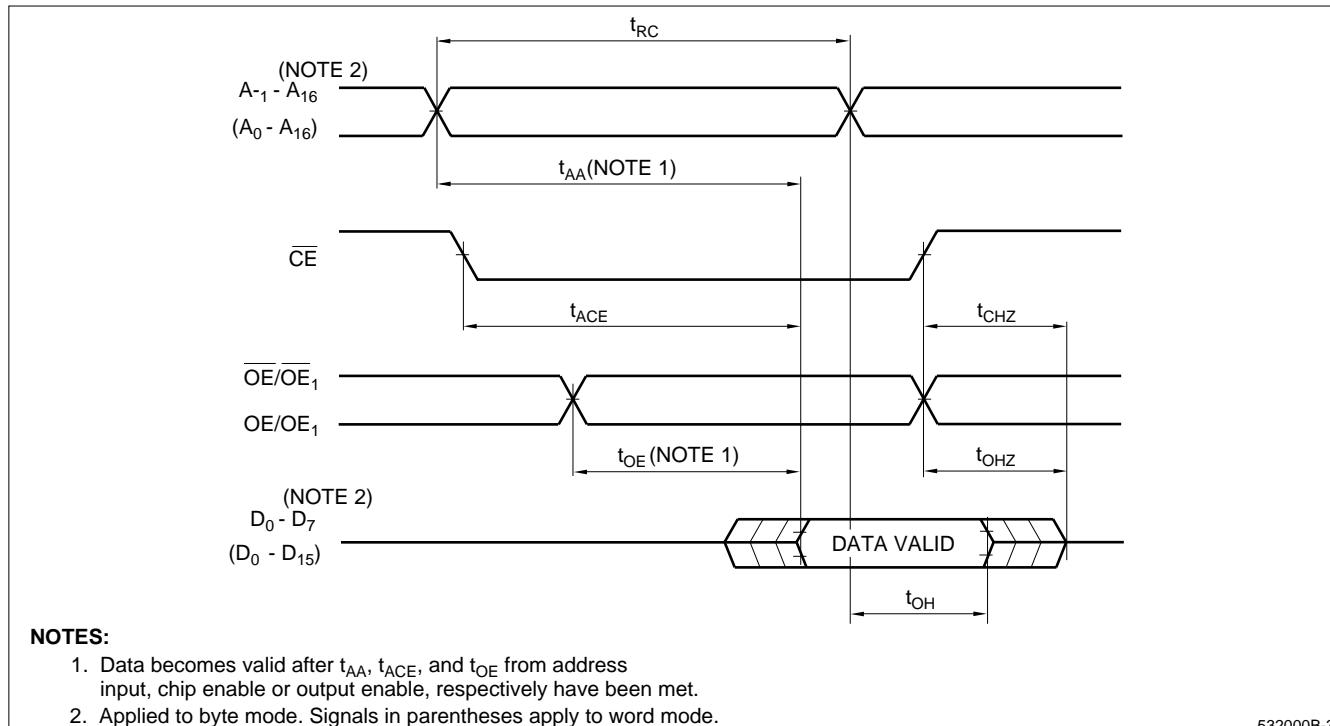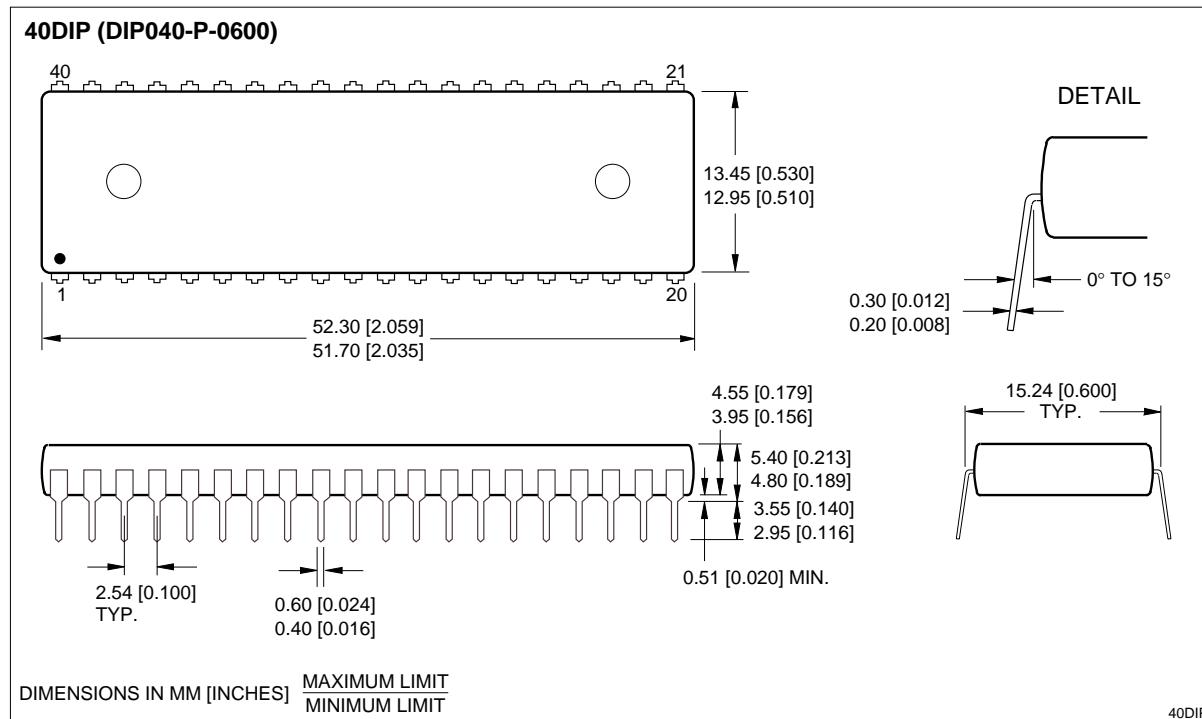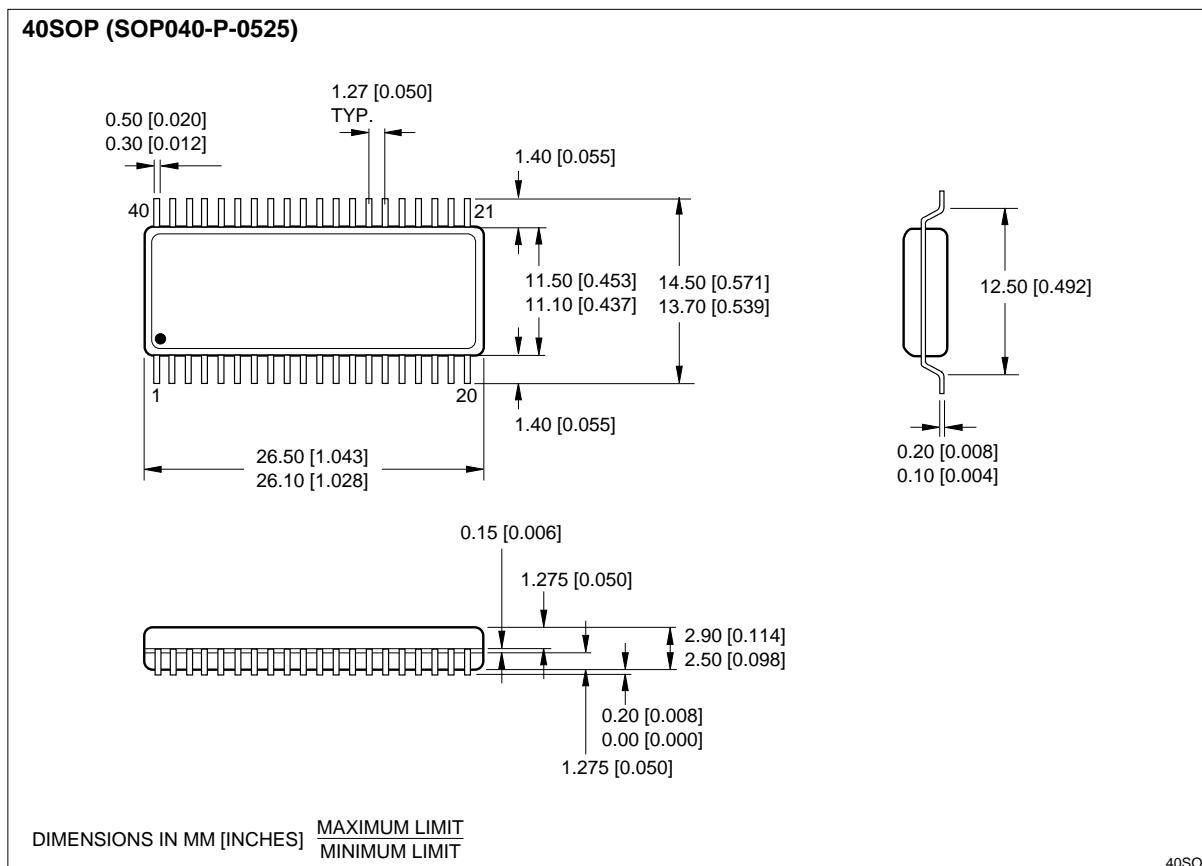
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Figure 4. Timing Diagram

PACKAGE DIAGRAMS

40DIP (DIP040-P-0600)

40   21

13.45 [0.530]
12.95 [0.510]

1   20

52.30 [2.059]
51.70 [2.035]

DETAIL

0° TO 15°

0.30 [0.012]
0.20 [0.008]

4.55 [0.179]
3.95 [0.156]

5.40 [0.213]
4.80 [0.189]

3.55 [0.140]
2.95 [0.116]

0.51 [0.020] MIN.

2.54 [0.100]
TYP.

0.60 [0.024]
0.40 [0.016]

15.24 [0.600]
TYP.

DIMENSIONS IN MM [INCHES] $\dfrac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

40DIP

40-pin, 600-mil DIP

40SOP (SOP040-P-0525)

1.27 [0.050]
TYP.

0.50 [0.020]
0.30 [0.012]

1.40 [0.055]

40   21

11.50 [0.453]   14.50 [0.571]
11.10 [0.437]   13.70 [0.539]

1   20

1.40 [0.055]

26.50 [1.043]
26.10 [1.028]

12.50 [0.492]

0.20 [0.008]
0.10 [0.004]

0.15 [0.006]

1.275 [0.050]

2.90 [0.114]
2.50 [0.098]

0.20 [0.008]
0.00 [0.000]

1.275 [0.050]

DIMENSIONS IN MM [INCHES] $\dfrac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

40SOP

40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)

0.50 [0.020] TYP.
0.30 [0.012]
0.10 [0.004]

48   25
1   24

16.60 [0.654]
16.20 [0.638]

18.40 [0.724]
17.60 [0.693]

17.00 [0.669]

12.20 [0.480]
11.80 [0.465]

0.20 [0.008]
0.10 [0.004]

0.15 [0.006]
0.425 [0.017]

1.10 [0.043]
0.90 [0.035]

1.20 [0.047] MAX.

0.425 [0.017]

0.20 [0.008]
0.00 [0.000]

DIMENSIONS IN MM [INCHES] $\dfrac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

48TSOP

48-pin, 12 $\times$ 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH532000B   X
Device Type   Package

D   40-pin, 600-mil DIP (DIP040-P-0600)
N   40-pin, 525-mil SOP (SOP040-P-0525)
T   48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
TR   48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 2M (256K x 8 or 128K x 16) Mask Programmable ROM

Example: LH532000BD (CMOS 2M (256K x 8 or 128K x 16) Mask Programmable ROM, 40-pin, 600-mil DIP)

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