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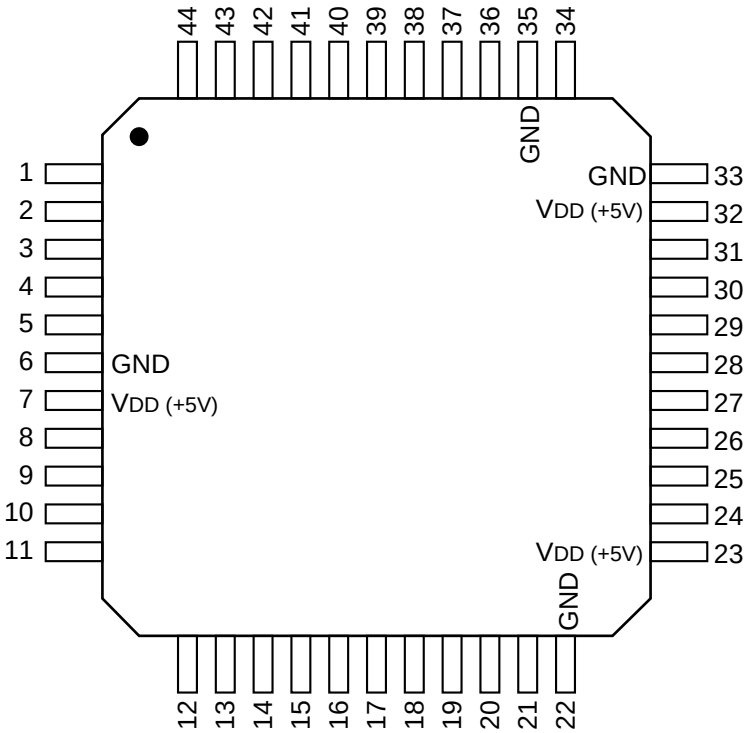
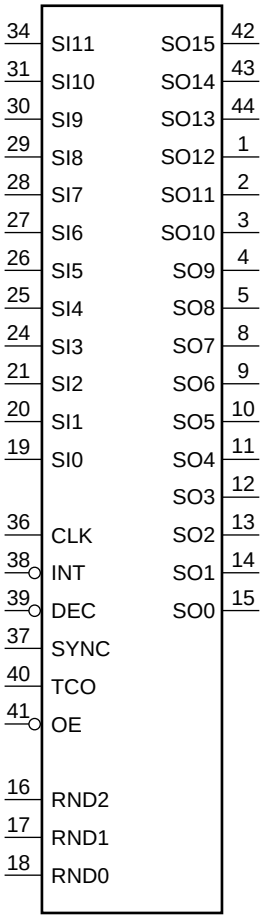
C-MOS 12 / 16-BIT HALF-BAND INTERPOLATING / DECIMATING DIGITAL FILTER

—TOP VIEW—





(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	O	SO12	12	O	SO3	23	—	VDD	34	I	SI11
2	O	SO11	13	O	SO2	24	I	SI3	35	—	GND
3	O	SO10	14	O	SO1	25	I	SI4	36	I	CLK
4	O	SO9	15	O	SO0	26	I	SI5	37	I	SYNC
5	O	SO8	16	I	RND2	27	I	SI6	38	I	$\overline{\text{INT}}$
6	—	GND	17	I	RND1	28	I	SI7	39	I	$\overline{\text{DEC}}$
7	—	VDD	18	I	RND0	29	I	SI8	40	I	TCO
8	O	SO7	19	I	SI0	30	I	SI9	41	I	$\overline{\text{OE}}$
9	O	SO6	20	I	SI1	31	I	SI10	42	O	SO15
10	O	SO5	21	I	SI2	32	—	VDD	43	O	SO14
11	O	SO4	22	—	GND	33	—	GND	44	O	SO13

INPUT

CLK ; MASTER CLOCK
$\overline{DEC}$; DECIMATION CONTROL
$\overline{INT}$; INTERPOLATION CONTROL
$\overline{OE}$; OUTPUT ENABLE
RND0-RND2 ; ROUNDING CONTROL
SI0-SI11 ; DATA INPUTS
SYNC ; SYNCHRONIZATION CONTROL
TCO ; TWO'S COMPLEMENT FORMAT CONTROL

OUTPUT

SO0-SO15 ; DATA OUTPUTS

MODE SELECTION		
$\overline{INT}$	$\overline{DEC}$	MODE
0	0	PASS-THROUGH *
0	1	INTERPOLATE
1	0	DECIMATE
1	1	PASS-THROUGH *

* Input and output registers run at full clock rate.

0 ; LOW LEVEL
1 ; HIGH LEVEL