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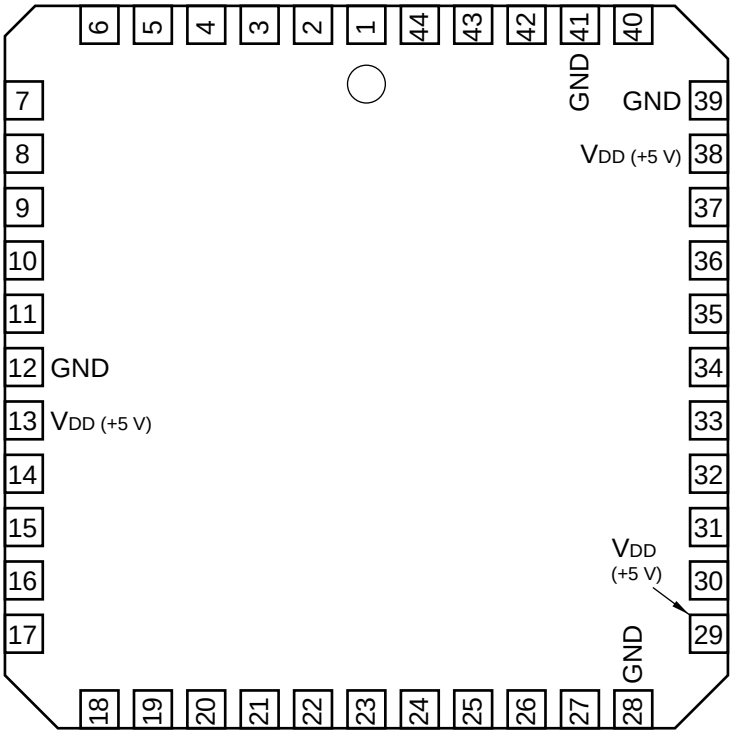
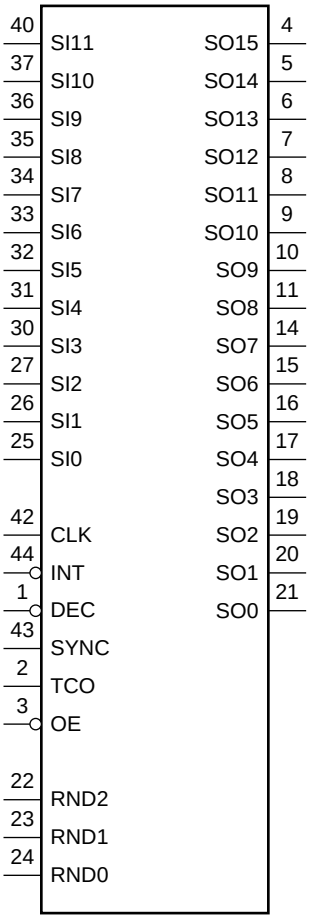
C-MOS 12/16-BIT HALF-BAND INTERPOLATION/DECIMATING DIGITAL FILTER

– TOP VIEW –





(V_{DD} = +5 V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{DEC}$	12	—	GND	23	I	RND1	34	I	SI7
2	I	TCO	13	—	V_{DD}	24	I	RND0	35	I	SI8
3	I	$\overline{OE}$	14	O	SO7	25	I	SI0	36	I	SI9
4	O	SO15	15	O	SO6	26	I	SI1	37	I	SI10
5	O	SO14	16	O	SO5	27	I	SI2	38	—	V_{DD}
6	O	SO13	17	O	SO4	28	—	GND	39	—	GND
7	O	SO12	18	O	SO3	29	—	V_{DD}	40	I	SI11
8	O	SO11	19	O	SO2	30	I	SI3	41	—	GND
9	O	SO10	20	O	SO1	31	I	SI4	42	I	CLK
10	O	SO9	21	O	SO0	32	I	SI5	43	I	SYNC
11	O	SO8	22	I	RND2	33	I	SI6	44	I	$\overline{INT}$

INPUT

CLK ; MASTER CLOCK
$\overline{DEC}$; DECIMATION CONTROL
$\overline{INT}$; INTERPOLATION CONTROL
$\overline{OE}$; OUTPUT ENABLE
RND0-RND2 ; ROUNDING CONTROL
SI0-SI11 ; DATA INPUTS
SYNC ; SYNCHRONIZATION CONTROL
TCO ; TWO'S COMPLEMENT FORMAT CONTROL

OUTPUT

SO0-SO15 ; DATA OUTPUTS

MODE SELECTION		
$\overline{INT}$	$\overline{DEC}$	MODE
0	0	PASS-THROUGH *
0	1	INTERPOLATE
1	0	DECIMATE
1	1	PASS-THROUGH *

* Input and output registers run at full clock rate.

0 ; LOW LEVEL
1 ; HIGH LEVEL