

Product Preview

Low-Voltage CMOS 16-Bit Latching Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16543 is a high performance, non-inverting 16-bit latching transceiver operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate control inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16543 inputs to be safely driven from 5V devices. The MC74LCX16543 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

For data flow from A to B with the \overline{EAB} LOW, the A-to-B Output Enable (OEAB) must be LOW in order to enable data to the B bus, as indicated in the Function Table. With \overline{EAB} LOW, a LOW signal on the A-to-B Latch Enable (LEAB) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the LEAB signal will latch the A latches, and the outputs no longer change with the A inputs. With \overline{EAB} and OEAB both LOW, the 3-State B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is symmetric to that above, but uses the \overline{EBA} , \overline{LEBA} , and OEBA inputs.

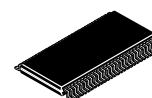
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0V$
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

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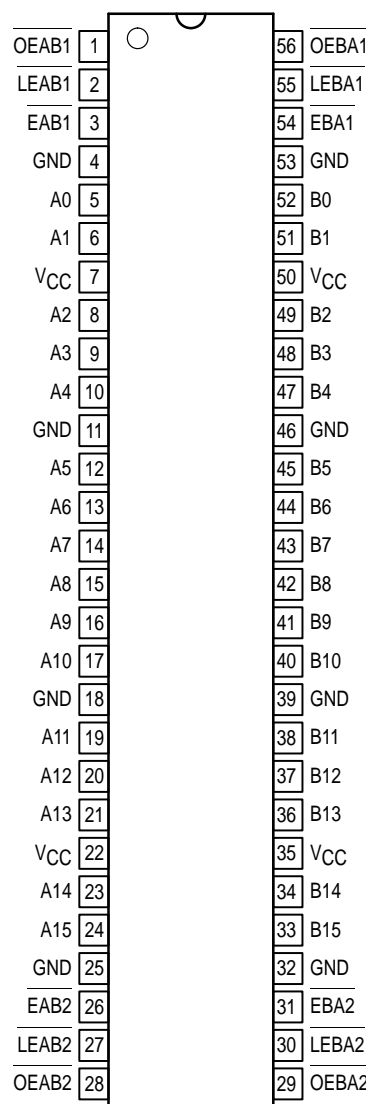
MC74LCX16543

LCX

LOW-VOLTAGE CMOS
16-BIT LATCHING
TRANSCIVER

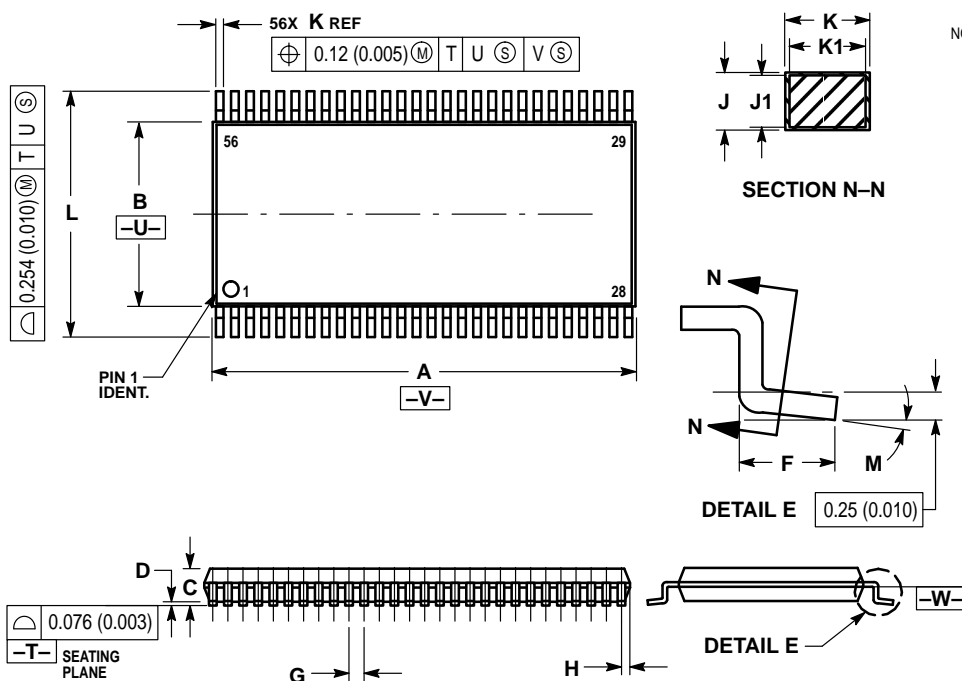


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202-01



OUTLINE DIMENSIONS


DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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