Product Preview

Low-Voltage CMOS 18-Bit Universal Bus Transceiver

With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

MC74LCX16500

LCX

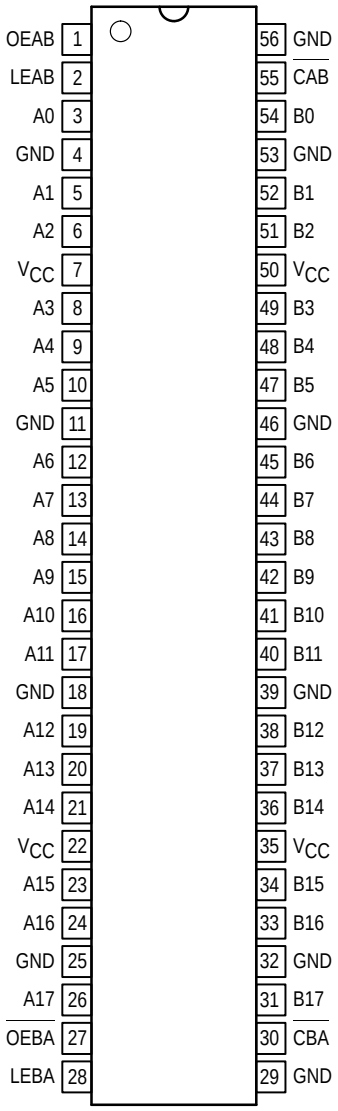
LOW–VOLTAGE CMOS 18–BIT UNIVSERAL BUS TRANSCEIVER

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01

The MC74LCX16500 is a high performance, non–inverting 18–bit universal bus transceiver operating from a 2.7 to 3.6V supply. The device is “byte+1” controlled. Each “byte+1” has separate control inputs which can be tied together for full 18–bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5V allows MC74LCX16500 inputs to be safely driven from 5V devices. The MC74LCX16500 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Data flow in each direction is controlled by Output Enable (OEAB, OEBA), Latch Enable (LEAB, LEBA) and Clock inputs (CAB, CBA). When LEAB is HIGH, the A–to–B dataflow is transparent. When LEAB is LOW, and CAB is held at LOW or HIGH, the data A is latched; on the HIGH–to–LOW transition of CAB the A–data is stored in the latch/flip–flop. The outputs are active when OEAB is HIGH. When OEAB is LOW the B–outputs are in 3–state. Similarly, the LEBA, OEBA and CBA control the B–to–A dataflow. Please note that the output enables are complementary; OEAB is active HIGH, OEBA is active LOW.

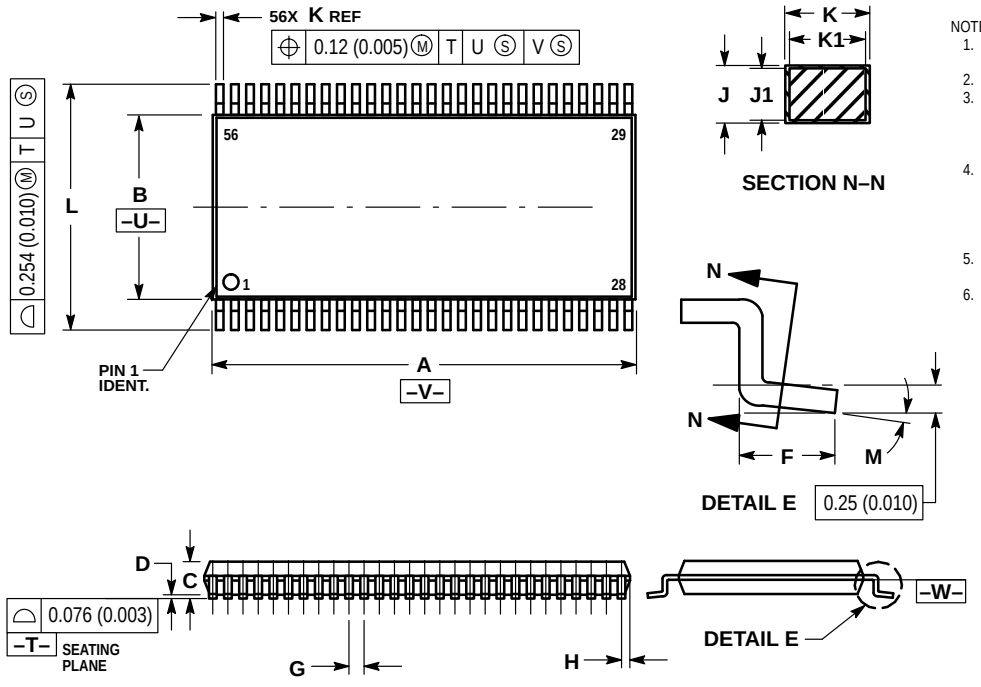
- Designed for 2.7 to 3.6V V_{CC} Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 1202–01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	6.00	6.20	0.236	0.244
C	—	1.10	—	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.12	—	0.005	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

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