

LC89972M

PAL CCD Delay Line

Overview

The LC89972M is a CCD delay line for PAL television systems. It incorporates a comb filter for chrominance signal and a 1H delay line for luminance signal.

Structure

• NMOS + CCD

Functions

- Two CCD shift registers (for chrominance and luminance signals)
- · CCD drive circuits
- · CCD stage count switching circuit
- · CCD signal adder
- · Auto-bias circuit
- Sync tip clamping circuit (luminance signal)
- Center-bias circuit (chrominance signal)
- · Sample-and-hold circuit
- PLL 3 × frequency multiplier
- 3 fsc clock output circuit
- · RD voltage generator

Features

- 5 V single-voltage power supply
- Built-in PLL 3 × frequency multiplier circuit allows 3 fsc operation from an fsc (4.43 MHz) input.
- Control pin switchable to handle PAL/GBI and 4.43 MHz NTSC systems.
- Built-in chrominance signal crosstalk exclusion comb filter features high-precision comb characteristics in an adjustment-free circuit.
- Built-in peripheral circuits allow applications to be constructed with a minimum number of external components.
- Positive-phase signal input/positive-phase signal output (luminance signal)

Specifications

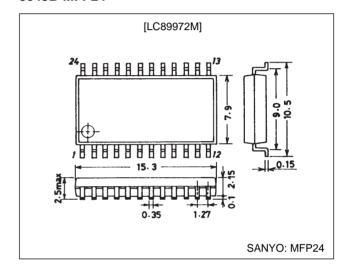
Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max		-0.3 to +6.0	V
Allowable power dissipation	Pd max		600	mW
Operating temperature	Topr		-10 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

Package Dimensions

unit: mm

3045B-MFP24



LC89972M

Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Clock input amplitude	V _{CLK}		300	500	1000	mVp-p
Clock frequency	F _{CLK}	Sine wave	_	4.43361875	_	MHz
Clock signal input amplitude	V _{IN-C}		_	350	500	mVp-p
Luminance signal input amplitude	V _{IN-Y}		_	400	572	mVp-p

Electrical Characteristics at Ta = 25 $^{\circ}C,\,V_{DD}$ = 5.0 V, F_{CLK} = 4.43361875 MHz, V_{CLK} = 500 mVp-p

Parameter	Coursels and	5	Switch state	s	Conditions	min	typ	max	Unit
	Symbol	SW1	SW2	SW3					
Supply current	I _{DD-1}	а	а	b	1	40	50	60	mA
Зарріу сапені	I _{DD-2}	b	а	b	1	40			
Chrominance System Character	ristics (with no Y-	-IN input)							
Pin voltage (input)	V _{INC-1}	а	а	b		2.0	2.4	2.8	V
Till Voltage (illput)	V _{INC-2}	b	а	b	2				
Pin voltage (output)	V _{OUTC-1}	а	а	b		1.2	1.6	2.0	V
riii voitage (output)	V _{OUTC-2}	b	а	b		1.2			
Voltage gain	G _{VC-1}	а	а	b	3	-2	0	+2	dB
	G _{VC-2}	b	а	b					
Comb depth	C _{D-1}	а	а	b	4	_	-40	-35	dB
	C _{D-2}	b	а	b					
Linearity	L _{NC-1}	а	а	b	5	-0.3	0.0	+0.3	dB
Linearity	L _{NC-2}	b	а	b					
Clock leakage (3 fsc)	L _{CK3C-1}	а	а	b		_	10	50	mVrms
Olock leakage (5 150)	L _{CK3C-2}	b	а	b	6				
Clock leakage (fsc)	L _{CK1C-1}	а	а	b	O	_	0.8	1.5	mVrms
Glock leakage (130)	L _{CK1C-2}	b	а	b					
Noise	N _{C-1}	а	а	b	7	_	0.5	2.0	mVrms
INUISE	N _{C-2}	b	а	b	7				
Output impedance	Z _{OC-1}	а	а	a, b	8	200	350	500	Ω
	Z _{OC-2}	b	а	a, b		200	330	000	32
0 H delay time	T _{DC-1}	а	а	b	9	_	245		ns
on delay lime	T _{DC-2}	b	a	b	9	_			

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Parameter	O:l		Switch state	:S	Conditions	min	typ	max	Unit
	Symbol	SW1	SW2	SW3					
Luminance System Characteristic	s (with no C-IN	11 or C-IN2	input)	•		•			
Pin voltage (input)	V _{INY-1}	а	а	b		1.7	2.1	2.5	V
	V _{INY-2}	b	а	b	10				
Din voltogo (outnut)	V _{OUTY-1}	а	а	b		0.8	1.2	1.6	V
Pin voltage (output)	V _{OUTY-2}	b	а	b		0.6			V
Voltage gain	G _{VY-1}	а	а	b	11	-2	0	+2	dB
Voltage gain	G _{VY-2}	b	а	b	''	-2			
Eroguenov rosponso	G _{FY-1}	а	b	b	12	-2	0	+2	dB
Frequency response	G _{FY-2}	b	b	b	12				
Differential gain	D _{GY-1}	а	а	b	13	0	5	7	%
	D _{GY-2}	b	а	b					
Differential phase	D _{PY-1}	а	а	b		0	5	7	deg
	D _{PY-2}	b	а	b					
Linearity	L _{SY-1}	а	а	b	14	37	40	43	%
Linearity	L _{SY-2}	b	а	b	14				
Clock leakage (3 fsc)	L _{CK3Y-1}	а	а	b		_	10	50	mVrms
Clock leakage (5 150)	L _{CK3Y-2}	b	а	b	15				
Clock leakage (fsc)	L _{CK1Y-1}	а	а	b		_	0.8	1.5	mVrms
Olock leakage (190)	L _{CK1Y-2}	b	а	b					
Noise	N _{Y-1}	а	а	b	16	_	0.5	2.0	mVrms
NOISE	N _{Y-2}	b	а	b					
Output impedance	Z _{OY-1}	а	а	c, b	17	250	400	550	Ω
- Catpat Impodanoo	Z _{OY-2}	b	а	c, b	17				
Delay time	T _{DY-1}	а	а	b	18	_	63.92	_	μs
Doiay allie	T _{DY-2}	b	а	b	18	_	63.47	_	μ3

Test Conditions

- 1. Supply current with no signal input
- 2. C-OUT voltage (center bias voltage) with no signal input.
- 3. Measure the C-OUT output with 350 mVp-p sine wave signals input to C-IN1 and C-IN2.

$$G_{VC} = 20 log \frac{C\text{-OUT output } [mVp\text{-}p]}{350 [mVp\text{-}p]} [dB]$$

Test frequencies

 G_{VC} -1 4.429662 MHz (PAL/GBI)

G_{VC}-2 4.425694 MHz (4.43 NTSC)

4. Measure the comb depth from the C-OUT output with a 350 mVp-p sine wave signal of frequency fa input to C-IN1 and C-IN2 and with a frequency of fb input.

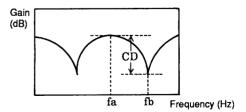
$$C_D = 20 log \frac{\text{C-OUT output with fb input } [\text{mVp-p}]}{\text{C-OUT output with fa input } [\text{mVp-p}]} [\text{dB}]$$

Test frequencies

fa fb

C_D-1 4.429662 MHz 4.425756 MHz (PAL/GBI)

C_D-2 4.425694 MHz 4.417819 MHz (4.43 NTSC)



5. Measure the C-OUT output with a 200 mVp-p sine wave signal input to C-IN1 and C-IN2 and with 500 mVp-p sine wave signal input and calculate the difference in the gains.

$$L_{NC} = 20 \ log \ \left(\ \frac{Output \ for \ a \ 500 \ mVp-p \ input \ [mVp-p]}{500 \ [mVp-p]} \ \middle/ \ \frac{Output \ for \ a \ 200 \ mVp-p \ input \ [mVp-p]}{200 \ [mVp-p]} \ \right) \ [dB]$$

Test frequencies

- 6. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the C-OUT output with no input.
- 7. Measure the noise in the C-OUT output with no input.

 Measure the noise with a noise meter set up with a 200 kHz high-pass filter and a 5 MHz low-pass filter.
- 8. Let V1 be the C-OUT output with a 350 mVp-p sine wave input to C-IN1 and C-IN2 and SW3 set to a, and let V2 be the C-OUT output with SW3 set to b.

$$Z_{OC} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

Test frequencies

- 9. The C-OUT output delay time with respect to inputs to C-IN1. (the CCD 2.5 bit delay)
- 10. Y-OUT voltage (clamp voltage) with no signal input.
- 11. Measure the Y-OUT output with a 200 kHz 400 mVp-p sine wave input to Y-IN.

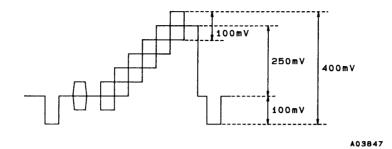
$$G_{VY} = 20 log \frac{Y\text{-OUT output } [mVp\text{-}p]}{400 [mVp\text{-}p]} [dB]$$

12. Measure the Y-OUT output with a 200 kHz 200 mVp-p sine wave input to Y-IN and with a 3.3 MHz 200 mVp-p sine wave input.

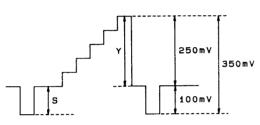
$$G_{FY} = 20 \ log \ \frac{Y\text{-OUT output with a 3.3 MHz input }[mVp\text{-}p]}{Y\text{-OUT output with a 200 kHz input }[mVp\text{-}p]} \ [dB]$$

Note that V_{bias} should be adjusted so that the circuit is biased to the clamp level plus 250 mV.

13. Input a five-level step waveform (see the figure below) to Y-IN and measure the differential gain and differential phase in the Y-OUT output with a vector scope.



14. Input a five-level step waveform (see the figure below) to Y-IN and measure the luminance level (Y) and the sync level (S) in the Y-OUT output.



$$L_{S} = \frac{S [mV]}{Y [mV]} \times 100 [\%]$$

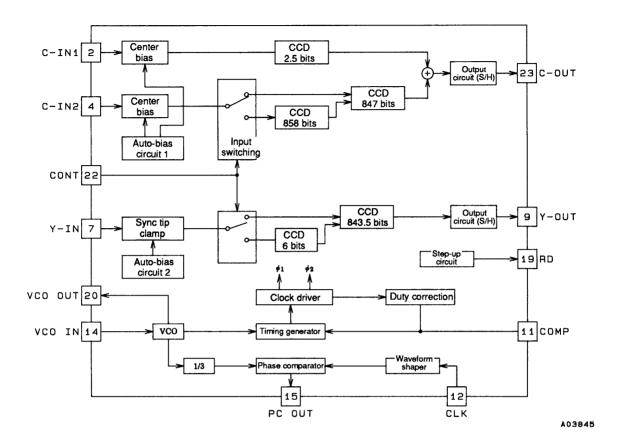
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- 15. Measure the 3 fsc (13.3 MHz) and fsc (4.43 MHz) components in the Y-OUT output with no input.
- 16. Measure the noise in the Y-OUT output with no input.
 Measure the noise with a noise meter set up with a 200 kHz high-pass filter, a 5 MHz low-pass filter and a 4.43 MHz trap filter.
- 17. Let V1 be the Y-OUT output with a 200 kHz 400 mVp-p sine wave input and SW3 set to c, and let V2 be the C-OUT output with SW3 set to b.

$$Z_{OY} = \frac{V2 \text{ [mVp-p]} - V1 \text{ [mVp-p]}}{V1 \text{ [mVp-p]}} \times 500 \text{ [}\Omega\text{]}$$

18. The Y-OUT delay time with respect to Y-IN

Block Diagram



Control Pin Function

CONT	Mode (representative example)	Chrominance signal delay (CCD bits)	Luminance signal delay (CCD bits)	
Low	PAL/GBI	2 H (1705) + 0 H (2.5)	1 H (849.5)	
High	4.43 NTSC	1 H (847) + 0 H (2.5)	1 H (843.5)	

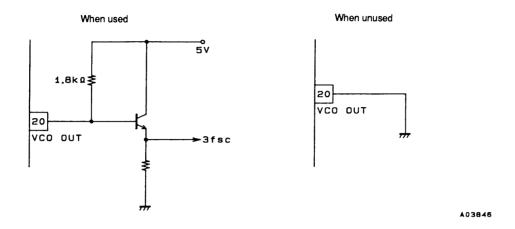
Switching Voltage Levels

Low/high	Symbol	min	typ	max	Unit
Low	V _L	-0.3	0.0	+0.5	V
High	V _H	2.0	5.0	6.0	٧

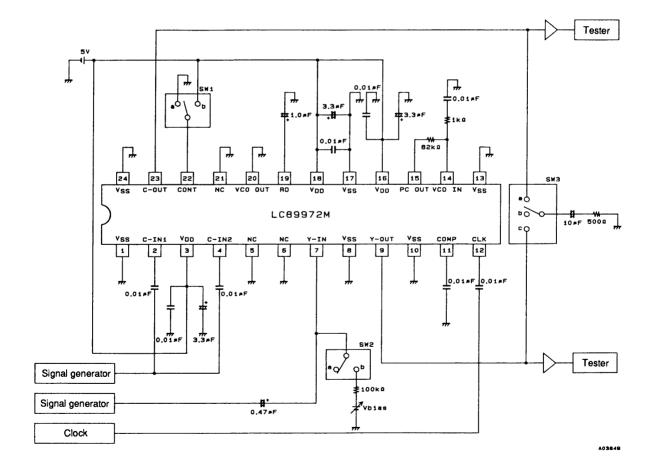
Note: Since the control pin has a built-in pull-down resistor, the pin will be set to the low state if left open.

VCO OUT Pin Function

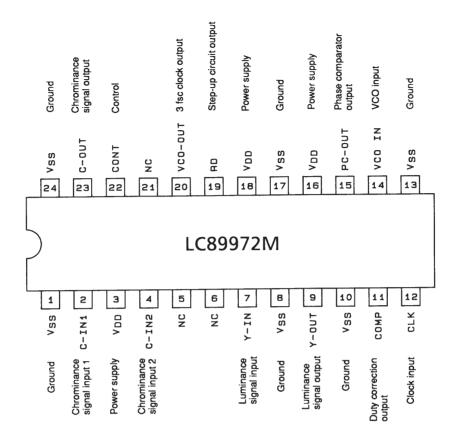
This pin outputs the 3 fsc clock generated by the PLL 3 × frequency multiplier circuit.



Test Circuit



Test Circuit



Top view

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