

# SCSI CD-ROM Decoder with On-Chip DVD Interface

#### Overview

The LC897127K is a CD-ROM decoder that includes an on-chip DVD interface. Since the LC897127K also includes an on-chip SCSI interface, it can be used to implement a SCSI-compatible DVD-ROM drive simply by combining it with a DVD decoder. It can also operate as an independent SPC functional unit.

#### **Functions**

- CD-ROM ECC function, subcode read function, SCSI I/F, CAV audio function, DVD I/F
- ATAPI-to-SCSI conversion function, DMA I/F-to-SCSI conversion function

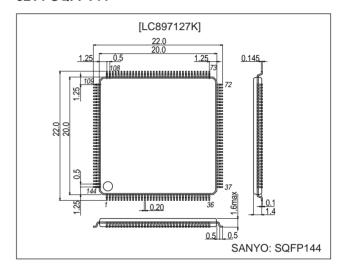
#### **Features**

- Built-in SCSI I/F (Built-in register for SCAM selection)
- 20× speed and transfer speed of 10 Mbytes/s supported using EDO-DRAM (×16, 70 ns)
- 32× speed and transfer speed of 10 Mbytes/s supported using EDO-DRAM (16×, 50 ns)
- Up to 4 Mbits of buffer RAM connectable
- CD main channel and C2 flag areas in buffer RAM can be freely set by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, etc. at one time)
- Built-in multi block transfer function (function for sending several blocks at one time)
- Built-in subcode buffering function and CD text support
- Built-in CAV audio function
- 20 Mbytes/s transfer supported
- Built-in DVD I/F
- Built-in ATAPI I/F-to-SCSI conversion function
- Built-in DMA I/F-to-SCSI conversion function

# **Package Dimensions**

unit: mm

#### 3214-SQFP144



- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

# **Specifications**

# Absolute Maximum Ratings at $V_{SS} = 0 V$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	Ta = 25°C	-0.3 to +7.0	V
Input/output voltage	V <sub>I</sub> V <sub>O</sub>	Ta = 25°C	-0.3 to V <sub>DD</sub> +0.3	V
Allowable power dissipation	Pd max	Ta≤70°C	550	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-55 to +125	°C
Soldering temperature (pin part only)		10s	260	°C

## Allowable Operating Ranges at Ta = -30 to $+70^{\circ}C$ , $V_{SS} = 0$ V

Parameter	Cumbal	Symbol Conditions		Unit		
Farameter	Symbol	Conditions	min	typ	max	Ullit
Supply voltage	V <sub>DD</sub>		4.5	5.0	5.25	V
Input voltage range	V <sub>IN</sub>		0		$V_{DD}$	V

### DC Characteristics at Ta = -30 to +70 °C, $V_{SS}$ = 0 V, $V_{DD}$ = 4.5 to 5.5 V

D	0	Complishing a	A		Unit			
Parameter	Symbol	Conditions	Applicable pins	min	typ	max	Onit	
Input high-level voltage	V <sub>IH1</sub>	TTL levels	(4)	2.2			V	
Input low-level voltage	V <sub>IL1</sub>	1 I L levels	(1)			0.8	V	
Input high-level voltage	V <sub>IH2</sub>	TTL levels	(0)	2.2	_	_	V	
Input low-level voltage	V <sub>IL2</sub>	with pull-up resistor	(9)	_	_	0.8	V	
Input high-level voltage	V <sub>IH3</sub>	TTL levels	(2)	2.2	_	_	V	
Input low-level voltage	V <sub>IL3</sub>	Schmitt	(2)	_	_	0.8	V	
Input high-level voltage	V <sub>IH3</sub>	TTL levels	(11)	2.2	_	_	V	
Input low-level voltage	V <sub>IL3</sub>	Schmitt with pull-down resistor	(11)	_	_	0.8	V	
Input high-level voltage	V <sub>IH4</sub>	TTL levels	(42)	2.2	_	_	V	
Input low-level voltage	V <sub>IL4</sub>	Schmitt with pull-up resistor	(12)	_	_	0.8	V	
Input high-level voltage	V <sub>IH4</sub>	CMOS levels	(2)	0.8 V <sub>DD</sub>	_	_	V	
Input low-level voltage	V <sub>IL4</sub>	Schmitt	(3)	_	_	0.2 V <sub>DD</sub>	V	
Input high-level voltage	VI <sub>H5</sub>		(4) (9) (40)	2.0		_	V	
Input low-level voltage	V <sub>IL5</sub>		(4), (8), (10)			0.8	V	
Output high-level voltage	V <sub>OH1</sub>	I <sub>OH1</sub> = -12 mA	(6)	V <sub>DD</sub> – 2.1	_	_	V	
Output low-level voltage	V <sub>OL1</sub>	I <sub>OL1</sub> = 12 mA	(6)	_	_	0.4	V	
Output high-level voltage	V <sub>OH2</sub>	I <sub>OH2</sub> = -8 mA	(7) (11)	2.4		_	V	
Output low-level voltage	V <sub>OL2</sub>	I <sub>OL2</sub> = 8 mA	(7), (11)			0.4	V	
Output high-level voltage	V <sub>OH2</sub>	I <sub>OH2</sub> = -2 mA	(O) (E)	2.4		_	V	
Output low-level voltage	V <sub>OL2</sub>	I <sub>OL2</sub> = 2 mA	(9), (5)			0.4	V	
Output low-level voltage	V <sub>OL4</sub>	I <sub>OL4</sub> = 48 mA	(10)			0.4	V	
Input leakage current	I <sub>IL</sub>	$V_I = V_{SS}, V_{DD}$	All input pins	-25		+25	μA	
Pull-up resistance	R <sub>UP</sub>		(5), (9)	60	120	240	kΩ	
Pull-down resistance	R <sub>DOWN</sub>		(11)	60	120	240	kΩ	

Applicable pin sets are as follows.

INPUT (1) TEST0 to TEST4, CSCTRL, SUA0 to SUA6, C2PO, SDATA, BCK, LRCK, SCOR, WFCK, SBS0, MCK2SEL

- (2) RESET
- (3)  $\overline{CS}, \overline{RD}, \overline{WR}$
- (4) SCSISEL, XTALSEL

OUTPUT (5) INTO, INT1, SWAIT

- (6) MCK
- (7) EXCK, DSDATA, DLRCK, DBCK, RASO, CASO, CASO, OE, UWE, LWE, RAO to RA8, HDBDIR

INOUT (8) ACK, ATN

- (9) D0 to D7, IO0 to IO15
- (10)  $\overline{DB0}$  to  $\overline{DB7}$ ,  $\overline{DBP}$ ,  $\overline{BSY}$ , I/O,  $\overline{MSG}$ ,  $\overline{SEL}$ ,  $\overline{RST}$ ,  $\overline{REQ}$ , C/D
- (11) DRESP, DREQ, HDB0 to HDB7
- (12) IOP0 to IOP7 (No pull-up resistor used when these pins are used as pins HDB0 to HDB7)

Note: Pins XTALO, XTALCKO, XTAL1, XTALCK1, and X1EN are not included in DC characteristics.

#### **SCSI Pin Input Characteristics**

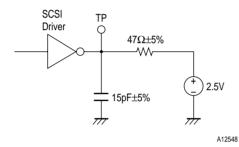
Parameter	Symbol	col Conditions		Ratings				
Falametei	Symbol		min	typ	max	Unit		
Input threshold voltage	V <sub>t+t1</sub>	V <sub>DD</sub> = 4.50 to 5.50 V		1.60	2.00	V		
Input threshold voltage	V <sub>t-t1</sub>		0.80	1.10		V		
Hysteresis width	$\Delta V_{tt1}$	V <sub>DD</sub> = 5.0 V	0.41	0.5		V		

#### **Active Low Output Characteristics**

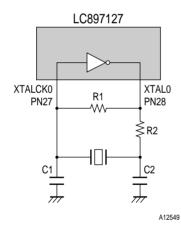
Parameter	Symbol	Conditions		Unit		
Faiametei	Symbol	Conditions	min	typ	max	Ullit
Output high-level voltage	V <sub>OH</sub>		2.5			V
Output low-level voltage	V <sub>OL</sub>				0.4	V

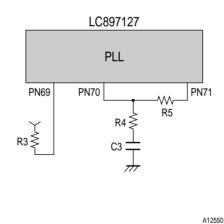
Note: Only applies to the active-low output pins  $\overline{DB0}$  to  $\overline{DB7}$ ,  $\overline{REQ}$ , and  $\overline{DBPB}$ 

#### **Rise Time Test Circuit**



#### **Recommended Oscillator and PLL Circuits**





 $R1 = 120 \text{ k}\Omega$ ,  $R2 = 47 \Omega$ , C1 = 30 pF

Crystal element oscillator frequency XTALCK0 = 16.9344 MHz

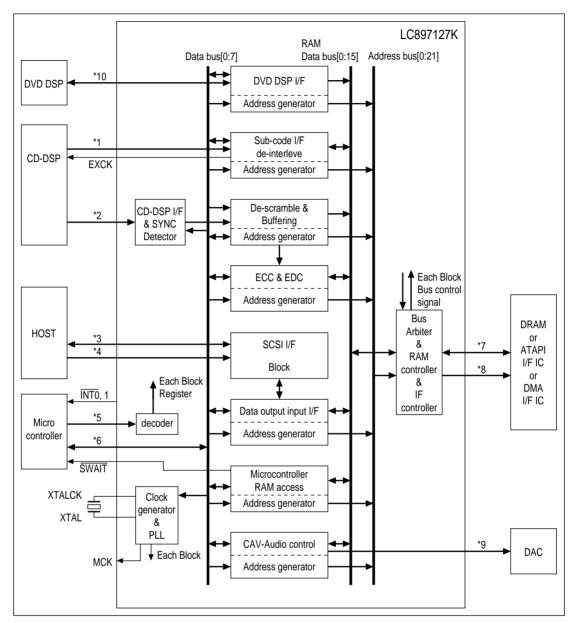
$$R3 = 7.5 \text{ k}\Omega$$
,  $R4 = 200 \Omega$ ,  $R5 = 10 \text{k} \Omega$ ,  $C3 = 0.1 \mu\text{F}$ 

Note: The values listed above for R3, R4, R5, and C3 also apply when the XTALKC0 frequency is 33.8688 MHz.

Applications must be designed so that the analog  $V_{DD}$  and  $V_{SS}$  power supply system is completely independent of the logic system power supply and is not affected by the logic system power supply in any way.

Since the exact values of these components will vary depending on characteristics of the printed circuit board used and other factors, consult the manufacturer of the crystal element when designing the oscillator circuit.

#### **Block Diagram**



A12551

- \*1. WFCK, SBSO, SCOR
- \*2. BCK, SDATA, LRCK, C2PO
- $*3. \ \overline{DB0} \ to \ \overline{DB7}, \ \overline{DBP}, \ \overline{BSY}, \ \overline{MSG}, \ \overline{SEL}, \ \overline{RST}, \ \overline{REQ}, \ I/O, \ C/D$
- \*4. ACK, ATN
- \*5. RD, WR, SUA0 to SUA6, CS, CSCTRL
- \*6. D0 to D7
- \*7. IO0 to IO15 (Data bus for both ATAPI and DMA interfaces)
- \*8. RA0 to RA10, RAS1, RAS0, OE, UWE, LWE

ATAPI interface: SBSO (DMARQ), DBCK (DMACK), DLRCK (DIOR), DSDATA (DIOW) DMA interface: EXCK (DMARQ), C2PO (DMACK), SDATA (DIOR), BCK (DIOW)

- \*9. DBCK, DLRCK, DSDATA
- \*10. HDB7 to HDB0, DRESP, DREQ

See the circuit examples for details on ATAPI and DMA interface IC connection.

### LC897127K Pin Functions

When the DVD Interface is Used

			Туре		
1	INPUT	В	BIDIRECTION	NC	NOT CONNECT
0	OUTPUT	Р	POWER		

Pin No.	Pin	Туре	Function
1	V <sub>SS0</sub>	P	
2	IO2	В	
3	IO1	В	Buffer RAM data I/O.
4	100	В	These pins have built-in pull-up resistors.
5	MCK2SEL	1	PLL frequency selection. This pin must be connected to V <sub>DD</sub> .
6	C2PO	i	· LE Moquello Millio pin must be commoded to TDD.
7	SDATA	i	
8	BCK	i	CD DSP interface
9	LRCK	i	
10	EXCK	0	
11	WFCK	ı	Subcode I/O
12	SBSO	i	
13	SCOR	1	Subcode I/O
14	DSDATA	0	
15	DLRCK	0	D/A converter outputs
16	DBCK	0	
17	MCK	0	XTALCLK0 1/1, 1/2, and stop output
18	V <sub>DD</sub>	P	, , , , ,
19	V <sub>SS0</sub>	Р	
20	RESET	1	IC reset. The IC is reset on a low-level input.
21	CSCTRL	1	Microcontroller CS low/high
22	TEST3	1	,
23	TEST0	1	
24	TEST1	1	Test pins. These pins must be connected to V <sub>SS0</sub> in normal operation.
25	TEST2	ı	
26	V <sub>SS0</sub>	Р	
27	XTALCK0	ı	Crystal oscillator circuit input
28	XTAL0	0	Crystal oscillator circuit output
29	TEST4	ı	Test pin. This pin must be connected to V <sub>SS0</sub> in normal operation.
30	DRESP	В	DVD ECC data latching. A pull-down resistor is built in.
31	HDBDIR	0	DVD data bus direction output. A pull-down resistor is built in.
32	DREQ	В	DVD ECC data request. A pull-down resistor is built in.
33	V <sub>SS0</sub>	Р	
34	HDB7	ı	
35	HDB6	I	DVD data input
36	V <sub>SS0</sub>	Р	
37	V <sub>DD</sub>	Р	
38	HDB5	ı	
39	HDB4	ı	
40	HDB3	ı	DVD data irant
41	HDB2	I	DVD data input
42	HDB1	ı	
43	HDB0	I	
44	V <sub>SS0</sub>	Р	
45	RD	I	Microcontroller data read signal input
46	WR	I	Microcontroller data write signal input
47	CS	I	Register chip select input from the microcontroller
48	SUA0	I	
49	SUA1	I	
50	SUA2	I	Micro controllor register celection sign-1-
51	SUA3	I	Microcontroller register selection signals
F0	SUA4	ı	
52			

Continued from preceding page.

Pin No.	Pin	Туре	Function
54	$V_{DD}$	Р	
55	$V_{SS0}$	Р	
56	SUA6	I	Microcontroller register selection signals
57	D0	В	
58	D1	В	
59	D2	В	
60	D3	В	Microcontroller data signals
61	D4	В	
62	D5	В	
63	V <sub>SS0</sub>	Р	
64	D6	В	
65	D7	В	Microcontroller data signals
66	ĪNT0	0	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	INT1	0	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	SWAIT	0	Wait signal output to the microcontroller
69	X1EN	i	Used by the PLL. This pin must be connected to V <sub>DD</sub> through a resistor.
70	XTALCK1	i	Used by the PLL.
71	XTAL1	0	Used by the PLL.
72	V <sub>SS0</sub>	P	Analog V <sub>SS</sub>
73		P	Analog V <sub>SS</sub> Analog V <sub>DD</sub>
74	$V_{DD}$		Allalog VDD
	1/0	NC	
75	1/0	В	SCSI interface
76	REQ	В	
77	V <sub>SS1</sub>	P	
78	C/D	В	SCSI interface
79	SEL	В	
80		NC	
81	V <sub>DD</sub>	Р	
82	V <sub>SS1</sub>	Р	
83	MSG	В	SCSI interface
84	RST	В	
85	V <sub>SS1</sub>	Р	
86	ACK	В	SCSI interface
87	BSY	В	COOL INCOLOGO
88	V <sub>SS1</sub>	Р	
89	ĀTN	В	SCSI interface
90	$V_{DD}$	Р	
91	V <sub>SS1</sub>	Р	
92		NC	
93	DBP	В	SCSI interface
94	$V_{DD}$	Р	
95	DB7	В	0001:44-4
96	DB6	В	SCSI interface
97	V <sub>SS1</sub>	Р	
98	DB5	В	
99	DB4	В	SCSI interface
100	V <sub>DD</sub>	Р	
101	DB3	В	
102	DB2	В	SCSI interface
103	V <sub>SS1</sub>	P	
104	DB1	В	
105	DB0	В	SCSI interface
	SCSISEL	I	SCSI pin layout selection. (This pin must be connected to V <sub>SS0</sub> .)
106			

#### Continued from preceding page.

Pin No.	Pin	Type	Function
108	V <sub>SS1</sub>	Р	
109	$V_{DD}$	Р	
110	V <sub>SS0</sub>	Р	
111	RAS0	0	Buffer RAM RAS signal output 0
112	DVDSEL	Р	V <sub>SS0</sub> selects the DVD interface and V <sub>DD</sub> selects the I/O port function.
113	CAS0	0	Buffer RAM CAS signal output 0 (Normally fixed at 0 (low).)
114	CAS1	0	Buffer RAM CAS signal output 1
115	ŌE	0	Buffer RAM output enable
116	UWE(RA9)	0	Buffer RAM upper write enable (RA9 when 8M or more DRAM is used.)
117	LWE	0	Buffer RAM lower write enable
118	V <sub>SS0</sub>	Р	
119	RA0	0	
120	RA1	0	
121	RA2	0	
122	RA3	0	Buffer RAM address signal outputs
123	RA4	0	
124	RA5	0	
125	RA6	0	
126	$V_{DD}$	Р	
127	V <sub>SS0</sub>	Р	
128	RA7	0	Duffee DAM address sixed autoute
129	RA8	0	Buffer RAM address signal outputs
130	IO15	В	
131	IO14	В	
132	IO13	В	
133	IO12	В	Buffer RAM data I/O.
134	IO11	В	These pins have built-in pull-up resistors.
135	IO10	В	
136	109	В	
137	IO8	В	
138	V <sub>SS0</sub>	Р	
139	107	В	
140	IO6	В	Duffer DAM data I/O
141	IO5	В	Buffer RAM data I/O.
142	104	В	These pins have built-in pull-up resistors.
143	IO3	В	
144	$V_{DD}$	Р	

- Unused ("NC") pins must be left open.
  Pins whose name is under a bar operate with inverted (negative) logic.
- V<sub>SS0</sub> is the logic system ground and V<sub>SS1</sub> is the SCSI interface driver ground.

   If DRAM is used, applications must adopt measures to prevent undershoot and other DRAM problems. Such measures include inserting resistors in the RAS and CAS lines and inserting capacitors between V<sub>SS</sub> pins. See the article on Designing with the Latest Microcontrollers and Memory in special issue number 25 of Transistor Technology for details on these measures.

  • Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

# LC897127K Pin Functions

When ATAPI to SCSI Conversion is Used

			Туре		
1	INPUT	В	BIDIRECTION	NC	NOT CONNECT
0	OUTPUT	Р	POWER		

Pin No.	Pin	Туре	Function			
1	V <sub>SS0</sub>	Р				
2	IO2	В				
3	IO1	В	ATAPI data I/O.			
4	100	В	These pins have built-in pull-up resistors.			
5	MCK2SEL	I	This pin must be connected to V <sub>DD</sub> .			
6	V <sub>SS0</sub>	P	F			
7	V <sub>SS0</sub>	P				
8	V <sub>SS0</sub>	P				
9	V <sub>DD</sub>	P				
10	טטי	NC NC				
11	V <sub>DD</sub>	P				
12	DMARQ		ATAPI interface			
13	V <sub>DD</sub>	Р				
14	DIOW	0				
15	DIOR	0	ATAPI interface			
16	DMACK	0				
17	MCK	0	XTALCLK0 1/1, 1/2, and stop output			
18	V <sub>DD</sub>	Р				
19	V <sub>SS0</sub>	Р				
20	RESET	ı	IC reset. The IC is reset on a low-level input.			
21	CSCTRL	ı	Microcontroller CS low/high			
22	TEST3	ı				
23	TEST0	ı				
24	TEST1	ı	Test pins. These pins must be connected to V <sub>SS0</sub> in normal operation.			
25	TEST2	I				
26	V <sub>SS0</sub>	Р				
27	XTALCK0	1	Crystal oscillator circuit input			
28	XTAL0	0	Crystal oscillator circuit output			
29	TEST4	ı	Test pin. This pin must be connected to V <sub>SS0</sub> in normal operation.			
30	V <sub>SS0</sub>	Р				
31	V <sub>SS0</sub>	Р				
32	V <sub>SS0</sub>	Р				
33	V <sub>SS0</sub>	Р				
34	IOP7	I	General-purpose inputs			
35	IOP6	ı	These pins have built-in pull-up resistors.			
36	V <sub>SS0</sub>	Р				
37	V <sub>DD</sub>	Р				
38	IOP5	I				
39	IOP4	I				
40	IOP3	I	General-purpose inputs			
41	IOP2	I	These pins have built-in pull-up resistors.			
42	IOP1	I				
43	IOP0	I				
44	V <sub>SS0</sub>	Р				
45	RD	I	Microcontroller data read signal input			
46	WR	I	Microcontroller data write signal input			
47	CS	I	Register chip select input from the microcontroller			
48	SUA0	I				
49	SUA1	I				
50	SUA2	I	Microcontroller register selection signals			
51	SUA3	I	Militaria i register serection signals			
52	SUA4	I				
53	SUA5	I	Continued on next page			

Continued from preceding page.

Pin No.	Pin	Туре	Function
54	$V_{DD}$	Р	
55	$V_{SS0}$	Р	
56	SUA6	I	Microcontroller register selection signals
57	D0	В	
58	D1	В	
59	D2	В	
60	D3	В	Microcontroller data signals
61	D4	В	
62	D5	В	
63	V <sub>SS0</sub>	Р	
64	D6	В	
65	D7	В	Microcontroller data signals
66	ĪNT0	0	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	ĪNT1	0	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	SWAIT	0	Wait signal output to the microcontroller
69	X1EN	1	Used by the PLL. This pin must be connected to V <sub>DD</sub> through a resistor.
70	XTALCK1	i	Used by the PLL.
71	XTAL1	0	Used by the PLL.
72	V <sub>SS0</sub>	P	Analog V <sub>SS</sub>
73	V <sub>DD</sub>	P	Analog V <sub>DD</sub>
74	<b>₹</b> 00	NC	7 Titalog V <sub>DD</sub>
75	I/O	В	
76	REQ	В	SCSI interface
		Р	
77	V <sub>SS1</sub>		
78	C/D	В	SCSI interface
79	SEL	В	
80		NC	
81	V <sub>DD</sub>	P	
82	V <sub>SS1</sub>	P	
83	MSG	В	SCSI interface
84	RST	В	
85	V <sub>SS1</sub>	Р	
86	ACK	В	SCSI interface
87	BSY	В	
88	V <sub>SS1</sub>	Р	
89	ATN	В	SCSI interface
90	$V_{DD}$	Р	
91	V <sub>SS1</sub>	Р	
92		NC	
93	DBP	В	SCSI interface
94	$V_{DD}$	Р	
95	DB7	В	SCSI interface
96	DB6	В	OCO: IIICITACE
97	V <sub>SS1</sub>	Р	
98	DB5	В	SCSI interface
99	DB4	В	SOSI III. ei iace
100	$V_{DD}$	Р	
101	DB3	В	0001:44-4
102	DB2	В	SCSI interface
103	V <sub>SS1</sub>	Р	
104	DB1	В	
105	DB0	В	SCSI interface
106	SCSISEL	ı	SCSI pin layout selection. (This pin must be connected to V <sub>SS0</sub> .)
I		+	

### Continued from preceding page.

Pin No.	Pin	Туре	Function
108	V <sub>SS1</sub>	Р	
109	V <sub>DD</sub>	Р	
110	V <sub>SS0</sub>	Р	
111		NC	
112	V <sub>DD</sub>	Р	
113		NC	
114		NC	
115		NC	
116		NC	
117		NC	
118	V <sub>SS0</sub>	Р	
119		NC	
120		NC	
121		NC	
122		NC	
123		NC	
124		NC	
125		NC	
126	V <sub>DD</sub>	Р	
127	V <sub>SS0</sub>	Р	
128		NC	
129		NC	
130	IO15	В	
131	IO14	В	
132	IO13	В	
133	IO12	В	ATAPI data I/O
134	IO11	В	These pins have built-in pull-up resistors.
135	IO10	В	
136	IO9	В	
137	IO8	В	
138	V <sub>SS0</sub>	Р	
139	107	В	
140	IO6	В	ATAPI data I/O
141	IO5	В	
142	IO4	В	These pins have built-in pull-up resistors.
143	IO3	В	
144	V <sub>DD</sub>	Р	

- Unused ("NC") pins must be left open.
  Pins whose name is under a bar operate with inverted (negative) logic.
  V<sub>SS0</sub> is the logic system ground and V<sub>SS1</sub> is the SCSI interface driver ground.
  Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

### LC897127K Pin Functions

When DMA Interface to SCSI Conversion is Used

Туре						
-1	INPUT	В	BIDIRECTION	NC	NOT CONNECT	
0	OUTPUT	Р	POWER			

		1		
Pin No.	Pin	Туре	Function	
1	V <sub>SS0</sub>	Р		
2	IO2	В	DAM interface data I/O.	
3	IO1	В	These pins have built-in pull-up resistors.	
4	IO0	В	πιοσο μιπο πανε υαπιτιπ μαπταμ τεσισεύτο.	
5	MCK2SEL	I	This pin must be connected to V <sub>DD</sub> .	
6	DMACK	I		
7	DIOR	I	DMA interface functions	
8	DIOW	ı		
9	$V_{DD}$	Р		
10	DMARQ	0	DMA interface functions	
11	V <sub>DD</sub>	Р		
12	V <sub>DD</sub>	Р		
13	V <sub>DD</sub>	Р		
14		NC		
15		NC		
16		NC		
17	MCK	0	XTALCLK0 1/1, 1/2, and stop output	
18	V <sub>DD</sub>	Р		
19	V <sub>SS0</sub>	Р		
20	RESET	ı	IC reset. The IC is reset on a low-level input.	
21	CSCTRL	ı	Microcontroller CS low/high	
22	TEST3	ı		
23	TEST0	ı	1 _ , , , _, , , , , , , , , , , , , , ,	
24	TEST1	ı	Test pins. These pins must be connected to V <sub>SS0</sub> in normal operation.	
25	TEST2	ı		
26	V <sub>SS0</sub>	P		
27	XTALCK0	1	Crystal oscillator circuit input	
28	XTAL0	0	Crystal oscillator circuit output	
29	TEST4	ı	Test pin. This pin must be connected to V <sub>SS0</sub> in normal operation.	
30	V <sub>SS0</sub>	P		
31	V <sub>SS0</sub>	P		
32	V <sub>SS0</sub>	P		
33	V <sub>SS0</sub>	P		
34	IOP7	1	General-purpose inputs	
35	IOP6	i	These pins have built-in pull-up resistors.	
36	V <sub>SS0</sub>	P		
37	V <sub>DD</sub>	P		
38	IOP5	1		
39	IOP4	i		
40	IOP3	ı	General-purpose inputs	
41	IOP2	ı	These pins have built-in pull-up resistors.	
42	IOP1	· ·		
43	IOP0	· ·	1	
44	V <sub>SS0</sub>	P		
45	RD	1	Microcontroller data read signal input	
46	WR	'	Microcontroller data viite signal input	
47		1	Register chip select input from the microcontroller	
48	SUA0	1	5 1	
49	SUA1	1	1	
50	SUA2	'		
51	SUA3	<u>'</u>	Microcontroller register selection signals	
52	SUA3	'	1	
52	SUA4 SUA5	1	1	
აა	SUAS	1 1	Continued on next page.	

Continued from preceding page.

Pin No.	Pin	Туре	Function	
54	V <sub>DD</sub>	Р		
55	V <sub>SS0</sub>	Р		
56	SUA6	I	Microcontroller register selection signals	
57	D0	В		
58	D1	В	Microcontroller data signals	
59	D2	В		
60	D3	В		
61	D4	В		
62	D5	В		
63	V <sub>SS0</sub>	Р		
64	D6	В	Microcontroller data signals	
65	D7	В		
66	INT0	0	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)	
67	ĪNT1	0	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)	
68	SWAIT	0	Wait signal output to the microcontroller	
69	X1EN	I	Used by the PLL. This pin must be connected to V <sub>DD</sub> through a resistor.	
70	XTALCK1	I	Used by the PLL.	
71	XTAL1	0	Used by the PLL.	
72	V <sub>SS0</sub>	Р	Analog V <sub>SS</sub>	
73	V <sub>DD</sub>	Р	Analog V <sub>DD</sub>	
74		NC		
75	I/O	В	SCSI interface	
76	REQ	В	SCOI interrace	
77	V <sub>SS1</sub>	Р		
78	C/D	В	SCSI interface	
79	SEL	В	SCSI interiace	
80		NC		
81	V <sub>DD</sub>	Р		
82	V <sub>SS1</sub>	Р		
83	MSG	В	SCSI interface	
84	RST	В	OCOI interiace	
85	V <sub>SS1</sub>	Р		
86	ACK	В	SCSI interface	
87	BSY	В	OCOI interiace	
88	V <sub>SS1</sub>	Р		
89	ATN	В	SCSI interface	
90	V <sub>DD</sub>	Р		
91	V <sub>SS1</sub>	Р		
92		NC		
93	DBP	В	SCSI interface	
94	V <sub>DD</sub>	Р		
95	DB7	В	SCSI interface	
96	DB6	В	OOOI III.GII aoo	
97	V <sub>SS1</sub>	Р		
98	DB5	В	SCSI interface	
99	DB4	В	SCSI interface	
100	$V_{DD}$	Р		
101	DB3	В	SCSI interface	
102	DB2	В		
103	V <sub>SS1</sub>	Р		
104	DB1	В	SCSI interfere	
105	DB0	В	SCSI interface	
106	SCSISEL	I	SCSI pin layout selection. (This pin must be connected to V <sub>SS0</sub> .)	
	XTALSEL			

### Continued from preceding page.

Pin No.	Pin	Туре	Function
108	V <sub>SS1</sub>	Р	
109	$V_{DD}$	Р	
110	V <sub>SS0</sub>	Р	
111		NC	
112	$V_{DD}$	Р	
113		NC	
114		NC	
115		NC	
116		NC	
117		NC	
118	V <sub>SS0</sub>	Р	
119		NC	
120		NC	
121		NC	
122		NC	
123		NC	
124		NC	
125		NC	
126	V <sub>DD</sub>	Р	
127	V <sub>SS0</sub>	Р	
128		NC	
129		NC	
130	IO15	В	
131	IO14	В	
132	IO13	В	
133	IO12	В	DMA interface data I/O.
134	IO11	В	These pins have built-in pull-up resistors.
135	IO10	В	
136	IO9	В	
137	IO8	В	
138	V <sub>SS0</sub>	Р	
139	IO7	В	
140	IO6	В	ATADI data I/O
141	IO5	В	ATAPI data I/O.
142	104	В	These pins have built-in pull-up resistors.
143	IO3	В	
144	V <sub>DD</sub>	Р	
	1 ,00		

- Unused ("NC") pins must be left open.
  Pins whose name is under a bar operate with inverted (negative) logic.
  V<sub>SS0</sub> is the logic system ground and V<sub>SS1</sub> is the SCSI interface driver ground.
  Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of November, 1999. Specifications and information herein are subject to change without notice.