Ordering number : ENN 6891

CMOS IC

LC896431

MD Decoder IC

Overview

The LC896431 implements playback signal processing that conforms to the MiniDisc format standards. This device was designed to form a chip set in conjunction with a SANYO RF amplifier IC.

Features

- Fabricated in a CMOS process for low power
- An application system can be created easily by combining this IC with a SANYO RF amplifier IC.
- Provides digital servo functions and a VCEC for high-speed access.
- Allows the creation of optimal systems by integrating 8× oversampling digital filters, a 1-bit D/A converter, and a low-pass filter on the same chip.

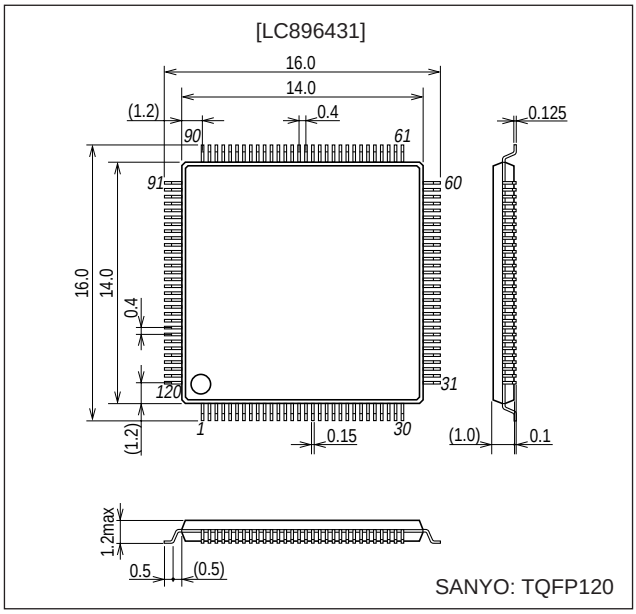
Functions

- Full complement of automatic adjustment functions
- Intensity, defect, and shock detection
- Both CLV and CAV control
- VCEC circuit
- Automatic adjustment functions
- High-performance ATRAC3 decoder
- EFM data demodulation
- Error detection and correction (C1: E12, C2: E24)
- Error correction RAM
- Intelligent commands
- Anti-shock control
- ADIP demodulation and decoding
- Digital servo
- EFM ACIRC decoding
- High-performance 1-bit D/A converter
- Built-in second-order low-pass filter for audio output
- Power saving function for the stopped and paused states

Package Dimensions

unit: mm

3257-TQFP120



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Specifications

Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD1} max		2.7	V
	V_{DD2} max		2.7	V
Input and output voltage	V_I, V_O		0 to V_{DD2}	V
Operating temperature *1	Topr		–10 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Input and output current *2	I_I, I_O		±20	mA

Notes: 1. Does not guarantee continuous operation.
2. Maximum output current that flows constantly (except OUTL, OUTR, SLC0, PD0 pins)

Allowable Operating Ranges at Ta = –10°C to +70°C, V_{SS} = 0 V

In case of external I/O power supply, V_{DD2} = 2.3 V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	External I/O	V_{DD2}		2.2	2.3	2.4	V
	Internal	V_{DD}		1.5	1.6	1.8	
	Analog system	AV_{DD}		2.2	—	2.6	
		AV_{DD1}		2.2	—	2.6	
		VCV_{DD}		2.2	—	2.6	

In case of external I/O power supply, V_{DD2} = 2.5 V

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	External I/O	V_{DD2}		2.2	2.5	2.55	V
	Internal	V_{DD}		1.55	1.6	1.80	
	Analog system	AV_{DD}		2.2	—	2.6	
		AV_{DD1}		2.2	—	2.6	
		VCV_{DD}		2.2	—	2.6	

Notes: 1. Supply all power supplies at less than the maximum gradient of 0.4 V/ms, and implement a delay of 10 ms or longer for current to go from 0 V to 2.4 V.
2. Supply all power supplies simultaneously so that there are no delay differences among them.
3. Supply 0 to the RESETB pin only upon power application, and following power application, supply 1 and use with this value.

Electrical Characteristics

DC characteristics

Input/output level: at Ta = –10 to 70°C, V_{SS} = 0 V, V_{DD1} = 1.5 to 1.8 V, V_{DD2} = 2.2 to 2.55 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	Except *1 to *3	$V_{DD2} \times 0.75$	—	—	V
		*1	$V_{DD2} \times 0.80$	—	—	
		*2	$V_{DD2}/2 + 0.10$	—	V_{DD2}	
Input low-level voltage	V_{IL}	Except *1 to *3	—	—	$V_{DD2} \times 0.25$	V
		*1	—	—	$V_{DD2} \times 0.20$	
		*2	V_{SS}	—	$V_{DD2}/2 - 0.10$	
Output high-level voltage	V_{OH}	I_{OH2} = –1 mA, Except *4	$V_{DD2} \times 0.80$	—	—	V
Output low-level voltage	V_{OL}	I_{OL} = 1 mA, Except *4	—	—	$V_{DD2} \times 0.15$	V
Output leakage current	I_{OZ}	*5	–10.0	—	10.0	µA
Pull-up resistance	R_{UP}		46	100	270	kΩ

Notes: *1: CL, CE, RESETB, ADIPWO, HFL
*2: EFMIN
*3: PEAK, BOTTOM, ABCD, TE, FE, VC
*4: OUTL, OUTR
*5: During high-impedance output. Current also flows through pull-up resistance for MD3 to 0.
• XIN, XOUT, SLC0, and PD0 are not included in DC characteristics.
• The FR, ISET, SLCIST bias resistance pins are not included in DC characteristics.

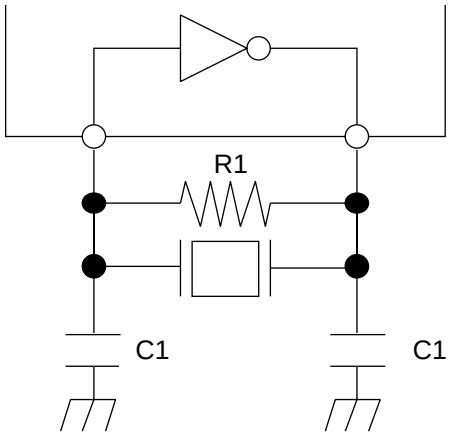
Analog characteristics

Input/output level: at Ta = –10 to +70°C, V_{SS} = 0 V, V_{DD1} = 2.2 to 2.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Analog input voltage	V_I	PEAK, BOTTOM, ABCD, TE, FE, VC	$AV_{DD1} \times 0.2$	—	$AV_{DD1} \times 0.8$	V
Input load capacitance		PEAK, BOTTOM, ABCD, TE, FE, VC	—	—	7.5	pF

Oscillation amplifier

Note: Xtal is limited to the basic mode.



Pin Functions

I/O → I: Input pin, O: Output pin, B: Bidirectional pin

Note: Do not leave V_{DD} and V_{SS} open, connect all to power supply, ground.

Pin No.	Pin Name	I/O	Function
1	V_{DD2}	—	Power supply pin
2	SHOCK	O	SHOCK/RFNG output pin
3	SLCO	O	HF signal slice level output pin
4	SLCIST	I	Bias resistance pin of slice level adjustment amplifier
5	EFMIN	I	HF signal input pin
6	RESETB	I	System reset
7	HFL	I	Track detection signal input pin
8	TEST2	I	Test input pin
9	PDO	O	VCEC current charge pump output pin
10	VCV_{SS}	—	VCEC ground pin
11	FR	I	Bias resistance pin for oscillation frequency of VCEC
12	ISET	I	Bias resistance pin for current charge pump of VCEC
13	VCV_{DD}	—	VCEC power supply pin
14	AV_{SS1}	—	Digital servo ground pin
15	PEAK	I	PEAK signal input pin
16	BOTTOM	I	BOTTOM signal input pin
17	ABCD	I	Main beam light intensity signal input pin
18	TE	I	Tracking error signal input pin
19	FE	I	Focus error signal input pin
20	VC	I	Midpoint potential input pin
21	AV_{DD1}	—	Digital servo power supply pin
22	DSW1	B*	Disk mode switch output
23	DSW0	B*	Disk mode switch output
24	SGC	B*	AGC control signal output pin
25	AOFFSET	B*	ABCD offset control signal output pin
26	FOFFSET	B*	Focus offset control signal output pin
27	TOFFSET	B*	Tracking offset control signal output pin
28	TBAL	B*	Tracking balance control signal output pin
29	LDREF	B*	Laser control signal output pin
30	V_{SS}	—	Ground pin
31	V_{DD}	—	Internal power supply pin
32	FBAL	B*	Focus balance control output pin
33	SPPWMF	B*	Spindle PWM output pin
34	SPPWMR	B*	Spindle PWM output pin
35	MD7	B	DRAM data input/output pin
36	MD6	B	DRAM data input/output pin
37	MD5	B	DRAM data input/output pin
38	MD4	B	DRAM data input/output pin
39	V_{DD2}	—	Power supply pin
40	MD3	B	DRAM data input/output pin
41	MD2	B	DRAM data input/output pin
42	MD1	B	DRAM data input/output pin
43	MD0	B	DRAM data input/output pin
44	PCK	O	VCEC system clock signal output pin
45	V_{DD2}	—	Power supply pin
46	V_{SS}	—	Ground pin
47	DEFECT	B*	Defect signal input/output pin
48	MD15	B	DRAM data input/output pin
49	MD14	B	DRAM data input/output pin
50	MD13	B	DRAM data input/output pin
51	MD12	B	DRAM data input/output pin
52	V_{SS}	—	Ground pin
53	MD11	B	DRAM data input/output pin

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Pin No.	Pin Name	I/O	Function
54	MD10	B	DRAM data input/output pin
55	MD9	B	DRAM data input/output pin
56	MD8	B	DRAM data input/output pin
57	SLPWMF	B*	Sled PWM output pin
58	SLPWMR	B*	Sled PWM output pin
59	SLD0	B*	Sled control signal output pin
60	V_{SS}	—	Ground pin
61	V_{DD2}	—	Power supply pin
62	SLD1	B	Sled control signal input/output pin
63	V_{DD}	—	Internal power supply pin
64	SLD2	I	Sled control signal input pin
65	SLD3	I	Sled control signal input pin
66	FOPWMF	B*	Focus PWM output pin
67	FOPWMR	B*	Focus PWM output pin
68	TRPWMF	B*	Tracking PWM output pin
69	TRPWMR	B*	Tracking PWM output pin
70	FG	I	Speed pulse input pin
71	VP	B*	CLV servo lock judgment output pin
72	FOK	B*	Focus OK signal output pin
73	FAST	B*	FAST signal output pin
74	CL	I	CPU interface data transfer clock input pin
75	CE	I	CPU interface chip enable signal input pin
76	DI	I	CPU interface data input pin
77	DO	O	CPU interface data output pin
78	WRQB	O	CPU interface interrupt signal output pin
79	INTB	O	CPU interface interrupt signal output pin
80	FSEQ	B*	Frame synchronization detection signal output pin
81	F16M	B*	16.9344 MHz output pin
82	ENH	B*	De-emphasis specification output pin
83	LRCO	B*	LR clock output pin
84	DDATA	B*	Speech signal data output pin
85	BCO	B*	Bit clock output pin
86	DDOUT (DEFECT)	B*	Digital audio output pin
87	V_{DD2}	—	Power supply pin
88	XIN	I	16.9344 MHz oscillation input pin
89	XOUT	O	16.9344 MHz oscillation output pin
90	V_{SS}	—	Ground pin
91	V_{DD}	—	Internal power supply pin
92	AV_{SS}	—	1-bit DAC ground pin
93	OUTR	O	1-bit DAC right channel output pin
94	OUTL	O	1-bit DAC left channel output pin
95	AV_{DD}	—	1-bit DAC power supply pin
96	MCASB	B*	DRAM $\overline{CAS}$ signal output pin
97	MOEB	B*	DRAM $\overline{OE}$ signal output pin
98	MAD9	B*	DRAM address output pin
99	MAD8	B*	DRAM address output pin
100	MAD7	B*	DRAM address output pin
101	TEST1	I	Test input pin
102	MAD6	B*	DRAM address output pin
103	MAD5	B*	DRAM address output pin
104	MAD4	B*	DRAM address output pin
105	TEST3	I	Test input pin
106	V_{SS}	—	Ground pin
107	V_{DD2}	—	Power supply pin
108	SMON3	B*	Monitor signal output pin
109	SMON2	B*	Monitor signal output pin

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Pin No.	Pin Name	I/O	Function
110	MAD3	B*	DRAM address output pin
111	MAD2	B*	DRAM address output pin
112	MAD1	B*	DRAM address output pin
113	MAD0	B*	DRAM address output pin
114	SMON1	B*	Monitor signal output pin
115	SMON0	B*	Monitor signal output pin
116	MRASB	B*	DRAM $\overline{RAS}$ signal output pin
117	MWEB	B*	DRAM $\overline{WE}$ signal output pin
118	ADIPWO	I	Wobble signal input pin
119	V_{DD}	—	Internal power supply pin
120	V_{SS}	—	Ground pin

Note: * Output/input only during testing. Normally output.
TEST1 to TEST3: Always use fixed to High.
MD3 to MD0: Pull-up I/O with resistor