

40× CD-ROM Decoder with SCSI Interface

Functions

- CD-ROM ECC function
- SCSI I/F function
- · Subcode I/F function
- · CAV audio function

Features

- SCSI interface (includes on-chip SCAM selection register)
- Supports 20× speed and a 10 MBytes/s transfer rate when using 16-bit 70-ns EDO DRAM
- Supports 40× speed and a 10 MB/s transfer rate when using 16-bit 50-ns EDO DRAM
- Up to 4 M bits of buffer RAM can be used.
- The user can freely set up the CD main channel and the C2 flag areas in buffer RAM.
- Batch transfer function (Allows the CD main channel, the C2 flags, and other data to be sent in a single operation.)
- Multi-block transfer function (Allows multiple blocks to be sent automatically in a single operation.)
- Subcode buffering and CD-TEXT support

Specifications

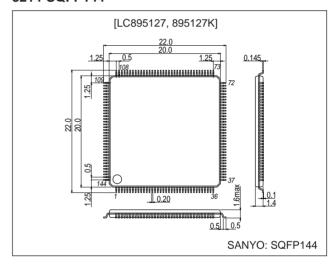
Absolute Maximum Ratings at $V_{SS} = 0 \text{ V}$

- CAV audio function
- Supports 20 MBytes/s transfers
- Package: SQFP-144

Package Dimensions

unit: mm

3214-SQFP144



Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} max	Ta = 25°C	-0.3 to +7.0	V
Input/output voltage	V _I , V _O	Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	550	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-55 to +125	°C
Soldering temperature (pin part only)		10 s	260	°C

Allowable Operating Ranges at Ta = -30° C to $+70^{\circ}$ C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
Farameter		Conditions	min	typ	max	Onit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V _{IN}		0		V_{DD}	V

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DC Characteristics at $Ta=-30~to~+70^{\circ}C,~V_{SS}=0~V,~V_{DD}=4.5~to~5.5~V$

Dorometer	Cumbal	Conditions	Appliaghla ping		Ratings		Unit
Parameter	Symbol	Conditions	Applicable pins	min	typ	max	Unit
Input high-level voltage	V _{IH1}	TTL levels	(4)	2.2			V
Input low-level voltage	V _{IL1}	1 I L levels	(1)			0.8	V
Input high-level voltage	V _{IH2}	TTL levels	(9)	2.2	_	_	V
Input low-level voltage	V _{IL2}	with pull-up resistor	(9)	_	_	0.8	V
Input high-level voltage	V _{IH3}	TTL levels	(2)	2.2	_	_	V
Input low-level voltage	V _{IL3}	Schmitt	(2)	_	_	0.8	V
Input high-level voltage	V _{IH4}	CMOS levels	(2)	0.8 V _{DD}	_	_	V
Input low-level voltage	V _{IL4}	Schmitt	(3)	_	_	0.2 V _{DD}	V
Input high-level voltage	V _{IH5}		(4) (9) (10)	2.0		_	V
Input low-level voltage	V _{IL5}		(4), (8), (10)			0.8	V
Input high-level voltage	V _{IH2}	TTL levels	(44)	2.2		_	V
Input low-level voltage	V _{IL2}	with pull-up resistor	(11)	_	_	0.8	V
Output high-level voltage	V _{OH1}	I _{OH1} = -12 mA	(6)	V _{DD} – 2.1	_	_	V
Output low-level voltage	V _{OL1}	I _{OL1} = 12 mA	(6)	_	_	0.4	V
Output high-level voltage	V _{OH2}	I _{OH2} = -8 mA	(7)	2.4			V
Output low-level voltage	V _{OL2}	I _{OL2} = 8 mA				0.4	V
Output high-level voltage	V _{OH2}	I _{OH2} = -2 mA	(O) (E) (11)	2.4			V
Output low-level voltage	V _{OL2}	I _{OL2} = 2 mA	(9), (5), (11)			0.4	V
Output low-level voltage	V _{OL4}	I _{OL4} = 48 mA	(10)			0.4	V
Input leakage current	I _{IL}	$V_I = V_{SS}, V_{DD}$	All input pins	-25		+25	μA
Pull-up resistance	R _{UP}		(5), (9), (11)	60	120	240	kΩ

Applicable pin sets are as follows.

INPUT

- (1) TEST0 to TEST4, CSCTRL, SUA0 to SUA6, C2P0, SDATA, BCK, LRCK, SCOR, WFCK, SBS0, MCK2SEL
- (2) RESET
- (3) \overline{CS} , \overline{RD} , \overline{WR}
- (4) SCSISEL, XTALSEL

OUTPUT

- (5) $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$
- (6) MCK
- (7) EXCK, DSDATA, DLRCK, DBCK, \overline{RASO} , \overline{CASO} , \overline{CASO} , \overline{OE} , \overline{UWE} , \overline{LWE} , RA0 to RA8

INOUT

- (8) ACK, ATN
- (9) D0 to D7, IO0 to IO15, IOP0 to IOP7
- (10) $\overline{DB0}$ to $\overline{DB7}$, \overline{DBP} , \overline{BSY} , I/O, \overline{MSG} , \overline{SEL} , \overline{RST} , \overline{REQ} , C/D
- (11) IOP0 to IOP7

Note: Pins XTAL0, XTALCK0, XTAL1, XTALCK1, and X1EN are not included in DC characteristics.

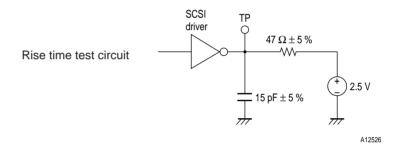
SCSI Pin Input Characteristics

Parameter	Symbol Conditions		Ratings			Unit
raianietei	Symbol	Conditions	min	typ	max	Offic
Input threshold voltage	V _{t+t1}	V - 450 to 5 50 V		1.60	2.00	V
Input theshold voltage	V _{t-t1}	V _{DD} = 4.50 to 5.50 V	0.80	1.10		V
Hysteresis width	ΔV_{tt1}	V _{DD} = 5.0 V	0.41	0.5		V

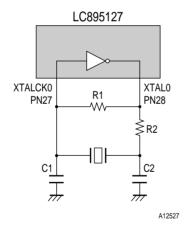
Active-Low Output Characteristics

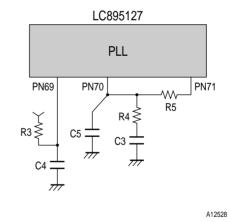
Parameter	Symbol	Conditions		Ratings	Unit	
Falameter	Symbol	TIDOI CONDITIONS		typ		max
Output high-level voltage	V _{OH}		2.5			V
Output low-level voltage	V _{OL}				0.4	V

Note: Only applies to the active-low output pins $\overline{\mathsf{DB0}}$ to $\overline{\mathsf{DB7}}$, $\overline{\mathsf{REQ}}$, $\overline{\mathsf{DBPB}}$



Recommended Oscillator and PLL Circuits





 $R1 = 120 \text{ k}\Omega, R2 = 47 \Omega, C1 = 30 \text{ pF}$

Crystal oscillator frequency XTALCK0 = 16.9344 MHz

$$R3=7.5~k\Omega,\,R4=200~\Omega,\,R5=10~k\Omega,\,C3=0.1~\mu F$$

 $C4 = 0.1 \ \mu F, C5 = 0.002 \ \mu F \ to \ 0.01 \ \mu F$

Note: The values listed above for R3, R4, R5, and C3 also apply when the XTALKC0 frequency is 33.8688 MHz.

Applications must be designed so that the analog V_{DD} and V_{SS} power supply system is completely independent of the logic system power supply and is not affected by the logic system power supply fluctuation in any way.

Note: Since the exact values of these components will vary depending on the characteristics of the printed circuit board used and other factors, consult the manufacturer of the crystal element when designing the oscillator circuit.

Pin Functions

			Туре		
1	INPUT	В	BIDIRECTION	NC	NOT CONNECT
0	OUTPUT	Р	POWER		

Pin No.	Pin name	Туре	Pin functions	
1	V _{SS0}	Р		
2	102	В	D # DAM + 1/0	
3	IO1	В	Buffer RAM data I/O	
4	100	В	These pins have built-in pull-up resistors.	
5	MCK2SEL	I	PLL frequency selection. Currently, this pin must be connected to V _{DD} .	
6	C2PO	ı		
7	SDATA	ı		
8	BCK	ı	CD DSP interface	
9	LRCK	1		
10	EXCK	0	Subcode I/O	
11	WFCK	1		
12	SBSO	ı	Outro de I/O	
13	SCOR	I	Subcode I/O	
14	DSDATA	0		
15	DLRCK	0	D/A converter outputs	
16	DBCK	0		
17	MCK	0	XTALCLK0 1/1, 1/2, and stop output	
18	V_{DD}	Р		
19	V _{SS0}	Р		
20	RESET	I	IC reset. The IC is reset on a low-level input	
21	CSCTRL	I	MC (Microcontroller) CSL ₀ , Hi	
22	TEST3	I		
23	TEST0	I	Tost pine. These pine must be connected to V in normal appraisin	
24	TEST1	I	Test pins. These pins must be connected to V _{SS0} in normal operation.	
25	TEST2	I		
26	V _{SS0}	Р		
27	XTALCK0	I	Crystal oscillator circuit input	
28	XTAL0	0	Crystal oscillator circuit output	
29	TEST4	I	Test pin. This pin must be connected to V _{SS0} in normal operation.	
30	V _{SS0}	Р		
31	V _{SS0}	Р		
32	V _{SS0}	Р		
33	V _{SS0}	Р		
34	IOP7	I	General-purpose I/O ports. These pins include built-in pull-up resistors.	
35	IOP6	I	Constant purposed to perior rivous pine instance built in pull up residents.	
36	V _{SS0}	Р		
37	V _{DD}	Р		
38	IOP5	I		
39	IOP4	I		
40	IOP3	I	General-purpose I/O ports. These pins include built-in pull-up resistors.	
41	IOP2	I	22 parpose no person moses parlo moses bank in pain ap rediction.	
42	IOP1	I		
43	IOP0	I		
44	V _{SS0}	Р		
45	RD	I	Microcontroller data read signal input	
46	WR	I	Microcontroller data write signal input	
47	CS	I	Register chip select input from the microcontroller	
48	SUA0	I		
49	SUA1	I		
50	SUA2	I	Microcontroller register selection signals	
51	SUA3	I		
52	SUA4	I		
53	SUA5	I	Continued on payt page	

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Pin No.	Pin	I/O	Function
54	V_{DD}	Р	
55	V _{SS0}	Р	
56	SUA6	I	Microcontroller register selection signals
57	D0	В	
58	D1	В	
59	D2	В	Migroportrollor data signala
60	D3	В	Microcontroller data signals
61	D4	В	
62	D5	В	
63	V_{SS0}	Р	
64	D6	В	Microcontroller data signals
65	D7	В	Microcontroller data signals
66	ĪNT0	0	Interrupt request signal output to the microcontroller (ECC side. Set by setting a register value.)
67	ĪNT1	0	Interrupt request signal output to the microcontroller (SCSI side. Set by setting a register value.)
68	SWAIT	0	Wait signal output to the microcontroller
69	X1EN	I	Used by the PLL. This pin must be connected to V _{DD} through a resistor.
70	XTALCK1	I	Used by the PLL.
71	XTAL1	0	Used by the PLL.
72	V _{SS0}	Р	Analog V _{SS}
73	V_{DD}	Р	Analog V _{DD}
74		NC	
75	I/O	В	SCSI interface
76	REQ	В	OGG III.Ondo
77	V _{SS1}	Р	
78	C/D	В	SCSI interface
79	SEL	В	
80		NC	
81	V _{DD}	Р	
82	V _{SS1}	Р	
83	MSG	В	SCSI interface
84	RST	В	
85	V _{SS1}	P	
86	ĀCK	В	SCSI interface
87	BSY	В	
88	V _{SS1}	В	
89	ĀTN	В	SCSI interface
90	V _{DD}	P P	
91	V _{SS1}	NC NC	
92	DBP	B	SCSI interface
93	V _{DD}	Ь	OODI III.GIIAUC
95	DB7	В	
95	DB7	В	SCSI interface
97	V _{SS1}	Р	
98	DB5	В	
99	DB3 DB4	В	SCSI interface
100	V _{DD}	P	
101	DB3	В	
102	DB2	В	SCSI interface
103	V _{SS1}	P	
104	DB1	В	
105	DBO	В	SCSI interface
106	SCSISEL	ı	SCSI pin layout selection. (This pin must be connected to V _{SS0} .)
107	XTALSEL	ı	PLL XTAL oscillator selection
		· ·	

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Pin No.	Pin	I/O	Function
108	V _{SS1}	Р	
109	V_{DD}	Р	
110	V _{SS0}	Р	
111	RAS0	0	Buffer RAM RAS signal output 0
112	V_{DD}	Р	
113	CAS0	0	Buffer RAM CAS signal output 0 (Normally held fixed at 0 (low).)
114	CAS1	0	Buffer RAM RAS signal output 1
115	ŌĒ	0	Buffer RAM output enable
116	UWE (RA9)	0	Buffer RAM upper write enable (RA9 when 8M or more DRAM is used.)
117	LWE	0	Buffer RAM lower write enable
118	V _{SS0}	Р	
119	RA0	0	
120	RA1	0	
121	RA2	0	
122	RA3	0	Buffer RAM address signal outputs
123	RA4	0	
124	RA5	0	
125	RA6	0	
126	V_{DD}	Р	
127	V _{SS0}	Р	
128	RA7	0	D. (C. DAM . I.)
129	RA8	0	Buffer RAM address signal outputs
130	IO15	В	
131	IO14	В	
132	IO13	В	
133	IO12	В	Buffer RAM data I/O
134	IO11	В	These pins have built-in pull-up resistors.
135	IO10	В	
136	109	В	
137	IO8	В	
138	V _{SS0}	Р	
139	107	В	
140	IO6	В]
141	IO5	В	Buffer RAM data I/O
142	IO4	В	These pins have built-in pull-up resistors.
143	IO3	В	
144	V_{DD}	Р	

Unused ("NC") pins must be left open.

Pins whose name is under a bar operate with inverted (negative) logic.

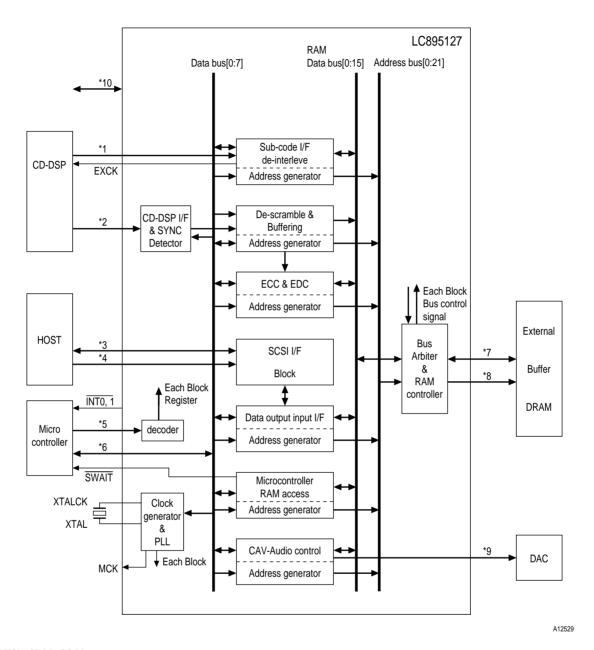
V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface driver ground.

If DRAM is used, applications must adopt measures to prevent undershoot and other DRAM problems. Such measures include inserting resistors in the RAS

and CAS lines and inserting capacitors between V_{SS} pins.

See the article on Designing with the Latest Microcontrollers and Memory in special issue number 25 of Transistor Technology for details on these measures. Since this device includes buffers that sink a current of 48 mA, applications must take adequate noise prevention measures.

Block Diagram



- *1 WFCK, SBSO, SCOR
- *2 BCK, SDATA, LRCK, C2PO
- *3 $\overline{DB0}$ to $\overline{DB7}$, \overline{DBP} , \overline{BSY} , \overline{MSG} , \overline{SEL} , \overline{RST} , \overline{REQ} , I/O, C/D
- *4 ACK, ATN
- *5 RD, WR, SUA0 to SUA6, ZCS, CSCTRL
- *6 D0 to D7
- *7 IO0 to IO15
- *8 RA0 to RA10, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, \overline{OE} , \overline{UWE} , \overline{LWE}
- *9 DBCK, DLRCK, DSDATA
- *10 IOP7 to IOP0

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