Ordering number: EN *5585

CMOS LSI

# LC86P4564

## One-time PROM built-in 8-bit Single Chip Microcontroller

## Preliminary



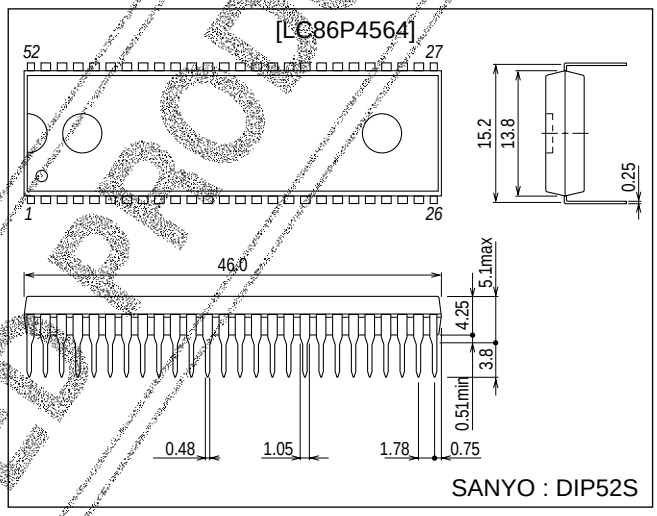
## Overview

The LC86P4564 is a CMOS 8-bit single chip microcontroller with One-time PROM for the LC864500 series.
This microcontroller has the function and the pin assignment identical to those of the LC864500 series mask ROM version, and has the built-in 64K-byte PROM.

## Package Dimensions

unit : mm

**3128-DIP52S**




## Features

(1) Options switchable by PROM data
The option functions of the LC864500 series can be specified by the PROM data.
The functions of the trial pieces can be evaluated using mass production board.

(2) Internal PROM capacity : 65512 bytes (For program)
8192 × 12 bits (For character)

(3) Internal RAM capacity : 256 bytes
The LC86P4564 contains a 65512-byte PROM and a 256-byte RAM. Each size is the maximum capacity of the LC86P4564 mask-ROM series.

| Mask ROM version | PROM capacity | RAM capacity |
|---|---|---|
| LC864532 | 32768 bytes | 256 bytes |
| LC864528 | 28672 bytes | 256 bytes |
| LC864524 | 24576 bytes | 256 bytes |
| LC864520 | 20480 bytes | 256 bytes |
| LC864516 | 16384 bytes | 256 bytes |
| LC864512 | 12288 bytes | 256 bytes |
| LC864508 | 8192 bytes | 256 bytes |

(4) Operating supply voltage : 4.5 V to 5.5 V
(5) Instruction cycle time : 1.0 µs to 366 µs
(6) Operating temperature : –30°C to +70°C
(7) The pin and the package compatible with the LC864500 series mask ROM version
(8) Applicable mask ROM version : LC864532/LC864528/LC864524/LC864520/LC864516/LC864512/LC864508
(9) Factory shipment : DIP52S

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Usage Notes

When using, take note of the followings.

(1) Differences between the LC86P4564 and the LC864500 series

| Item | LC86P4564 | LC864532/28/24/20/16/12/08 |
|---|---|---|
| Operation after reset releasing | The option must be set internally within 3 ms after a high-level signal is applied to the reset terminal. In this period options are switched gradually, and after that, the program is executed from 00H of the program counter. | The program is executed from 00H of the program counter as soon as a high-level signal is applied to the reset terminal. |
| Operating supply voltage range ($V_{DD}$) | 4.5 V to 5.5 V | 2.5 V to 6.0 V |
| Current drain under normal operation | Refer to 'electrical characteristics' on the semiconductor news. | |

Port format of the LC86P4564 during the reset is identical to that of the LC864532/28/24/20/16/12/08.
The LC86P4564 uses 256-byte spaces addressed 0FF00H to 0FFFH in the program memory to set options. In this way, all options of the LC864500 series cannot be executed.
Some of the LC864500 series options, which the LC86P4564 can support are as shown in the table below.

• LC86P4564 options

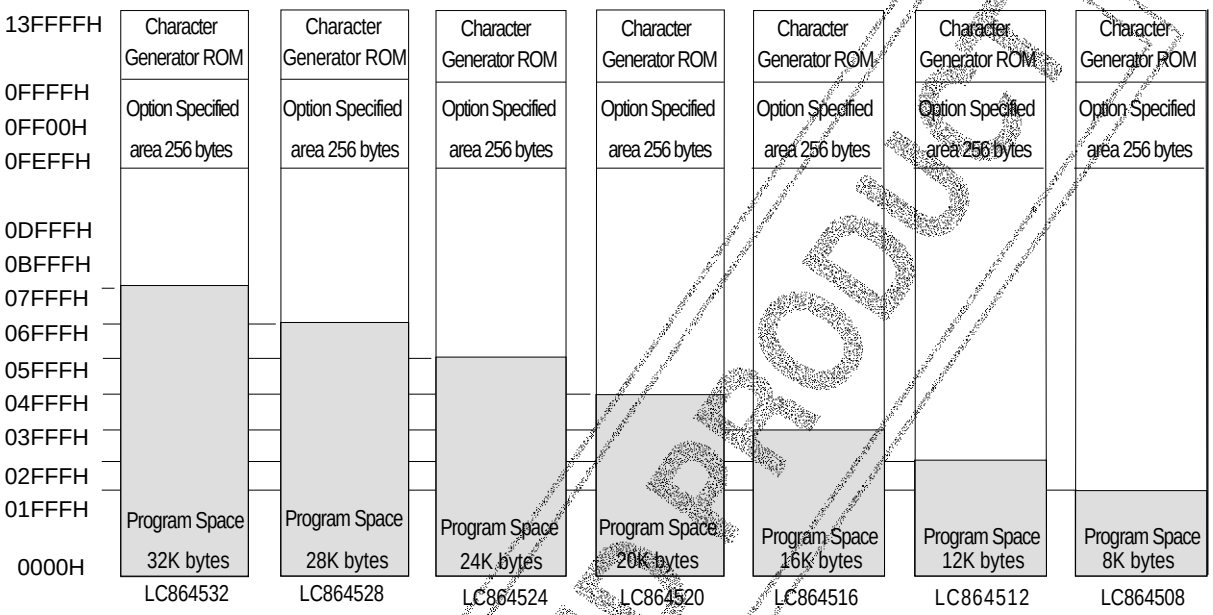
| Option types | Pins, circuits | Contents of the option |
|---|---|---|
| Input/output specifications of input/output ports | Port 0 | 1. N-channel open-drain output<br>2. CMOS output *1 |
| | | 1. Pull-up MOS transistor provided<br>2. Pull-up MOS transistor not provided *2 |
| | Port 1 *1 | 1. Input : Programmable pull-up MOS transistor<br>Output : N-channel open drain<br>2. Input : Programmable pull-up MOS transistor<br>Output : CMOS |
| Pull-up MOS transistor of input port. | Port 7 *1 | 1. Pull-up MOS transistor not provided.<br>2. Pull-up MOS transistor provided. |

*1) Specified in bit units
*2) When the "CMOS output" is selected as an output format, the pull-up MOS transistor will be provided, and when the "n-channel open-drain output" is selected, the pull-up MOS transistor will not be provided.

(2) Option setting program
The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

(3) ROM space

The LC86P4564 and LC864500 series use 256 bytes addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. The program memory capacity of the series is 65280 bytes addressed on 0000H to 0FEFFH. Note that the capacity of the LC86P4564 user-available PROM is 32768 bytes addressed on 0000H to 7FFFH, because the maximum ROM capacity of the LC864500 series ROM version is 32 K byte.



## How to Use

(1) Create a programming data for LC86P4564
Programming data for PROM of the LC86P4564 is required.
Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P4564.

(2) How to program for the PROM
The LC86P4564 can be programmed by the general purpose EPROM programmer with an attachment : W86EP4564D.

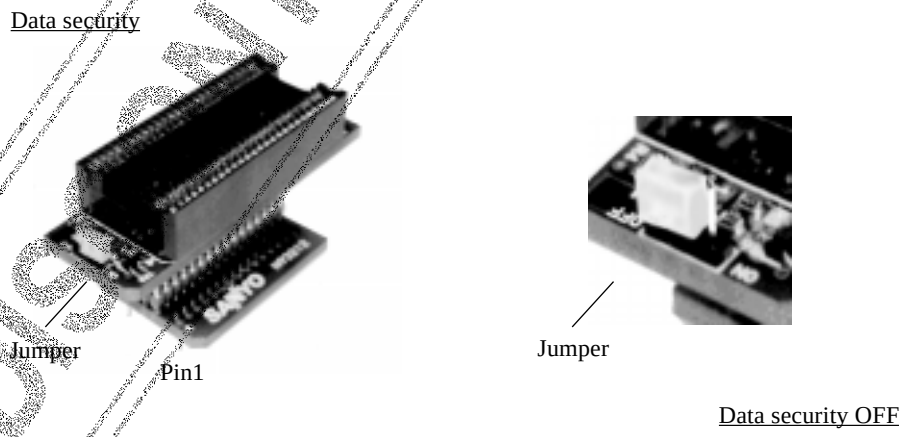
• Recommended EPROM programmers are as shown in the table below.

| Manufacturer | EPROM programmer |
|---|---|
| Advantest | R4945, R4944 |
| Andou | AF-9704 |
| AVAL | PKW-1100, PKW-3000 |
| Minato electronics | MODEL1890A |

• The "27010 (Vp-p = 12.5 V) Intel high speed programming" mode requires to be used for writing. The storage area addressed "0 to 13FFFH" requires to be selected for address setting and the jumper (DASEC) must be set to 'OFF' at programming.

(3) How to use the data security function
"Data security" is the function to prevent the EPROM data from being read out.
The following is the process in order to execute the data security.
1. Set the jumper of attachment 'ON'.
2. Program again. The EPROM programmer will display an error. The error indication means normal activity of the data security. It does not mean a trouble of the EPROM programmer or the LSI.

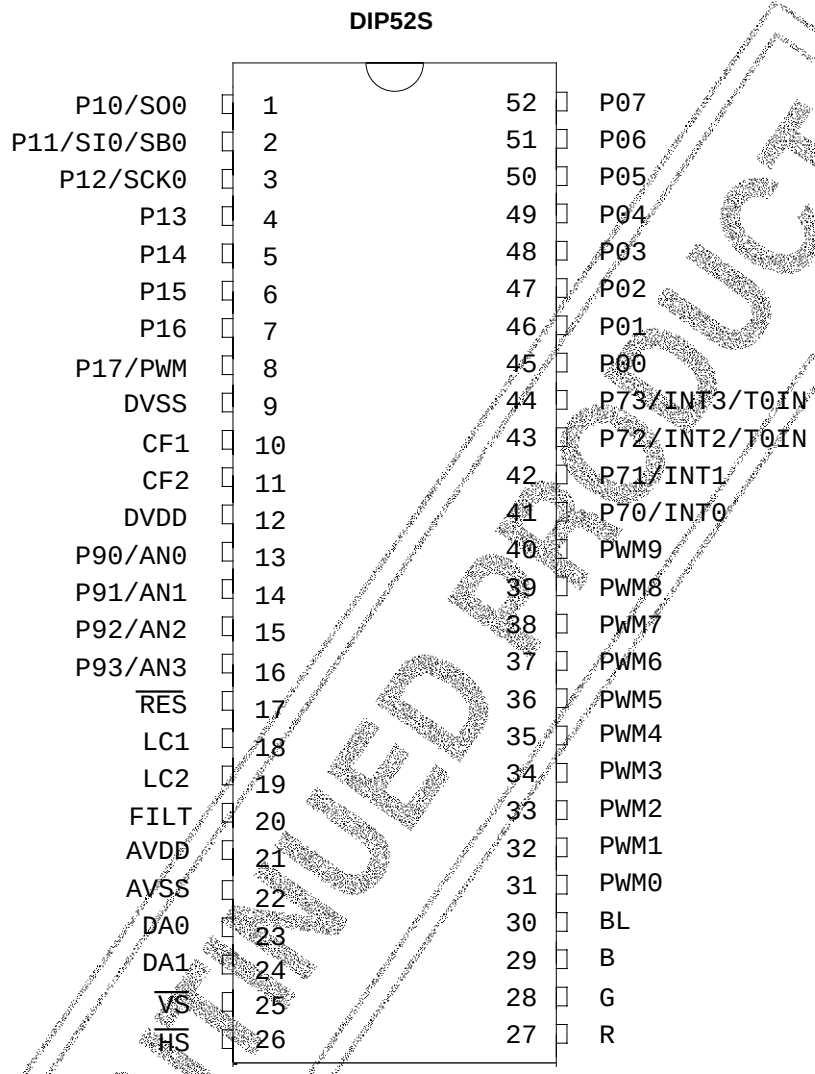
Notes
• Data security is not executed when the data of all address have 'FF' at sequence 2 above.
• Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at sequence 2 above.
• Set the jumper 'OFF' after executing the data security.




W86EP4564D

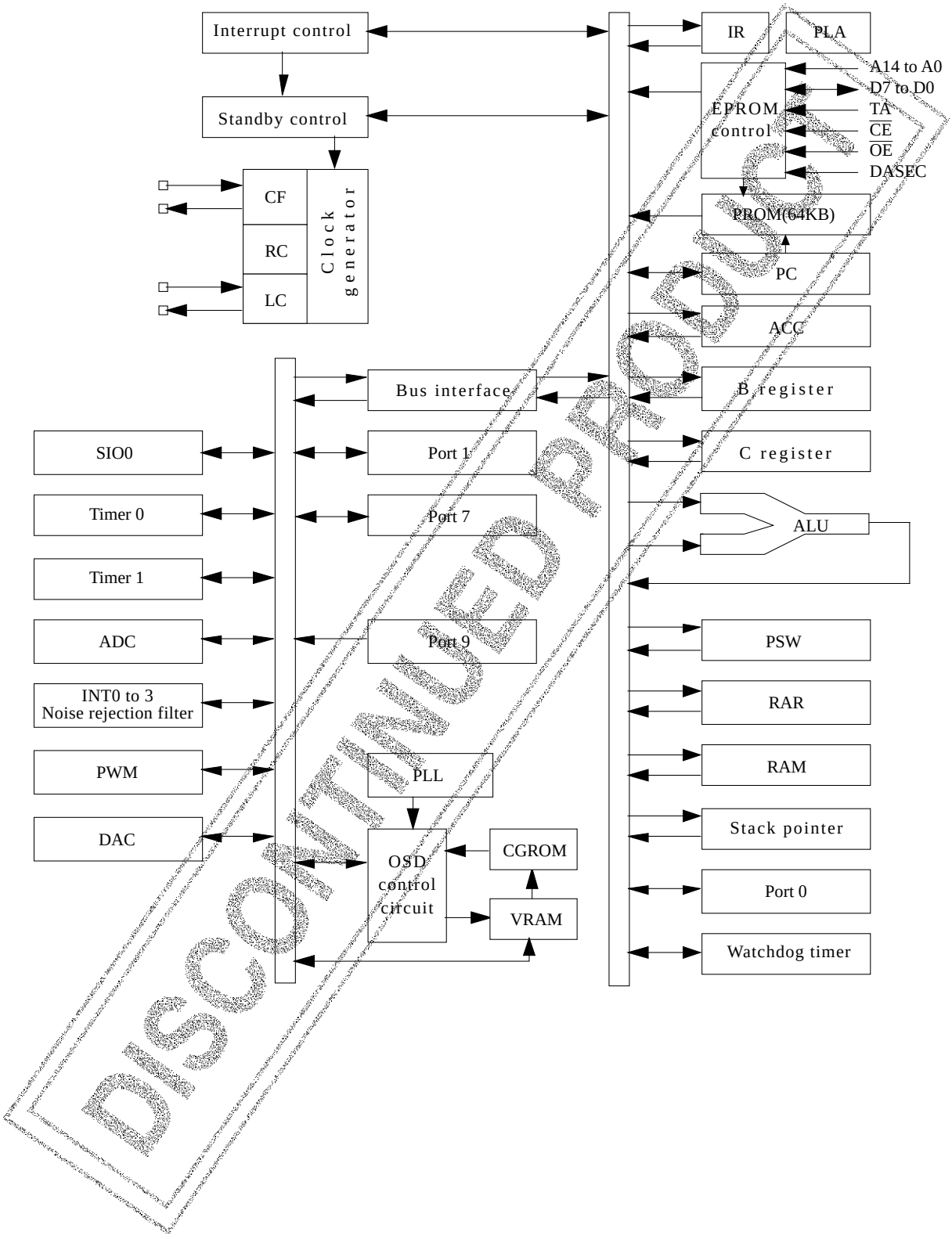
## Pin Assignment

DIP52S




Top view

## System Block Diagram



## Pin Description

Pin Description Table

| Pin name | Pin No. | I/O | Function description | Option | PROM mode |
|---|---|---|---|---|---|
| DVSS | 9 | — | Negative power supply for digital circuit | | |
| CF1 | 10 | I | Input for ceramic oscillator | | |
| CF2 | 11 | O | Output for ceramic oscillator | | |
| DVDD | 12 | — | Positive power supply for digital circuit | | |
| $\overline{RES}$ | 17 | I | Reset | | |
| LC1 | 18 | I | LC oscillation circuit input | | |
| LC2 | 19 | O | LC oscillation circuit output | | |
| FILT | 20 | O | Filter for PLL | | |
| AVDD | 21 | — | Positive power supply for analog circuit | | |
| AVSS | 22 | — | Negative power supply for analog circuit | | |
| DA0 | 23 | I/O | DA0 output/General purpose I/O port | | |
| DA1 | 24 | I/O | DA1 output/General purpose I/O port | | |
| $\overline{VS}$ | 25 | I | Vertical synchronization signal input | | |
| $\overline{HS}$ | 26 | I | Horizontal synchronization signal input | | |
| R | 27 | O | Red (R) output of RGB image output | | A4 (*1) |
| G | 28 | O | Green (G) output of RGB image output | | A5 (*1) |
| B | 29 | O | Blue (B) output of RGB image output | | A6 (*1) |
| BL | 30 | O | Fast blanking control signal<br>TV image signal or OSD image signal selecting | | A7 (*1) |
| PWM0 to PWM9 | 31 to 40 | O | PWM0 to PWM9 output<br>15V withstand | | PWM 0 to PWM 8 : A8 to A16 (*1)<br>PWM 9 : fixed to "L" |
| Port0<br>P00 to P07 | 45 to 52 | I/O | 8-bit Input/output port<br>Input/output can be specified in nibble units.<br>HOLD release input<br>Interrupt input | Pull-up resistor provided/not provided<br>Output Format CMOS/Nch-OD | |
| Port1<br>P10 to P17 | 1 to 8 | I/O | 8-bit Input/output port<br>Input/output can be specified in bit units.<br>Other functions<br>P10 SIO0 data output<br>P11 SIO0 data input /bus input/output<br>P12 SIO0 clock input/output<br>P17 Timer 1 (PWM) output | Output Format<br>CMOS/Nch-OD | D0 to D7 (*2) |

<table>
<tr><th>Terminal</th><th>No.</th><th>I/O</th><th>Function description</th><th>Option</th><th>PROM mode</th></tr>
<tr><td>Port7<br>P70<br>P71 to P73</td><td><br>41<br>42 to 44</td><td><br>I/O<br>I</td><td>4-bit input port<br>Other function<br>P70 INT0 input/HOLD release input/ n-ch transistor output for watchdog timer<br>P71 INT1 input/HOLD release input<br>P72 INT2 input/timer 0 event input<br>P73 INT3 input (noise rejection filter attached input/timer 0 event input<br>Interrupt receiver format vector address
<table>
<tr><th></th><th>Rise</th><th>Fall</th><th>Rise/Fall</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor provided/ not provided (in bit units)</td><td>P70 : VPP (*3)<br>P71 : DASEC (*4)<br>P72 : $\overline{OE}$ (*5)<br>P73 : $\overline{CE}$ (*6)</td></tr>
<tr><td>Port9<br>P90 to P93</td><td><br>13 to 16</td><td><br>I</td><td>4-bit input port<br>Other function<br>A/D converter input port (4 lines)</td><td></td><td>A0 to A3 (*1)</td></tr>
</table>

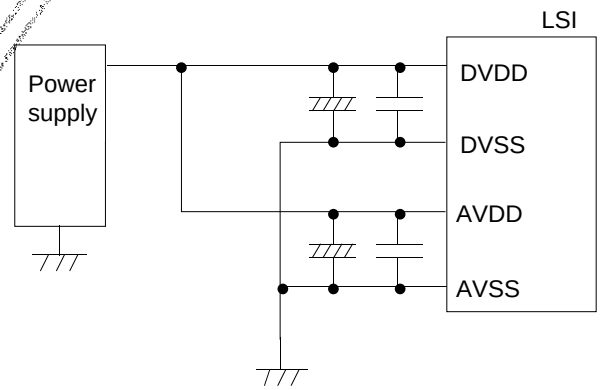
*1 An → Address input
*2 Data I/O
*3 Power for programming
*4 Memory select input/output for data security
*5 Output enable input
*6 Chip enable input

○ All of port options except the pull-up resistor option of Port 0 can be specified in bit units.
○ When the “CMOS output” is selected for port 0 as an output format, the pull-up resistor will be provided, and when the “n-channel open-drain output” is selected, the pull-up resistor will not be provided.
○ Whichever the “CMOS” or the “n-channel open-drain” output format is selected, the programmable pull-up resistor will be provided.

• Port states during reset

| Terminal | I/O | Pull-up resistor status at selecting pull-up option |
|---|---|---|
| Port 0 | Input | Pull-up resistor OFF, ON after reset release |
| Port 1 | Input | Programmable pull-up resistor OFF |
| Port 7 | Input | Fixed pull-up resistor provided |

* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the mutual noise influence.



# Specifications

## 1. Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | | Symbol | Pins | Conditions | $V_{DD}$[V] | Ratings min | typ | max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply voltage | | $V_{DD}$ max | DVDD, AVDD | DVDD = AVDD | | –0.3 | | +7.0 | V |
| Input voltage | | $V_I$ (1) | • P71, 72, 73<br>• Port 9<br>• $\overline{RES}$, $\overline{HS}$, $\overline{VS}$ | | | –0.3 | | $V_{DD}$+0.3 | |
| Output voltage | | $V_O$ (1) | R, G, B, BL, FILT | | | –0.3 | | $V_{DD}$+0.3 | |
| | | $V_O$ (2) | PWM0 to PWM9 | | | –0.3 | | +15 | |
| Input/output voltage | | $V_{IO}$ (1) | Ports 0, 1, P70<br>DA0, 1 | | | –0.3 | | $V_{DD}$+0.3 | |
| High-level output current | Peak output current | $I_{OPH}$ (1) | Ports 0, 1 | • Pull-up MOS transistor output<br>• At each pin | | –2 | | | mA |
| | | $I_{OPH}$ (2) | Ports 0, 1<br>DA0, 1 | • CMOS output<br>• At each pin | | –4 | | | |
| | | $I_{OPH}$ (3) | R, G, B, BL | • CMOS output<br>• At each pin | | –5 | | | |
| | Total output current | $\Sigma I_{OAH}$ (1) | Port 1 | The total of all pins | | –10 | | | |
| | | $\Sigma I_{OAH}$ (2) | Port 0 | The total of all pins | | –10 | | | |
| | | $\Sigma I_{OAH}$ (3) | R, G, B, BL | The total of all pins | | –15 | | | |
| Low-level output current | Peak output current | $I_{OPL}$ (1) | Ports 0, 1 DA0, 1 | At each pin | | | | 20 | |
| | | $I_{OPL}$ (2) | P70 | At each pin | | | | 30 | |
| | | $I_{OPL}$ (3) | • R, G, B, BL<br>• PWM0 to PWM9 | At each pin | | | | 5 | |
| | Total output current | $\Sigma I_{OAL}$ (1) | Port 0 | The total of all pins | | | | 40 | |
| | | $\Sigma I_{OAL}$ (2) | Port 1, P70 | The total of all pins | | | | 40 | |
| | | $\Sigma I_{OAL}$ (3) | R, G, B, BL | The total of all pins | | | | 15 | |
| | | $\Sigma I_{OAL}$ (4) | PWM0 to PWM9 | The total of all pins | | | | 30 | |
| Allowable power dissipation | | Pd max | DIP52S | Ta = –30 to +70°C | | | | 430 | mW |
| Operating temperature range | | Topr | | | | –30 | | +70 | °C |
| Storage temperature range | | Tstg | | | | –55 | | +150 | |

The same level voltage must be applied to both DVSS and AVSS. $V_{SS}$ = DVSS = AVSS
The same level voltage must be applied to both DVDD and AVDD. $V_{DD}$ = DVDD = AVDD

## 2. Allowable Operating Range at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$[V] | min | typ | max | |
| Operating supply voltage range | $V_{DD}$ | DVDD, AVDD | 0.98 µs ≤ tCYC tCYC ≤ 1.02 µs | | 4.5 | | 5.5 | V |
| Hold voltage | $V_{HD}$ | DVDD, AVDD | RAMs and the registers held at HOLD mode. | | 2.0 | | 5.5 | |
| High-level input voltage | $V_{IH}$(1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | 0.6$V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}$(2) | • Port 1 (Schmitt)<br>• P72, 73<br>• HS, VS | Output disable | 4.5 to 5.5 | 0.75$V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}$(3) | • P70 port input / interrupt<br>• P71<br>• RES (Schmitt) | Output n-channel transistor OFF | 4.5 to 5.5 | 0.75$V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}$(4) | P70 Watchdog timer input | Output n-channel transistor OFF | 4.5 to 5.5 | $V_{DD}$–0.5 | | $V_{DD}$ | |
| | $V_{IH}$(5) | Port 9 DA0, 1 port input | | 4.5 to 5.5 | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| Low-level input voltage | $V_{IL}$(1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | $V_{SS}$ | | 0.2$V_{DD}$ | |
| | $V_{IL}$(2) | • Port 1 (Schmitt)<br>• P72, 73<br>• HS, VS<br>• Port 9 | Output disable | 4.5 to 5.5 | $V_{SS}$ | | 0.25$V_{DD}$ | |
| | $V_{IL}$(3) | • P70 port input / interrupt<br>• P71<br>• RES (Schmitt) | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | 0.25$V_{DD}$ | |
| | $V_{IL}$(4) | P70 Watchdog timer input | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | 0.6$V_{DD}$ | |
| | $V_{IL}$(5) | Port 9 DA0, 1 Port input | | 4.5 to 5.5 | $V_{SS}$ | | 0.3$V_{DD}$ | |
| Operation cycle time | tCYC(1) | | OSD function | 4.5 to 5.5 | 0.98 | 1 | 1.02 | µs |
| | tCYC(2) | | No OSD function | 4.5 to 5.5 | 0.98 | | 30 | |

| Parameter | Symbol | Pin | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Oscillation frequency range (Note 1) | FmCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 1 | 4.5 to 5.5 | 11.76 | 12 | 12.24 | MHz |
| | FmLC | LC1, LC2 | 14.11 MHz (LC oscillation) Refer to Figure 2 | 4.5 to 5.5 | | 14.11 | | |
| | FmRC | | RC oscillation | 4.5 to 5.5 | 0.4 | 0.8 | 2.0 | |
| Oscillation stable time period (Note 2) | tmsCF | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 3 | 4.5 to 5.5 | | 0.02 | 0.2 | ms |

(Note 1) Refer to Table 1 and Table 2 for the oscillation constant.
(Note 2) The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released and the main-clock oscillation stop instruction released.
Refer to the Figure 3 for details.

## 3. Electrical Characteristics at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | $V_{DD}$ [V] | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input high-level current | $I_{IH}$(1) | • Port 1 DA0, 1<br>• Port 0 without pull-up MOS transistor | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN}$ = $V_{DD}$ (including the off-leakage current of the output transistor) | 4.5 to 5.5 | | | 1 | µA |
| | $I_{IH}$(2) | • Port 7 without pull-up MOS transistor<br>• Port 9<br>• $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | $V_{IN}$ = $V_{DD}$ | 4.5 to 5.5 | | | 1 | |
| Input low-level current | $I_{IL}$(1) | • Port 1 DA0, 1<br>• Port 0 without pull-up MOS transistor | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN}$ = $V_{SS}$ (including the off-leakage current of the output transistor) | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}$(2) | • Port 7 without pull-up MOS transistor<br>• Port 9 | $V_{IN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}$(3) | • $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | $V_{IN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| Output high-level voltage | $V_{OH}$(1) | CMOS output of ports 0, 1 DA0, 1 | $I_{OH}$ = –1.0 mA | 4.5 to 5.5 | $V_{DD}$–1 | | | V |
| | $V_{OH}$(2) | R, G, B, BL | $I_{OH}$ = –0.1 mA | 4.5 to 5.5 | $V_{DD}$–0.5 | | | |
| Output low-level voltage | $V_{OL}$(1) | Ports 0, 1 | $I_{OL}$ = 10 mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}$(2) | Ports 0, 1 DA0, 1 | • $I_{OL}$ = 1.6 mA<br>• The total current of the ports 0, 1 is not over 40 mA. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}$(3) | • R, G, B, BL<br>• PWM0 to PWM9 | • $I_{OL}$ = 3.0 mA<br>• The current of any pin is 3 mA or less. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}$(4) | P70 | $I_{OL}$ = 1 mA | 4.5 to 5.5 | | | 0.4 | |
| Pull-up MOS transistor resistance | Rpu | • Ports 0, 1<br>• Port 7 | $V_{OH}$ = 0.9 $V_{DD}$ | 4.5 to 5.5 | 13 | 38 | 80 | kΩ |
| Output off-leakage current | $I_{OFF}$ | PWM0 to PWM9 | $V_{OUT}$ = 13.5 V | 4.5 to 5.5 | | | 5 | µA |
| Hysteresis voltage | $V_{HIS}$ | • Ports 0, 1<br>• Port 7<br>• $\overline{RES}$<br>• $\overline{HS}$, $\overline{VS}$ | Output disable | 4.5 to 5.5 | | 0.1$V_{DD}$ | | V |

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Pin capacitance | CP | All pins | • f = 1 MHz<br>• Unmeasured input pins are set to $V_{SS}$ level.<br>• Ta = 25°C | 4.5 to 5.5 | | 10 | | pF |

## 4. Serial Input/Output Characteristics at Ta = –30°C to +70°C , $V_{SS}$ = 0 V

| Parameter | | | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | |
| Serial clock | Input clock | Cycle | tCKCY(1) | • SCK0<br>• SCLK0 | Refer to Figure 5 | 4.5 to 5.5 | 2 | | | tCYC |
| | | Low-level pulse width | tCKL(1) | | | 4.5 to 5.5 | 1 | | | |
| | | High-level pulse width | tCKH(1) | | | 4.5 to 5.5 | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | • SCK0<br>• SCLK0 | • Use a pull-up resistor (1 kΩ) when open-drain output<br>• Refer to Figure 5 | 4.5 to 5.5 | 2 | | | |
| | | Low-level pulse width | tCKL(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| | | High-level pulse width | tCKH(2) | | | 4.5 to 5.5 | | 1/2tCKCY | | |
| Serial input | Data set-up time | | tICK | SI0 | • Synchronized with the rising edge of SCK0.<br>• Refer to Figure 5 | 4.5 to 5.5 | 0.1 | | | µs |
| | Data hold time | | tCKI | | | 4.5 to 5.5 | 0.1 | | | |
| Serial output | Output delay time (External serial clock) | | tCKO(1) | SO0 | • Use a pull-up resistor (1kΩ) when open-drain output.<br>• Synchronized with the falling edge of SCK0.<br>• Refer to Figure 5 | 4.5 to 5.5 | | | 7/12tCYC +0.2 | µs |
| | Output delay time (Internal serial clock) | | tCKO(2) | | | 4.5 to 5.5 | | | 1/3tCYC +0.2 | |

## 5. Pulse Input Conditions at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [v] | min | typ | max | |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | • INT0, INT1<br>• INT2/T0IN | • Interrupt factor flag settable.<br>• Timer and counter 0 pulse-countable. | 4.5 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3/T0IN<br>(The noise rejection filter time constant is 1/1) | • Interrupt factor flag settable.<br>• Timer and counter 0 pulse-countable. | 4.5 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3/T0IN<br>(The noise rejection filter time constant is 1/16) | • Interrupt factor flag settable.<br>• Timer and counter 0 pulse-countable. | 4.5 to 5.5 | 32 | | | |
| | tPIL(4) | $\overline{RES}$ | Reset acceptable | 4.5 to 5.5 | 200 | | | µs |
| | tPIH(5)<br>tPIL(5) | $\overline{HS}$, $\overline{VS}$ | Display position can be controlled<br>Each active edge of $\overline{HS}$, $\overline{VS}$ must be set apart more than 1tCYC.<br>Refer to Figure 7 | 4.5 to 5.5 | 10 | | | tCYC |
| Rise/fall time | tTHL<br>tTLH | $\overline{HS}$ | Refer to Figure 7 | 4.5 to 5.5 | | | 500 | ns |
| Horizontal pull-in range | FH | $\overline{HS}$ | The monitor point in Figure 10 is 1/2 $V_{DD}$. | 4.5 to 5.5 | 15.23 | 15.73 | 16.23 | kHz |

## 6. A/D Converter Characteristics at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Resolution | N | | | 4.5 to 5.5 | | 4 | | bit |
| Absolute precision | ET | (Note 3) | | 4.5 to 5.5 | | ±1/4 | ±1/2 | LSB |
| Conversion time | tCAD | After the Vref selected till the conversion completed. | 1 bit conversion time = 2tCYC | 4.5 to 5.5 | | | 1.96 | µs |
| Reference current | $I_{REF}$ | | (Regulate the ladder resistor) | 4.5 to 55 | | 1.0 | 2.0 | mA |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN3 | | 4.5 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | $I_{AINH}$ | | $V_{AIN}$ = $V_{DD}$ | 4.5 to 5.5 | | | 1 | µA |
| | $I_{AINL}$ | | $V_{AIN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |

Note 3 : Absolute precision excepts quantizing error (±1/2LSB).

## 7. D/A Converter Characteristics at Ta = –30°C to +70°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Resolution | NDA | | | 4.5 to 5.5 | | 7 | | bit |
| Absolute precision | ETDA | | 7 bits mode (Note 4) | 4.5 to 5.5 | | ±2.0 | | LSB |
| Settling time | tSDA | | (Note 5) | 4.5 to 5.5 | | 1.0 | | µs |
| Analog input voltage range | $V_{AOUT}$ | DA0 to DA1 | | 4.5 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Output resistor | RODA | | (Note 6) | 4.5 to 5.5 | | 8 | | kΩ |

Note 4 : The ±1/2-LSB quantization error is not included. (No load.)
Note 5 : Settling time refers to the time from when the D/A conversion instruction is executed to when the analog voltage output corresponding to the digital voltage on the specific port is generated.
Note 6 : D/A data = 80H

## 8. Current Drain Characteristics at Ta = –30°C to +20°C , $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Current drain during basic operation (Note 7 ) | $I_{DDOP}$(1) | DVDD, AVDD | • FmCF = 12 MHz when ceramic oscillation<br>• FmLC = 14.11MHz when LC oscillation<br>• System clock : 12 MHz<br>• Internal RC when oscillation stops | 4.5 to 5.5 | | 21 | 32 | mA |
| Current drain in HALT mode (Note 7) | $I_{DDHALT}$(1) | DVDD, AVDD | • HALT mode<br>• FmCF = 12 MHz when ceramic oscillation<br>• FmLC = 0 Hz (when oscillation stops)<br>• System clock : 12 MHz<br>• Internal RC when oscillation stops. | 4.5 to 5.5 | | 5 | 10 | mA |
| | $I_{DDHALT}$(2) | DVDD, AVDD | • HALT mode<br>• FmCF = 0 MHz (when oscillation stops)<br>• FmLC = 0 Hz (when oscillation stops)<br>• System clock : Internal RC | 4.5 to 5.5 | | 400 | 800 | µA |
| Current drain in HOLD mode (Note 7) | $I_{DDHOLD}$(1) | DVDD, AVDD | • HOLD mode<br>• All oscillation stops. | 4.5 to 5.5 | | 0.05 | 20 | µA |
| | $I_{DDHOLD}$(2) | | | | | | | |

Note 7 : The current into the output transistors and the pull-up MOS transistors are ignored.

| Oscillation type | Manufacturer | Oscillator | C1 | C2 |
|---|---|---|---|---|
| 12 MHz ceramic resonator oscillation | Murata | CSA12.0MTZ | 33 pF | 33 pF |
| | | CST12.0MTW | on chip | |
| | Kyocera | KBR-12.0M | 47 pF | 47 pF |

* Both C1 and C2 must use an K rank (±10%) and an SL characteristics.

**Table 1 Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

| Oscillation type | L | C3 | C4 |
|---|---|---|---|
| 14.11 MHz LC oscillation | 4.7 μH | 33 pF | 45 pF (Trimmer) |
| | 4.7 μH ±10% (Variable) | 33 pH | 33 pH |

* See Figures 11 and 12.

**Table 2 LC Oscillation Guaranteed Constant (OSD clock)**

(Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
- If you use other oscillators herein, we provide no guarantee for the characteristics.
- Adjust the voltage of monitor point in Figure 10 to $1/2V_{DD}$±10% by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.

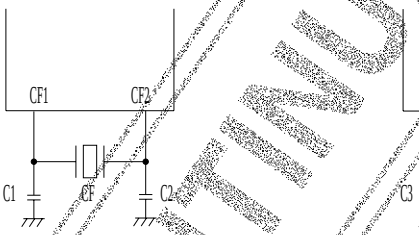



**Figure 1 Ceramic Oscillation**

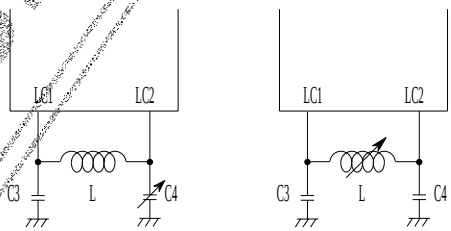



**Figure 2 LC Oscillation**

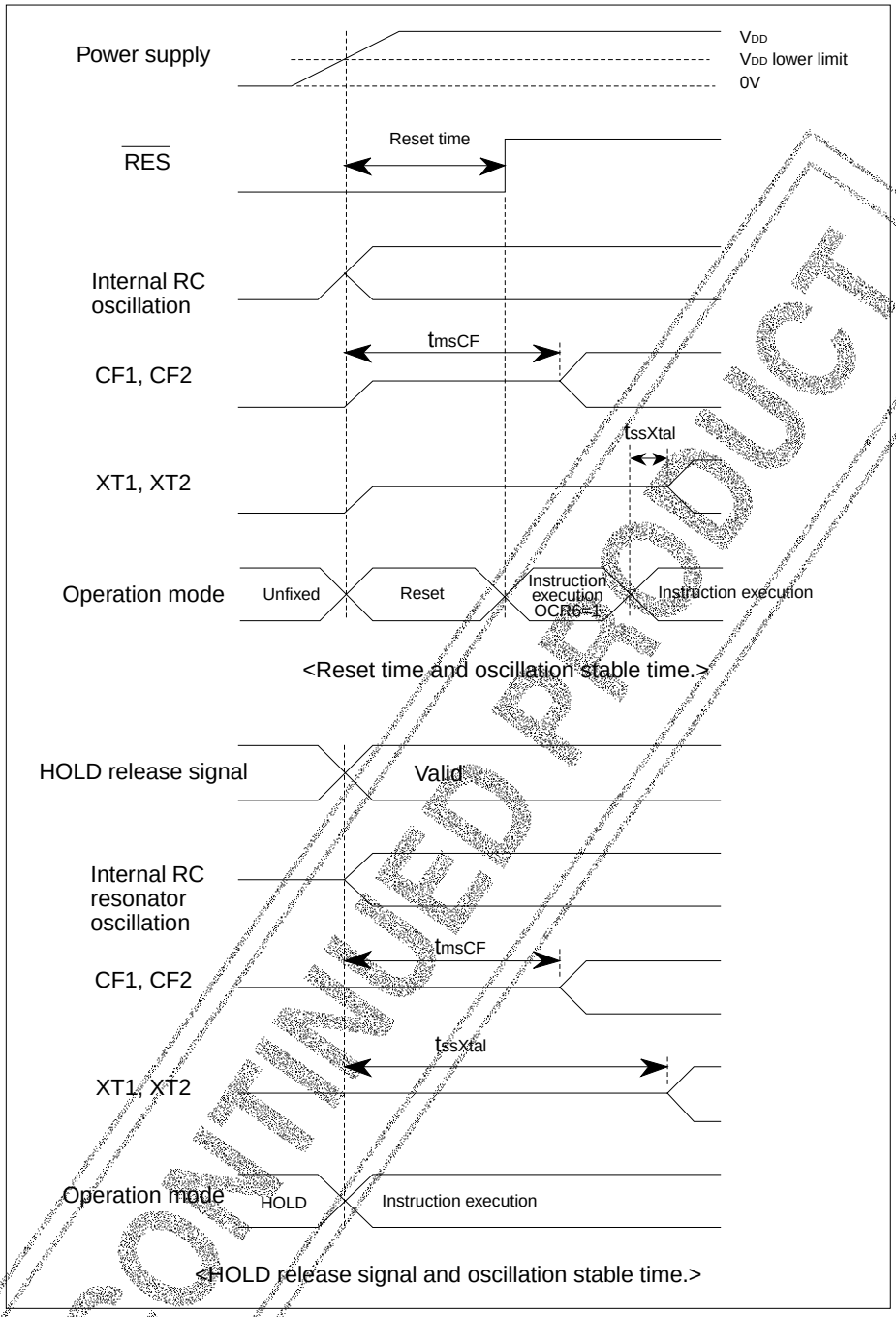
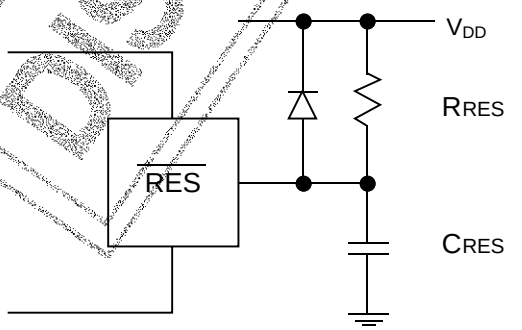



**Figure 3 Oscillation Stable Time**




(Note) Set the values of $C_{RES}$, $R_{RES}$ so that the reset time is 200 μs or longer.

**Figure 4 Reset Circuit**


< AC timing point >

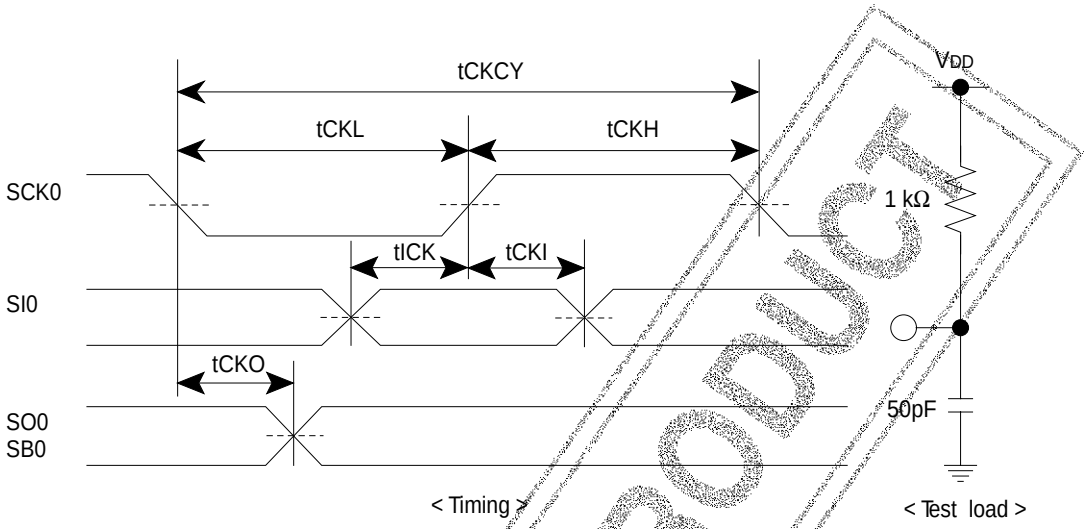



**Figure 5 Serial Input/output Test Condition**

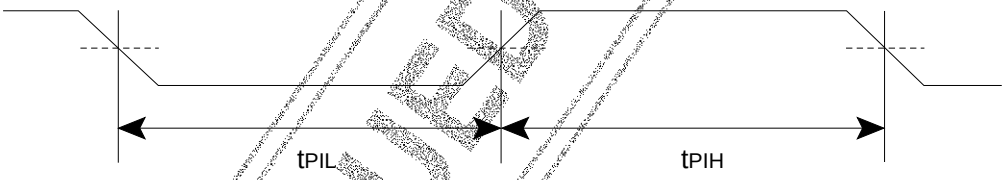



**Figure 6 Pulse Input Timing Condition - 1**

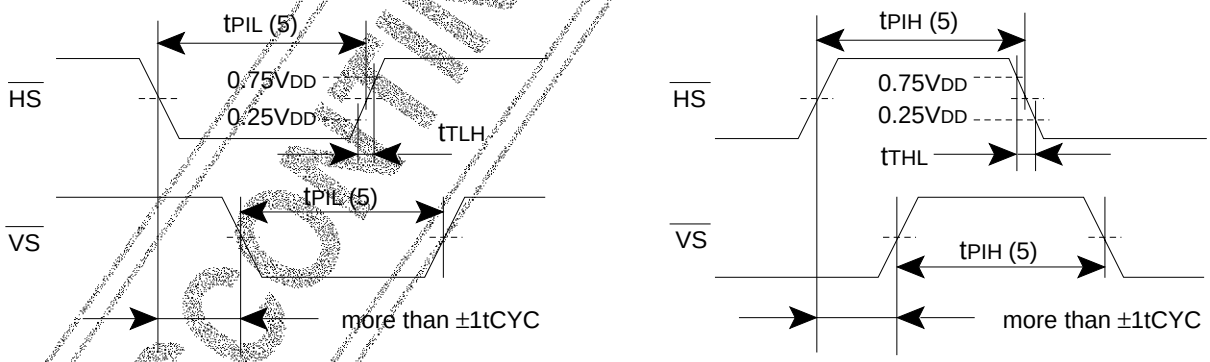



**Figure 7 Pulse Input Timing Condition - 2**

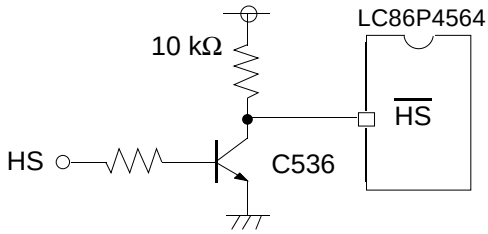



**Figure 8 Recommended Interface Circuit**

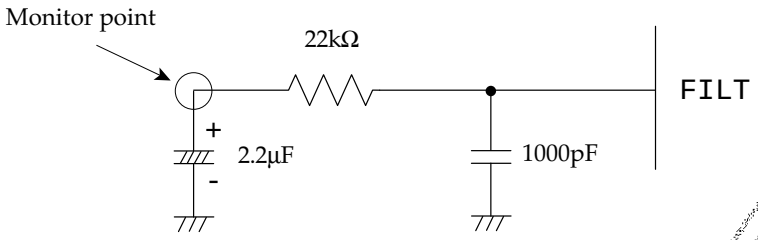



**Figure 10 FILT Recommended Circuit**

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

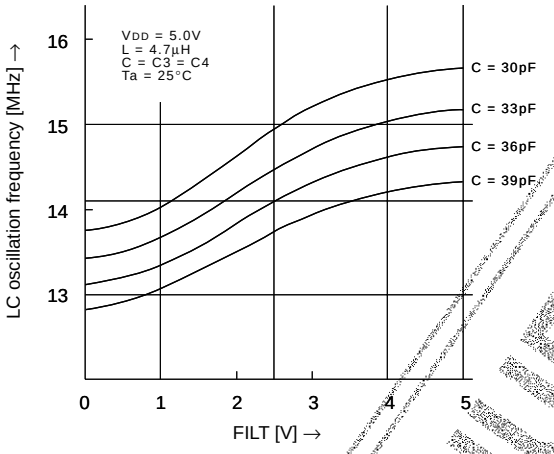



**Figure 11 FILT-LC Oscillation Frequency(1)**

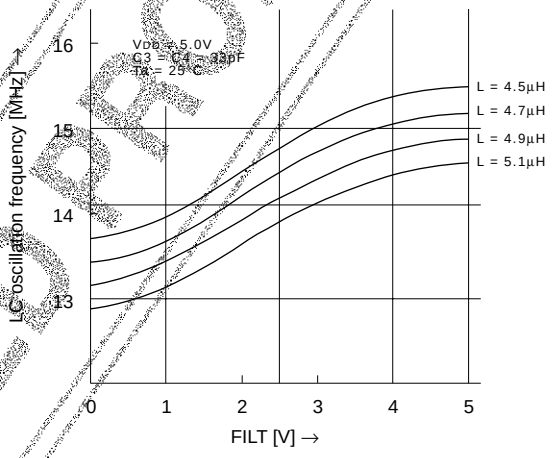



**Figure 12 FILT-LC Oscillation Frequency(2)**

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
- SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.
- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products(including technical data,services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- 
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of May, 1998. Specifications and information herein are subject to change without notice.