

**LC86E6032****8-Bit Single-Chip Microcontroller****Preliminary****Overview**

The LC86E6032 microcontroller is a CMOS 8-bit single chip microcontroller with UVEPROM for LC866000A series.

This microcontroller has the same functions and pin assignment as for the LC866000A series mask ROM version, and a 32K-byte EPROM.

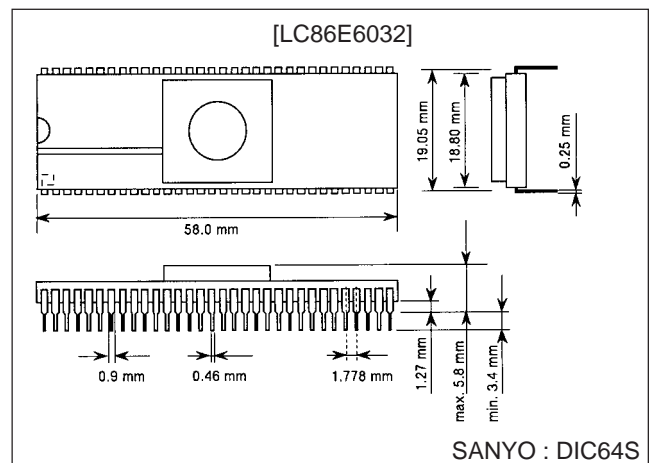
Program data is rewritable. It is suitable for program developments.

**Features**

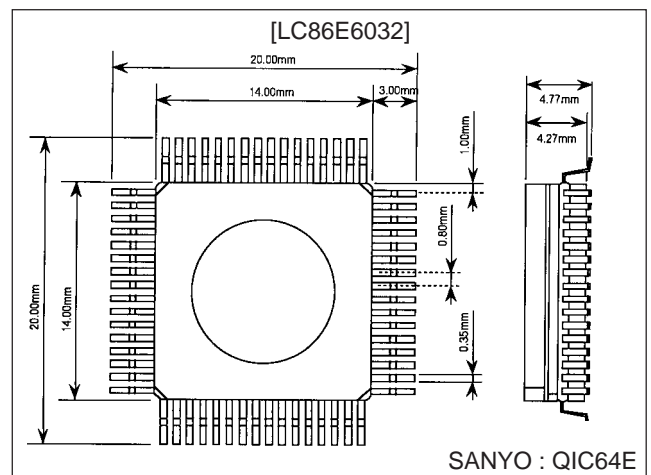
- (1) Option switching using EPROM data  
The optional functions of the LC866000A series can be specified using EPROM data.  
LC86E6032 can be checked the functions of trial piece using the mass production board.
- (2) Internal 32K-byte UVEPROM  
32K-byte UVEPROM (ultraviolet erasable and programmable ROM) is built in. This corresponds to LC866032B/28B/24B/20A/16A/12A/08A.
- (3) The pin compatible with mask ROM version
- (4) Factory shipment  
DIC-64S  
QFC-64E (Under development)

**Package Dimensions**

unit : mm

**3126-DIC64S**

unit : mm

**3152-QFC64E**

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## Notice for Use

LC86E6032 is provided for the program development and checking the function of LC866000A series.  
At using, take notice of the followings.

### (1) Reset

It is necessary to be sure to go into 'L' level and hold for 200  $\mu$ s to reset terminal ( $\overline{\text{RES}}$ ) after power supplied voltage has been over inferior limit of supply voltage.

The option is specified until 3ms after going into 'H' level to reset terminal by degrees.

The program is executed from 00H of program counter. The output form of all ports are N-channel open-drain while 'L' level to reset terminal.

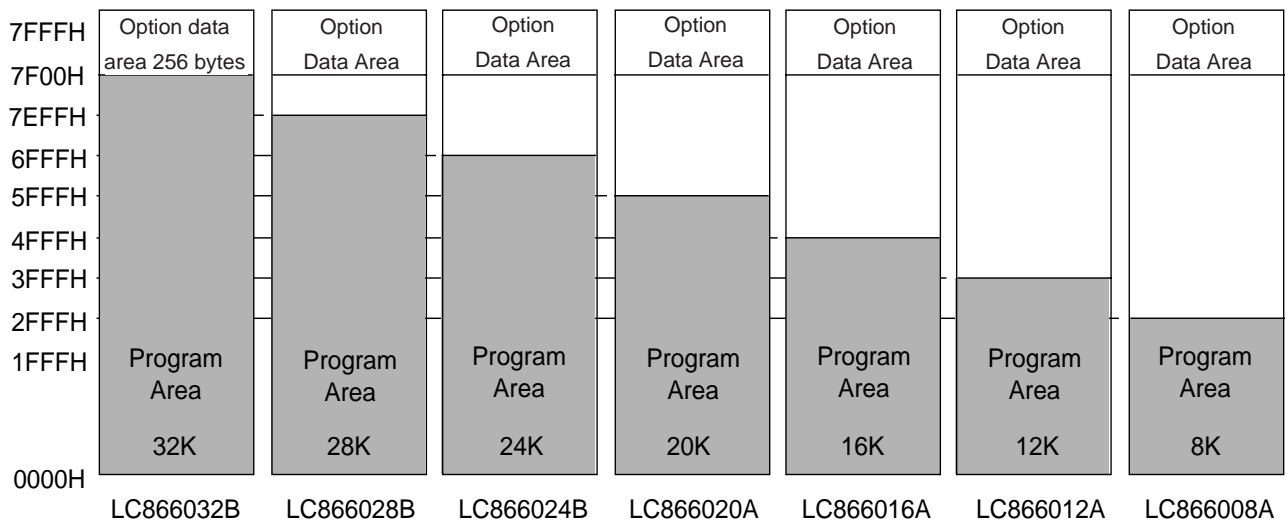
### (2) Option

The LC86E6032 uses 256 bytes addressed 7F00H to 7FFFH in program memory as option data area.

This area does not affect the execution of program but means that the LC866032A program memory is 32512 bytes addressed 0000H to 7FFFH.

The option data is specified by the option-setting program "SU866000.EXE". The specified option data is linked to the program area by linkage editor "L866000.EXE".

### (3) ROM space



### (4) Points of difference LC86E6032 and LC866000A series (mask ROM version)

Item	LC86E6032	LC866032B/28B/24B/20A/16A/12A/08A
Operating temperature range (Topr)	+10°C to +40°C	-30°C to +70°C
Output form of port at reset	Open-drain output	Output form specified by option data
Output form of segment S0/T0 to S6/T6 S7/T7 to S15/T15 S16 to S23 S24 to S29	Pulldown resistance Not provided Provided (fixed) Provided (fixed) Not provided	Pulldown resistance: Provided/ Not provided Specified by option Provided (fixed) Specified by option Specified by option
Operating supply voltage range (V <sub>DD</sub> )	4.5 to 6.0V	2.5 to 6.0V

## Option

A kind of option corresponding LC86E6032

Option types	Pins, Circuits	Contents of option
Input/output form of input/output ports	Port 0 (specified in a bit)	1. Input :No Pullup MOS Transistor Output :N-channel open-drain 2. Input :Pullup MOS Transistor Output :CMOS
	Port 1 (specified in a bit)	1. Input :Programmable pullup MOS Transistor Output :N-channel open-drain 2. Input :Programmable pullup MOS Transistor Output :CMOS
Pullup MOS Transistor of input port	Port 7 (specified in a bit)	1. No Pullup MOS Transistor 2. Pullup MOS Transistor

A kind of option not corresponding LC86E6032

Option types	Pins,Circuits	Contents of option
Pulldown resistance of high voltage withstand output terminal	S0/T0 to S6/T6 S16 to S29 (specified in a bit)	1. Pulldown resistance 2. No Pulldown resistance

## How to Use

### (1) Specification of options

LC86E6032 must be programmed after specifying option data. The option is specified by "SU866000.EXE". The specified option file and the file created by our macro assembler "M866000.EXE" are linked by our linkage loader "L866000.EXE" which creates .HEX file, then the option code is put in the option specified area (7F00H to 7FFFH) of its .HEX file.

### (2) How to write data to EPROM

When writing data that was created by the linker to the LC86E6032, a general-purpose EPROM programmer can be used by using special write conversion boards (W86EP6032D, W86EP6032Q).

- Recommended EPROM programmers

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL 1890A

- "27512 (Vp-p = 12.5 V) Intel high-speed programming" mode should be used. The address must be set to "0000H to 7FFFH" and the jumper (DASEC) must be set 'OFF' at programming.

### (3) How to use the data security function

"Data security" is a function to prevent the EPROM data from being read.

Instructions on using the data security function:

- Set the jumper (DASEC) of the attachment 'ON'.
- Attempt to program the EPROM.

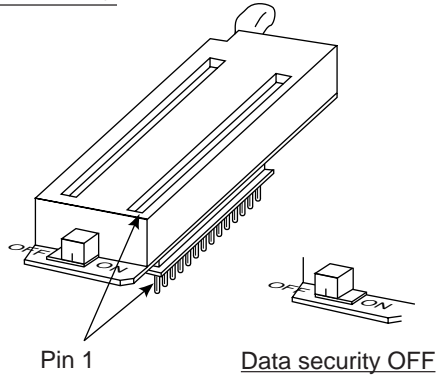
The EPROM programmer displays an error. The error is a result of normal activity of the data security feature, and does not indicate a problem with the programmer or the LSI.

### Notes

- The data security function is not carried out when the data of all address contain 'FF' at step 2 above.
- Data security cannot be executed when the sequential writing operation of programming "BLANK=>PROGRAM=>VERIFY" is used at step 2 above.
- Set the jumper 'OFF' after the execution of data security.

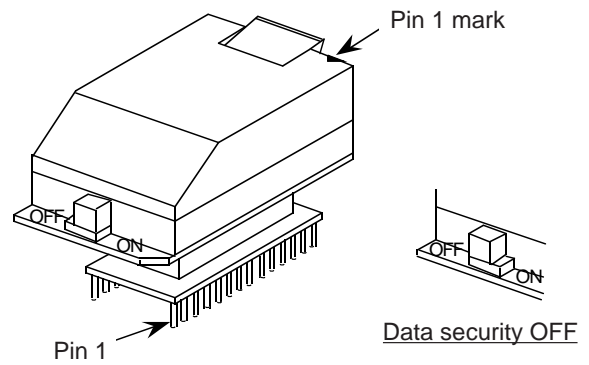
- (4) Erasing data  
Use a general-purpose EPROM eraser to erase the written data.
- (5) Shielding  
The UVEPROM (ultraviolet erasable programmable ROM) is incorporated in the IC. Cover the window of the IC with a seal in use.

### Data security



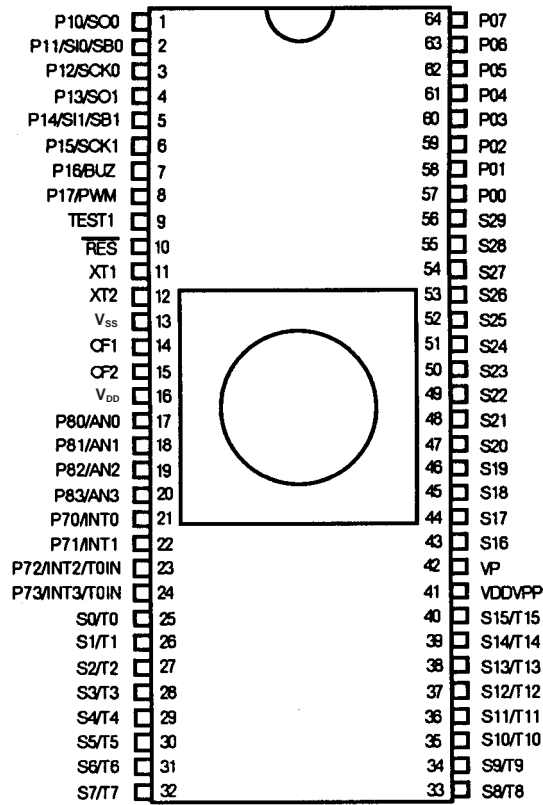
W86EP6032D

### Data security



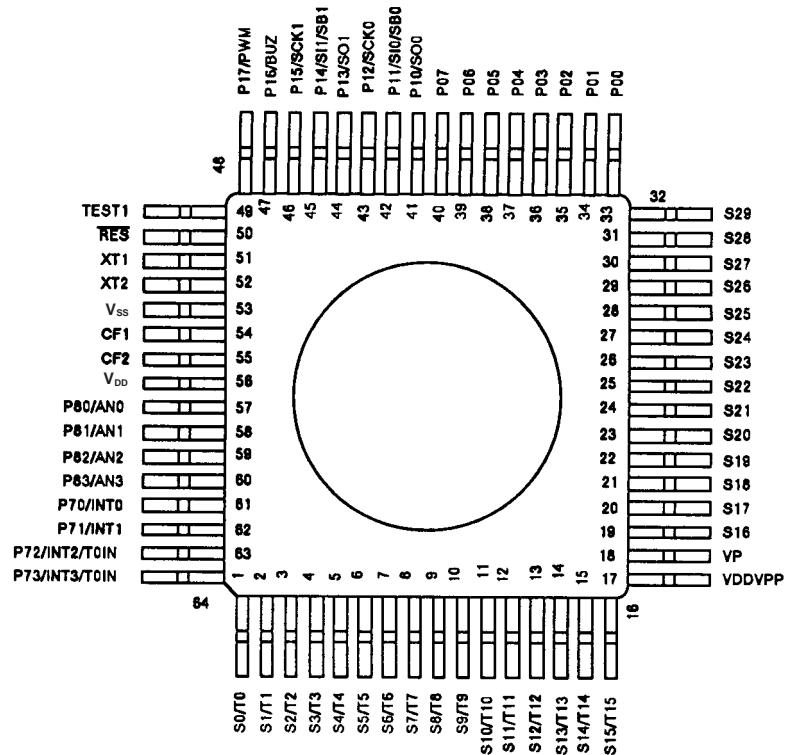
W86EP6032Q

## Pin Assignment



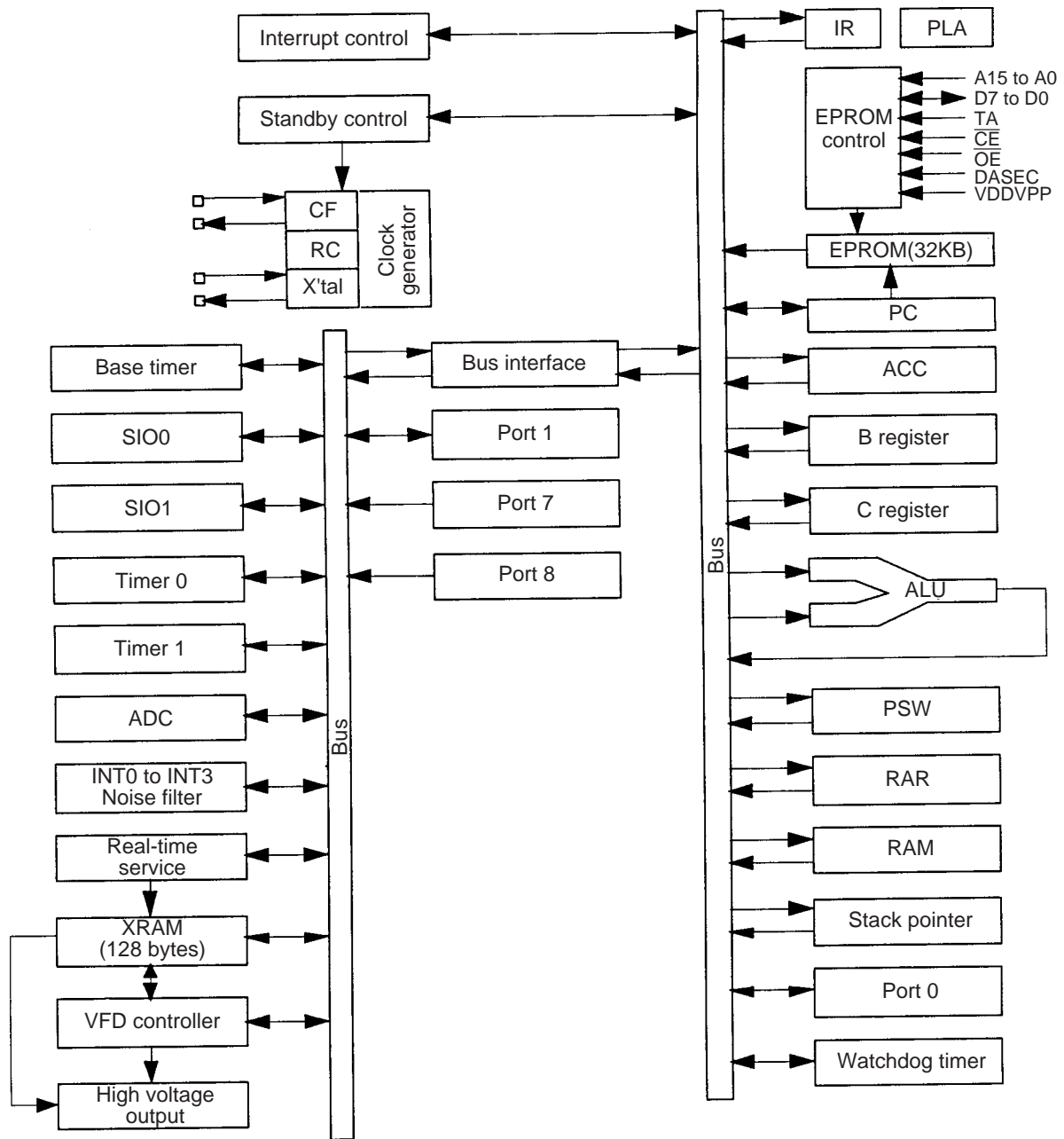
Top view

## Pin Assignment



Top view

## System Block Diagram



## Pin Description

Pin name	I/O	Function description					Option	Function in PROM mode
V <sub>SS</sub>	—	Power supply pin (–)						
V <sub>DD</sub>	—	Power supply pin (+)						
VP	—	Power supply pin (–) (Power supply for VFD display drive output) (Power supply for pull-down resistor)						
VDDVPP	—	Power supply pin (+)						Power for programming
PORT0 P00 to P07	I/O	• 8-bit input/output port • Input/output specification can be made for 4-bit unit. • Input for HOLD release • Input for port 0 interrupt					• Pull-up resistor : Provided/Not provided • Output form : CMOS/ N-channel open-drain.	
PORT1 P10 to P17	I/O	• 8-bit input/output port • Data direction can be specified for each bit. • Other pin functions P10 : SIO0 data output P11 : SIO0 data input/ bus input/output P12 : SIO0 clock input/output P13 : SIO1 data output P14 : SIO1 data input/ bus input/output P15 : SIO1 clock input/output P16 : Buzzer output P17 : Timer 1 output (PWM output)					Output form : CMOS/ N-channel open-drain	Data input/output • D0 to D7
PORT7 P70 P71 to P73	I/O  I	• 4-bit input port • Other pin functions P70 : INT0 input/HOLD release/N-channel transistor output for watchdog timer. P71 : INT 1 input/HOLD release. P72 : INT 2 input/timer 0 event input. P73 : INT 3 input with noise filter/timer 0 event input. • Interrupt received format, vector address.					• Pull-up resistor : Provided/Not provided	Input of PROM control signal  • DASEC (*1) • $\overline{OE}$ (*2) • $\overline{CE}$ (*3)
			Rising	Falling	Rising & falling	High level	Low level	Vector
		INT0	Enable	Enable	Disable	Enable	Enable	03H
		INT1	Enable	Enable	Disable	Enable	Enable	0BH
		INT2	Enable	Enable	Enable	Disable	Disable	13H
		INT3	Enable	Enable	Enable	Disable	Disable	1BH
PORT8 P80 to P83	I	• 4-bit input port • Other functions AD input port (4 port pins)						
S0/T0 to S6/T6	O	Output for VFD display controller Segment/timing common output						
S7/T7 to S15/T15	O	Output for VFD display controller Segment/timing common output Output with built-in pull-down resistor						• S14/T14 : TA (*4) • S15/T15 : A14 (*5)

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Pin name	I/O	Function description	Option	Function in PROM mode
S16 to S23	O	Output for VFD display controller Segment output Output with built-in pull-down resistor		Address input •A13 to A0
S24 to S29	O	Output for VFD display controller Segment output		
$\overline{\text{RES}}$	I	Reset pin		
TEST1	O	Test pin Should be left open.		
XT1	I	Input pin for 32.768 kHz crystal oscillation When not used, connect to $V_{DD}$ .		
XT2	O	Output pin for 32.768 kHz crystal oscillation When not used, should be left open.		
CF1	I	Input pin for ceramic resonator oscillation		
CF2	O	Output pin for ceramic resonator oscillation		

\*1 Memory select input for data security

\*2 Output enable input

\*3 Chip enable input

\*4 TA → PROM control signal input

\*5 A14 → Address input

\* All of port options can be specified in bit unit.

\* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistor specified at pullup option
Ports 0,7	Input	Fixed pullup resistor exists
Port 1	Input	Programmable pullup resistor OFF

Pin name	A state of P-channel transistor
S0/T0 to S15/T15	P-channel transistor OFF
S16 to S29	P-channel transistor OFF



## Specification

### 1. Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter		Symbol	Pins	Conditions	V <sub>DD</sub> [V]	Ratings			Unit
						min	typ	max	
Maximum supply voltage		V <sub>DD</sub> max	V <sub>DD</sub> ,V <sub>DDVPP</sub>	V <sub>DD</sub> = V <sub>DDVPP</sub>		−0.3		+7.0	V
Input voltage		V <sub>I</sub> (1)	• P 71, 72, 73 • Port 8 • RES			−0.3		V <sub>DD</sub> +0.3	
		V <sub>I</sub> (2)	VP			V <sub>DD</sub> −45		V <sub>DD</sub> +0.3	
Output voltage		V <sub>O</sub>	• S0/T0 to S15/T15 • S16 to S29			V <sub>DD</sub> −45		V <sub>DD</sub> +0.3	
Input/output voltage		V <sub>IO</sub>	Ports 0, 1,P 70			−0.3		V <sub>DD</sub> +0.3	
High-level output current	Peak output current	I <sub>OPH</sub> (1)	Ports 0, 1	• CMOS output • At each pin		−4			mA
		I <sub>OPH</sub> (2)	S0/T0 to S15/T15	At each pin		−30			
		I <sub>OPH</sub> (3)	S16 to S29	At each pin		−15			
	Total output current	ΣI <sub>OA</sub> H(1)	Port 0	Total of all pins		−10			
		ΣI <sub>OA</sub> H(2)	Port 1	Total of all pins		−10			
		ΣI <sub>OA</sub> H(3)	• S0/T0 to S15/T15 • S16 to S29	Total of all pins		−130			
Low-level output current	Peak output current	I <sub>OPL</sub> (1)	Ports 0, 1	At each pin				20	
		I <sub>OPL</sub> (2)	P70	At each pin				15	
	Total output current	ΣI <sub>OA</sub> L(1)	Port 0	Total of all pins				−30	
		ΣI <sub>OA</sub> L(2)	Port 1,P70	Total of all pins				40	
Allowable power dissipation		Pd max(1)	DIC64S	Ta = +10°C to +40°C				760	mW
		Pd max(2)	QFC64E	Ta = +10°C to +40°C		To be determined after evaluation			
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				−65		150	

**2. Allowable Operating Conditions at Ta = +10°C to +40°C, VSS = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				VDD[V]	min	typ	max	
Operating supply voltage range	VDD	VDD	0.98 μs ≤ tCYC tCYC ≤ 400 μs		4.5		6.0	V
HOLD voltage	VHD	VDD	<ul style="list-style-type: none"> <li>When in HOLD mode</li> <li>RAM and registers retain previous data.</li> </ul>		2.0		6.0	
Pulldown supply voltage	VP	VP		4.5 to 6.0	−35		VDD	
Input high-level voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	0.4VDD +0.9		VDD	
	VIH(2)	<ul style="list-style-type: none"> <li>Port 1</li> <li>P72, 73 (Schmitt)</li> </ul>	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(3)	<ul style="list-style-type: none"> <li>P70 Port input/interrupt.</li> <li>P71</li> <li>RES (Schmitt)</li> </ul>	Output N-channel transistor OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	P70 Watchdog timer	Output N-channel transistor OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(5)	Port 8		4.5 to 6.0	0.75VDD		VDD	
Input low-level voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	<ul style="list-style-type: none"> <li>Port 1</li> <li>P72, 73(Schmitt)</li> </ul>	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	<ul style="list-style-type: none"> <li>P70 Port input/interrupt.</li> <li>P71</li> <li>RES (Schmitt)</li> </ul>	N-channel transistor OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	P70 Watchdog timer	N-channel transistor OFF	4.5 to 6.0	VSS		0.8VDD −1.0	
	VIL(5)	Port 8		4.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	<ul style="list-style-type: none"> <li>12 MHz (ceramic resonator oscillation).</li> <li>Refer to Figure 1.</li> </ul>	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	<ul style="list-style-type: none"> <li>3 MHz (ceramic resonator oscillation).</li> <li>Refer to Figure 1.</li> </ul>	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	2.0	
	FsXtal	XT1, XT2	<ul style="list-style-type: none"> <li>32.768 kHz (crystal oscillation).</li> <li>Refer to Figure 2.</li> </ul>	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	<ul style="list-style-type: none"> <li>12 MHz (ceramic resonator oscillation).</li> <li>Refer to Figure 3.</li> </ul>	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1, CF2	<ul style="list-style-type: none"> <li>3 MHz (ceramic resonator oscillation).</li> <li>Refer to Figure 3.</li> </ul>	4.5 to 6.0		0.1	1	
	tssXtal	XT1, XT2	<ul style="list-style-type: none"> <li>32.768 kHz (crystal oscillation).</li> <li>Refer to Figure 3.</li> </ul>	4.5 to 6.0		1	1.5	s

(Note 1) Refer to Table 1 and Table 2 for the oscillation constants.

3. Electrical Characteristics at Ta= +10°C to +40°C , VSS = 0 V

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			Unit
					min	typ	max	
Input high-level current	I <sub>IH</sub> (1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF. • V <sub>IN</sub> = V <sub>DD</sub> (including off-state leak current of output transistor)	4.5 to 6.0			1	μA
	I <sub>IH</sub> (2)	• Port 7 without pull-up MOS transistor • Port 8	V <sub>IN</sub> = V <sub>DD</sub>	4.5 to 6.0			1	
	I <sub>IH</sub> (3)	• $\overline{\text{RES}}$	V <sub>IN</sub> = V <sub>DD</sub>	4.5 to 6.0			1	
Input low-level current	I <sub>IL</sub> (1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF. • V <sub>IN</sub> = V <sub>SS</sub> (including off-state leak current of output transistor)	4.5 to 6.0	−1			
	I <sub>IL</sub> (2)	• Port 7 without pull-up MOS transistor • Port 8	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 6.0	−1			
	I <sub>IL</sub> (3)	• $\overline{\text{RES}}$	V <sub>IN</sub> = V <sub>SS</sub>	4.5 to 6.0	−1			
Output high-level voltage	V <sub>OH</sub> (1)	• Ports 0, 1 at CMOS output	I <sub>OH</sub> = −1.0 mA	4.5 to 6.0	V <sub>DD</sub> −1			V
	V <sub>OH</sub> (2)		I <sub>OH</sub> = −0.1 mA	4.5 to 6.0	V <sub>DD</sub> −0.5			
	V <sub>OH</sub> (3)	S0/T0 to S15/T15	I <sub>OH</sub> = −20 mA	4.5 to 6.0	V <sub>DD</sub> −1.8			
	V <sub>OH</sub> (4)		• I <sub>OH</sub> = −1.0 mA • The current of any unmeasurement pin is not over 1 mA.	4.5 to 6.0	V <sub>DD</sub> −1			
	V <sub>OH</sub> (5)	S16 to S29	I <sub>OH</sub> = −5 mA	4.5 to 6.0	V <sub>DD</sub> −1.8			
	V <sub>OH</sub> (6)		• I <sub>OH</sub> = −1.0 mA • The current of any unmeasurement pin is not over 1 mA.	4.5 to 6.0	V <sub>DD</sub> −1			
Output low-level voltage	V <sub>OL</sub> (1)	Ports 0,1	I <sub>OL</sub> = 10 mA	4.5 to 6.0			1.5	
	V <sub>OL</sub> (2)		• I <sub>OL</sub> = 1.6 mA • The total current of the Ports 0,1 is not over 40 mA	4.5 to 6.0			0.4	
	V <sub>OL</sub> (3)	P70	I <sub>OL</sub> = 1 mA	4.5 to 6.0			0.4	
Pull-up MOS transistor resistor	R <sub>pu</sub>	• Ports 0, 1 • Port 7	V <sub>OH</sub> = 0.9 V <sub>DD</sub>	4.5 to 6.0	15	40	70	kΩ
Output off-state leak current	I <sub>OFF</sub> (1)	• S0/T0 to S6/T6 • S24 to S29 (Without pulldown resistor)	• Output P-channel transistor OFF. • V <sub>OUT</sub> = V <sub>SS</sub>	4.5 to 6.0	−1			μA
	I <sub>OFF</sub> (2)		• Output P-channel transistor OFF. • V <sub>OUT</sub> = V <sub>DD</sub> −40V	4.5 to 6.0	−30			

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Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V <sub>DD</sub> [V]	min	typ	max	
Pulldown resistor	R <sub>pd</sub>	• S7/T7 to S15T15 • S16 to S23 (With pulldown resistor)	• Output P-channel transistor OFF.  • V <sub>OUT</sub> = 3V  • V <sub>P</sub> = −30V	5.0	60	100	200	kΩ
Hysteresis voltage	V <sub>HIS</sub>	• Ports 0,1  • Port 7 • $\overline{\text{RES}}$	• Output disable	4.5 to 6.0		0.1V <sub>DD</sub>		V
Pin capacitance	C <sub>P</sub>	All pins	• f=1MHz • Unmeasurement terminals for input are set to V <sub>SS</sub> level. • Ta= 25°C	4.5 to 6.0		10		pF

#### 4. Serial Input/Output Characteristics at Ta = +10°C to +40°C , V<sub>SS</sub> = 0 V

Parameter		Symbol	Pins	Conditions	Ratings			Unit
					V <sub>DD</sub> [V]	min	typ	max
Serial clock	Input clock	Cycle	SCK0, SCK1	Refer to Figure 5.	4.5 to 6.0	2		tCYC
		Low-level pulse width			4.5 to 6.0	1		
		High-level pulse width			4.5 to 6.0	1		
	Output clock	Cycle	SCK0, SCK1	<ul style="list-style-type: none"> <li>• Use pull-up resistor (1 kΩ) when set to open-drain output.</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 6.0	2		
		Low-level pulse width			4.5 to 6.0		1/2tCKCY	
		High-level pulse width			4.5 to 6.0		1/2tCKCY	
Serial input	Data set-up time	t <sub>ICK</sub>	<ul style="list-style-type: none"> <li>• SI0, SI1</li> <li>• SB0, SB1</li> </ul>	<ul style="list-style-type: none"> <li>• Data set-up to SCK0, 1</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 6.0	0.1		μs
	Data hold time	t <sub>ICKI</sub>			4.5 to 6.0	0.1		
Serial output	Output delay time (Serial clock is extrnal clock.)	t <sub>CKO</sub> (1)	<ul style="list-style-type: none"> <li>• SO0, SO1</li> <li>• SB0, SB1</li> </ul>	<ul style="list-style-type: none"> <li>• Data hold from SCK0, 1</li> <li>• Use pull-up resistor (1 kΩ) when set to open-drain output.</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 6.0			7/12tCYC +0.2
	Output delay time (Serial clock is internal clock.)	t <sub>CKO</sub> (2)	<ul style="list-style-type: none"> <li>• SO0, SO1</li> <li>• SB0, SB1</li> </ul>	<ul style="list-style-type: none"> <li>• Data hold from SCK0, 1</li> <li>• Use pull-up resistor (1 kΩ) when set to open-drain output.</li> <li>• Refer to Figure 5.</li> </ul>	4.5 to 6.0			1/3tCYC +0.2

**5. Pulse Input Conditions at Ta = +10°C to +40°C, VSS = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				VDD [V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/64.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	128			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5 to 6.0	200			μs

**6. A/D Converter Characteristics at Ta = +10°C to +40°C, VSS = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				VDD [V]	min	typ	max	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)				±1.5	LSB
Conversion time	tCAD		A/D conversion time = 16 x tCYC (ADCR2 = 0) (Note 3)		15.68 (tCYC = 0.98 μs)		65.28 (tCYC = 4.08 μs)	μs
			A/D conversion time = 32 x tCYC (ADCR2 = 1) (Note 3)		31.36 (tCYC = 0.98 μs)		130.56 (tCYC = 4.08 μs)	
Analog input voltage range	VAIN	AN0 to AN3			VSS		VDD	V
Analog port input current	I <sub>AINH</sub>		VAIN = VDD				1	μA
	I <sub>AINL</sub>		VAIN = VSS		-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time is the time from execution of the instruction to start conversion to the completion of shifting the A/D converted value to the register.

**7. Current Drain Characteristics at Ta = +10°C to +40°C , VSS = 0 V**

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V <sub>DD</sub> [V]	min	typ	max	
Current drain during basic operation (Note 4)	I <sub>DDOP</sub> (1)	V <sub>DD</sub>	•FmCF = 12 MHz for ceramic resonator oscillation. •FsXtal = 32.768 kHz for crystal oscillator. •System clock : 12 MHz side •Internal RC oscillator stopped.	4.5 to 6.0		13	26	mA
	I <sub>DDOP</sub> (2)		•FmCF = 3 MHz for ceramic resonator oscillation. •FsXtal = 32.768 kHz for crystal oscillator. •System clock : 3 MHz side •Internal RC oscillator stopped.	4.5 to 6.0		6.5	14	
	I <sub>DDOP</sub> (3)		•FmCF = 0 Hz (when oscillator stops). •FsXtal = 32.768 kHz for crystal oscillator. •System clock : RC oscillator.	4.5 to 6.0		4	10	
	I <sub>DDOP</sub> (4)		•FmCF = 0 Hz (when oscillator stops). •FsXtal = 32.768 kHz for crystal oscillator. •System clock : 32.768 kHz side •Internal RC oscillator stopped.	4.5 to 6.0		3.5	9	

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Parameter	Symbol	Pins	Conditions	V <sub>DD</sub> [V]	Ratings			Unit
					min	typ	max	
Current drain at HALT mode (Note 4)	I <sub>DDHALT</sub> (1)	V <sub>DD</sub>	<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 12 MHz for ceramic resonator oscillation.</li> <li>• FsXtal = 32.768 kHz for crystal oscillator.</li> <li>• System clock : 12 MHz side</li> <li>• Internal RC oscillator stopped.</li> </ul>	4.5 to 6.0		5	10	mA
	I <sub>DDHALT</sub> (2)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 3 MHz for ceramic resonator oscillation.</li> <li>• FsXtal = 32.768 kHz for crystal oscillator.</li> <li>• System clock : 3 MHz side</li> <li>• Internal RC oscillator stopped.</li> </ul>	4.5 to 6.0		1.8	4.6	
	I <sub>DDHALT</sub> (3)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 0 Hz (when oscillator stops).</li> <li>• FsXtal = 32.768 kHz for crystal oscillator.</li> <li>• System clock : RC oscillator</li> </ul>	4.5 to 6.0		400	800	μA
	I <sub>DDHALT</sub> (4)		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF = 0 Hz (when oscillator stops).</li> <li>• FsXtal = 32.768 kHz for crystal oscillator.</li> <li>• System clock : 32.768 kHz side</li> <li>• Internal RC oscillator stopped.</li> </ul>	4.5 to 6.0		20	60	
Current drain at HOLD mode (Note 4)	I <sub>DDHOLD</sub> (1)	V <sub>DD</sub>	HOLD mode	4.5 to 6.0		0.05	30	
	I <sub>DDHOLD</sub> (2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CSA12.0MT	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
3 MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33 pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47 pF	47 pF

\* Both C1 and C2 must use K rank ( $\pm 10\%$ ) and SL characteristics.

**Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main-clock)**

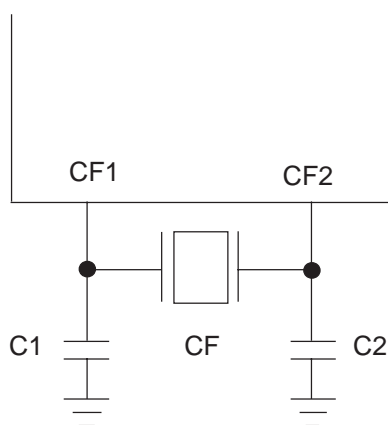
Oscillation type	Supplier	Oscillator	C3	C4
32.768 kHz crystal oscillation	Dai SINKU	DT-38(1TA252E00)	18 pF	18 pF
	Kyocera	KF-38G-13P0200	18 pF	18 pF

\* Both C3 and C4 must use J rank ( $\pm 5\%$ ) and CH characteristics.

(If high precision is unnecessary, use K rank ( $\pm 10\%$ ) and SL characteristics.)

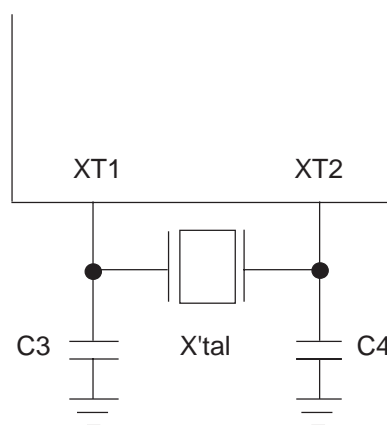
**Table 2. Crystal Oscillation Guaranteed Constants (Sub-clock)**

- Notes
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
  - If you use other oscillators herein, we provide no guarantee for the characteristics.



Main-clock circuit

**Figure 1 Ceramic Resonator Oscillation**



Sub-clock circuit

**Figure 2 Crystal Oscillation**



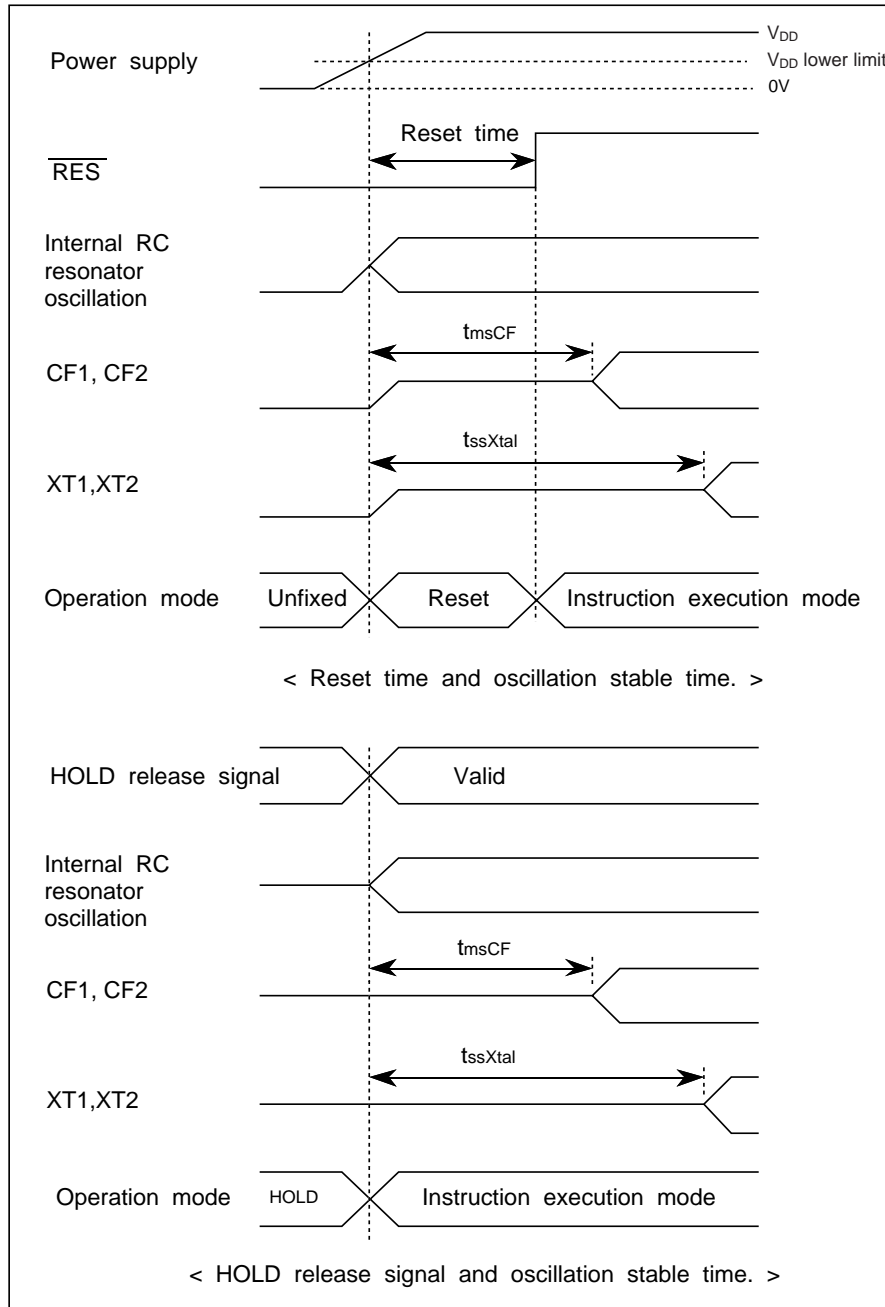
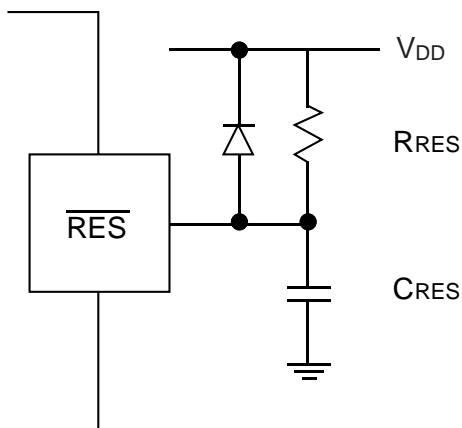


Figure 3 Oscillation Stable Time



(Note)

The values of  $C_{RES}$  and  $R_{RES}$  should be determined such that reset time is at least 200  $\mu s$ , measured from the moment the power exceeds the  $V_{DD}$  lower limit.

Figure 4 Reset Circuit

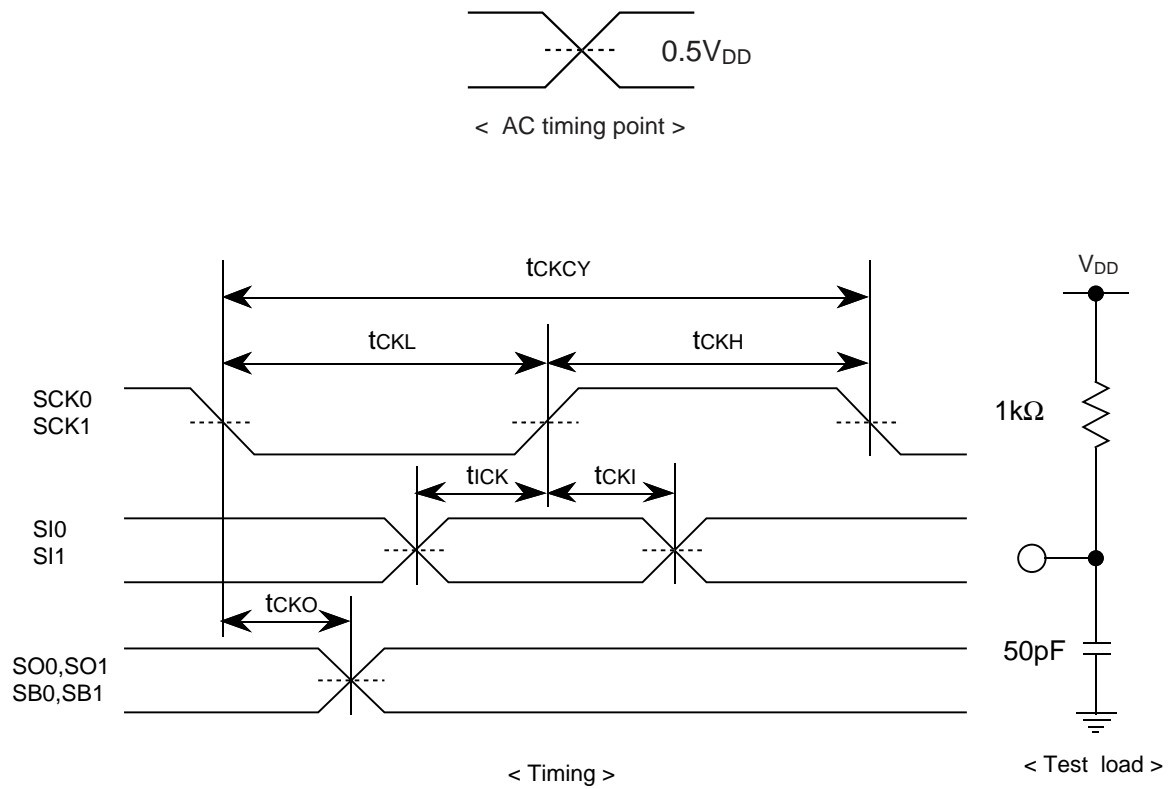


Figure 5 Serial Input/Output Test Conditions

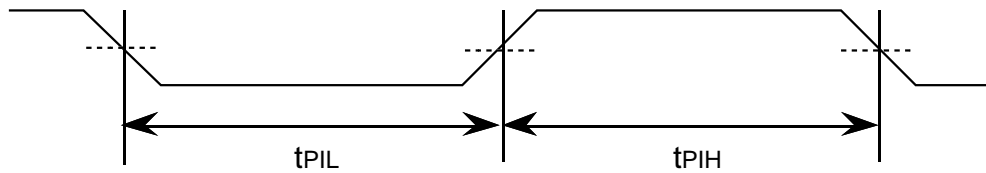


Figure 6 Pulse Input Timing Conditions

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