Ordering number : ENN*6703

CMOS IC

LC868920A

Dot Matrix LCD Segment Driver with On-Chip 1280-Byte Display RAM for the LC868364A Expansion

Preliminary

Overview

The LC868920A is a segment driver with built-in display RAM for the liquid crystal dot matrix-graphic display. It stores the display data sent from the 8-bit microcontroller in the internal display RAM and generates dot matrix LCD drive signals to control LCD panels. The LC868920A controls the graphic display simply in such a way that one bit of the display RAM corresponds to one dot of the LCD.

It is possible to expand the display capacity of LC868364A more than 32 × 100 dots by using this segment driver. The LCD controller operates on the low frequency clock from the microcontroller except when writing to registers or RAM. Therefore, it is suitable for personal electronics devices with LCD panelswhich operates in low-power.

Features

(1) Segment driver to expand LCD display capability for LC868364A.

(2) Internal RAM : 1280 × 8 bits

(3) Segment output port : 80 terminals
- Segment output direction : S01 → S80

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) LCD automatic display controller

- Display duty : 1/1 - 1/32 duty

- LCD control functions
  1. Number of display bits in horizontal direction control
  2. Vertical display scroll function : by changing the display start address
  3. Read/Write display RAM
  4. LCD drive frequency control

- Source clock of LCD controller : Crystal oscillator for low power consumption

- Clock for accessing registers and display RAM (R/W) : System clock from microcontroller.

(5) Power supply

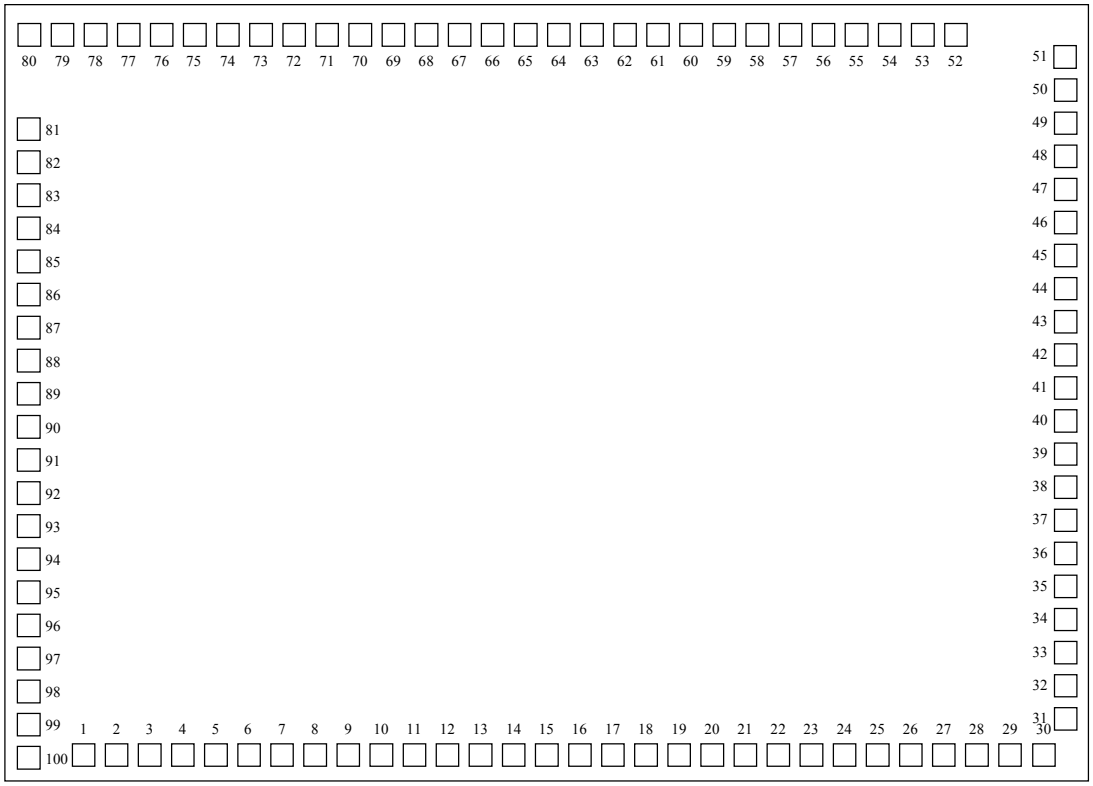
- Internal logic circuit 2.5V - 6.5V
- LCD driver 3.0V - 6.5V

(6) Shipping form

- Chip delivery form

Pad Assignment

Chip size (X × Y) : 4.04mm × 3.21mm
Thickness of chip : 480μm
Pad size : 105μm × 105μm
Pad pitch : 110μm



Pad name and Coordinates value

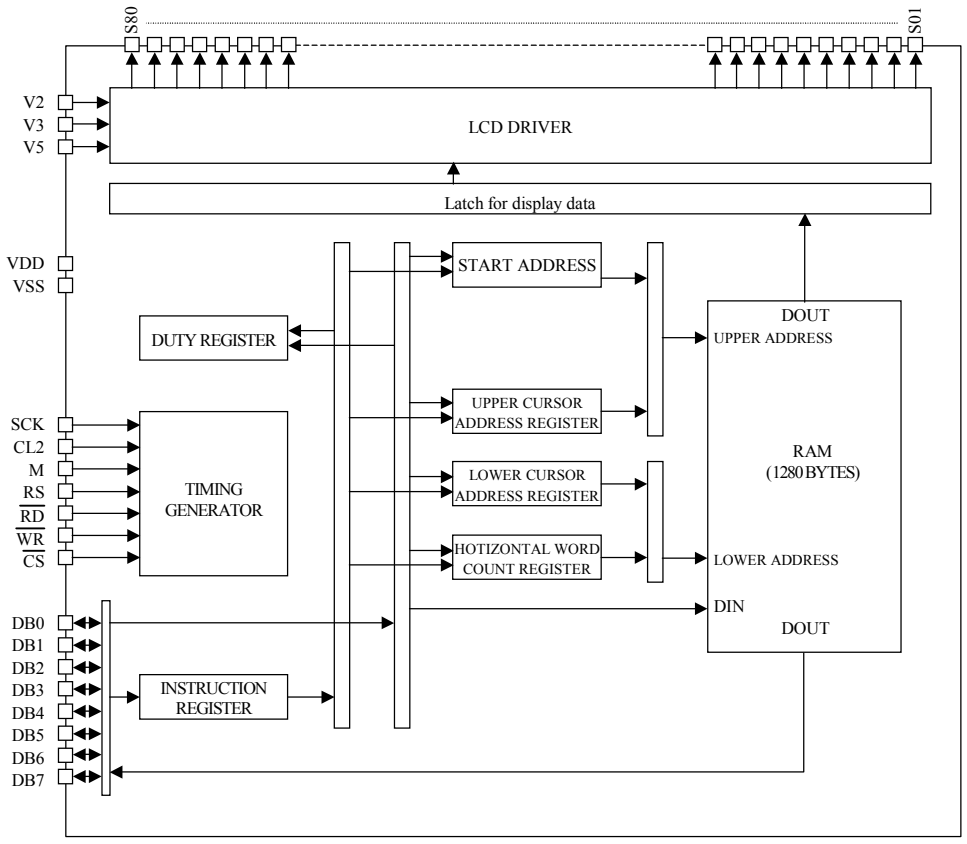
Pin No.	Pad No.	Name	Coordinates	
			Xμm	Yμm
1	1	S01	-1423	-1365
2	2	S02	-1313	-1365
3	3	S03	-1203	-1365
4	4	S04	-1093	-1365
5	5	S05	-983	-1365
6	6	S06	-873	-1365
7	7	S07	-763	-1365
8	8	S08	-653	-1365
9	9	S09	-543	-1365
10	10	S10	-433	-1365
11	11	S11	-323	-1365
12	12	S12	-213	-1365
13	13	S13	-103	-1365
14	14	S14	7	-1365
15	15	S15	117	-1365
16	16	S16	227	-1365
17	17	S17	337	-1365
18	18	S18	447	-1365
19	19	S19	557	-1365
20	20	S20	667	-1365
21	21	S21	777	-1365
22	22	S22	887	-1365
23	23	S23	997	-1365
24	24	S24	1107	-1365
25	25	S25	1218	-1365
26	26	S26	1328	-1365
27	27	S27	1438	-1365
28	28	S28	1548	-1365
29	29	S29	1658	-1365
30	30	S30	1768	-1365
31	31	S31	1780	-849
32	32	S32	1780	-739
33	33	S33	1780	-629
34	34	S34	1780	-519
35	35	S35	1780	-408
36	36	S36	1780	-298
37	37	S37	1780	-188
38	38	S38	1780	-78
39	39	S39	1780	32
40	40	S40	1780	142
41	41	S41	1780	252
42	42	S42	1780	362
43	43	S43	1780	472
44	44	S44	1780	582
45	45	S45	1780	692
46	46	S46	1780	802
47	47	S47	1780	912
48	48	S48	1780	1022
49	49	S49	1780	1132
50	50	S50	1780	1242

Pin No.	Pad No.	Name	Coordinates	
			Xμm	Yμm
51	51	S51	1780	1352
52	52	S52	1265	1364
53	53	S53	1155	1364
54	54	S54	1045	1364
55	55	S55	935	1364
56	56	S56	825	1364
57	57	S57	715	1364
58	58	S58	605	1364
59	59	S59	495	1364
60	60	S60	385	1364
61	61	S61	275	1364
62	62	S62	165	1364
63	63	S63	55	1364
64	64	S64	-55	1364
65	65	S65	-165	1364
66	66	S66	-275	1364
67	67	S67	-386	1364
68	68	S68	--496	1364
69	69	S69	-606	1364
70	70	S70	-716	1364
71	71	S71	-826	1364
72	72	S72	-936	1364
73	73	S73	-1046	1364
74	74	S74	-1156	1364
75	75	S75	-1266	1364
76	76	S76	-1376	1364
77	77	S77	-1486	1364
78	78	S78	-1596	1364
79	79	S79	-1706	1364
80	80	S80	-1816	1364
81	81	V2	-1753	909
82	82	V3	-1753	788
83	83	V5	-1753	668
84	84	VSS	-1753	548
85	85	DB0	-1753	428
86	86	DB1	-1753	308
87	87	DB2	-1753	188
88	88	DB3	-1753	68
89	89	DB4	-1753	-52
90	90	DB5	-1753	-172
91	91	DB6	-1753	-292
92	92	DB7	-1753	-412
93	93	VDD	-1753	-532
94	94	SCK	-1753	-652
95	95	$\overline{CS}$	-1753	-772
96	96	$\overline{RD}$	-1753	-892
97	97	$\overline{WR}$	-1753	-1012
98	98	RS	-1753	-1132
99	99	CL2	-1753	-1252
100	100	M	-1753	-1372

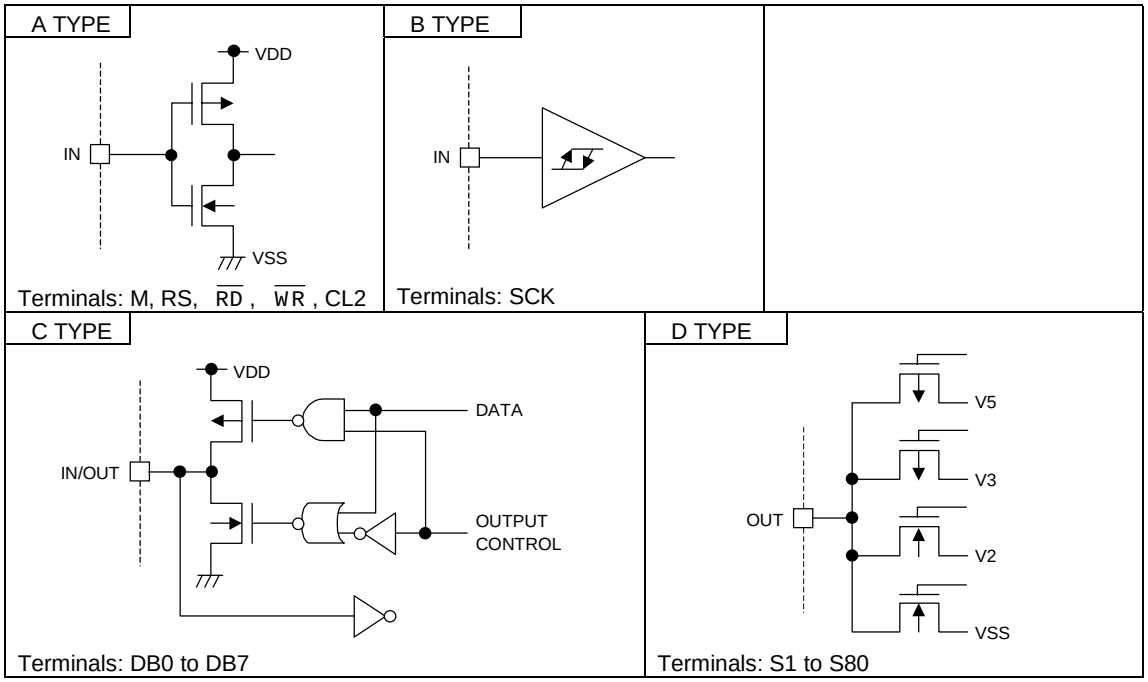
Notes:

- When using LC868920A in the form of chip, connect the substrate of chip to VSS or leave it open.

System Block Diagram



Terminal Form



Terminal Function Table

Terminal	Pin No.	Input/Output	Function Description
VSS	84	-	Negative power supply (-)
VDD	93	-	Positive power supply (+)
DB0 - DB7	85 - 92	Input/Output	Built-in Data bus Terminals for sending/receiving data to/from the MPU
SCK	94	Input	Clock for registers and display RAM access
$\overline{CS}$	95	Input	Chip select terminal : Enable when CS=0
$\overline{RD}$	96	Input	Read signal from LC868920A to LC868364A
$\overline{WR}$	97	Input	Write signal from LC868364A to LC868920A
RS	98	Input	Register selection RS=1 : Instruction register RS=0 : Data register
CL2	99	Input	LCD display signal (clock signal)
M	100	Input	LCD display signal (synchronization signal)
V2 V3 V5	81 82 83	- - -	LCD power supply
S1 - S80	1 - 80	Output	LCD segment drive output terminal

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Supply voltage	VDDMAX	VDD			-0.3	-	+7.0	V
LCD Input voltage	VNMAX	V2,V3,V5			VSS	-	+7.0	
Input voltage	VI(1)	$\overline{CS}$,$\overline{RD}$,$\overline{WR}$,RS, CL2,M,SCK			-0.3	-	VDD+0.3	
	VI(2)	DB0 to DB7 (Input mode)			-0.3		VDD+0.3	
Output voltage	VO(1)	S1 to S80			-0.3	-	V5+0.3	
	VO(2)	DB0 to DB7 (Output mode)			-0.3	-	VDD+0.3	
Maximum power consumption	Pdmax						200	mW
Operating temperature	Topr				-30	-	70	°C
Storage temperature	Tstg				-55	-	125	

*) The following condition has to be satisfied: $V5 \geq V3 \geq V2 \geq VSS$

2. Recommended Operating Range at Ta=-30 to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating supply voltage range	VDD	VDD	FSCK ≤ 6MHz		3.3		6.5	V
			FSCK ≤ 4MHz		2.7		6.5	
			FSCK ≤ 3MHz		2.4		6.5	
Supply voltage range in Hold mode	VHD	VDD	Keep RAM and register data in standby mode		2.0		6.5	
LCD supply voltage range	V5	V5			VSS		6.5	
High level input voltage	VIH(1)	DB0 to DB7 (Input mode) $\overline{CS}$,$\overline{RD}$,$\overline{WR}$,RS		4.5 - 6.5	0.75VDD		VDD	
				2.4 - 4.5	0.75VDD		VDD	
	VIH(2)	CL2,M,SCK		4.5 - 6.5	0.75VDD		VDD	
				2.4 - 4.5	0.75VDD		VDD	
Low level input voltage	VIL(1)	DB0 to DB7	Input mode	4.5 - 6.5	0		0.25VDD	
				2.4 - 4.5	0		0.25VDD	
	VIL(2)	$\overline{CS}$,$\overline{RD}$,$\overline{WR}$,RS		4.5 - 6.5	0		0.25VDD	
				2.4 - 4.5	0		0.25VDD	
	VIL(3)	CL2,M,SCK		4.5 - 6.5	0		0.25VDD	
				2.4 - 4.5	0		0.25VDD	
Input clock frequency	FCL2	CL2		2.4 - 6.5	32	32.768	33	kHz
	FSCK	SCK		2.4 - 6.5	0.3		3	MHz
				2.7 - 6.5	0.3		4	
				3.3 - 6.5	0.3		6	

Note:
The specifications above concerning recommended operating conditions and electrical characteristics assume the chip is in the QIP100E package. However, the LSI will be delivered in die form, not in a package. The specifications will be very similar for the die, however, depending on factors such as the board on which the chip is mounted, the bonding pressure, and the moulded plastic the characteristics will differ.
The ideal operating temperature for the above specifications is Ta= 25℃ ± 2℃.

3. Electrical Characteristics at Ta=-30 to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High level output voltage	VOH(1)	DB0 to DB7	• Output mode • IOH=-0.6mA	4.5 - 6.5	2.4		VDD	V
			• Output mode • IOH=-0.1mA	2.5 - 6.5	VDD-0.5		VDD	
Low level output voltage	VOL(1)	DB0 to DB7	• Output mode • IOL=+0.6mA	4.5 - 6.5	0		0.4	
			• Output mode • IOL=+0.1mA	2.5 - 6.5	0		0.4	
V5-Si drop voltage (i:1 to 80)	VD(1)	S1 to S80	• -90μA for each Si terminal • V5-VSS=5V	4.5 - 6.5			630	mV
			• -15μA for each Si terminal • V5-VSS=5V	2.5 - 6.5			120	
VX-Si drop voltage (X:2, 3) (i: 1 to 80)	VD(2)	S1 to S80	• -90μA for each Si terminal • V5-VSS=5V	4.5 - 6.5			200	
			• -15□μA for each Si terminal • V5-VSS=5V	2.5 - 6.5			120	
VSS-Si drop voltage (i:1 to 80)	VD(3)	S1 to S80	• +90μA for each Si terminal • V5-VSS=5V	4.5 - 6.5	-630			
			• +15μA for each Si terminal • V5-VSS=5V	2.5 - 6.5	-120			
Hysteresis voltage	VHIS	SCK		2.5 - 6.5		0.1VDD		V

4. Sample Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

The sample current dissipation characteristics shows the measurement result of Sanyo evaluation board.
The currents through the output transistors are ignored.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current consumption during normal operation	IDD(1)		• FCL2=32kHz • FSCK : stop • Figure 1 • V2=V3=V5=VSS	4.5 - 6.5		7	15	μA
				2.5 - 4.5		4	10	
	IDD(2)		• FCLK2=32kHz • FSCK : stop • Figure 4 • V5=5V, V3=3V, V2=2V	4.5 - 6.5		15	50	
				2.5 - 4.5		5	20	
Current consumption during READ/WRITE operation to RAM or registers	IDD(3)		• FCL2=32kHz • FSCK : 3MHz • Figure 2 • V2=V3=V5=VSS	4.5 - 6.5		170	300	
				3.0 - 4.5		100	200	
Current consumption during standby mode	IDD(4)		• FCL2=0Hz • FSCK : stop • Figure 3 • V2=V3=V5=VSS	4.5 - 6.5		0.05	30	
				2.5 - 4.5		0.02	20	

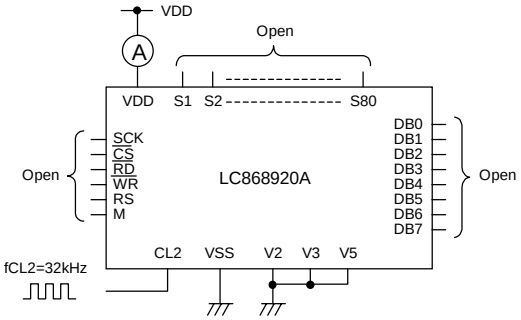


Figure 1 Current consumption measuring circuit during normal operation

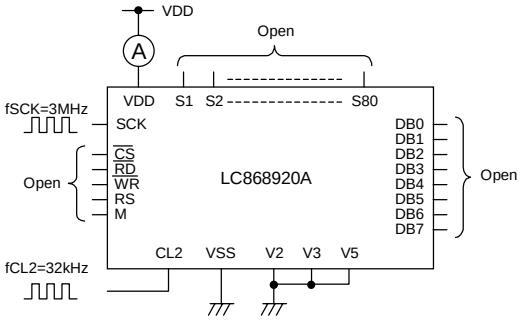


Figure 2 Current consumption measuring circuit during READ/WRITE operation to RAM or registers

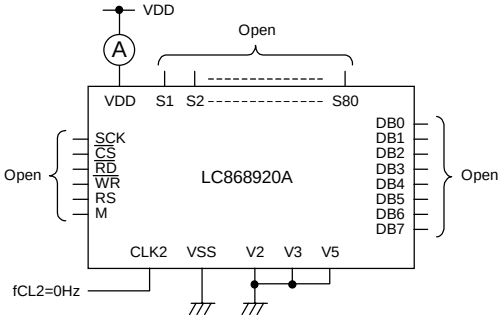


Figure 3 Current consumption measuring circuit during standby mode

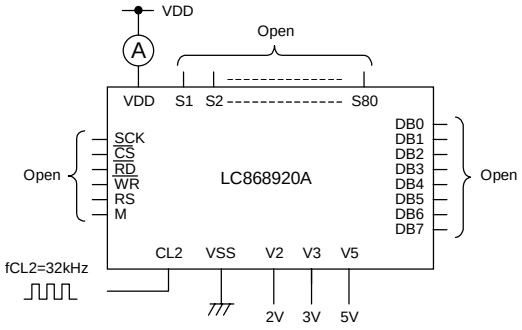
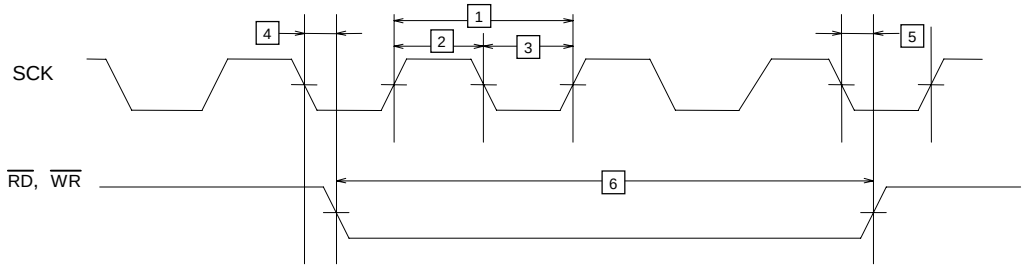


Figure 4 Current consumption measuring circuit during LCD operation

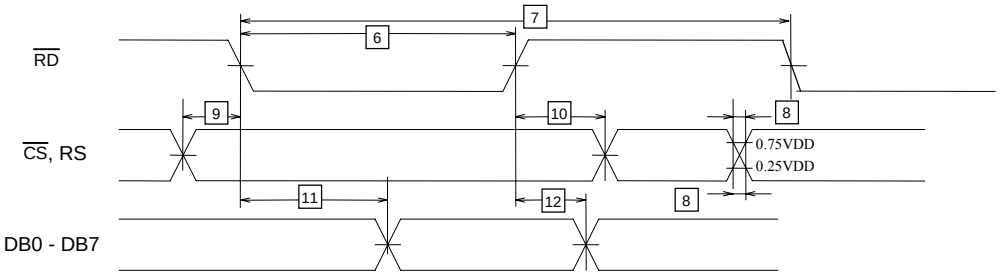
AC Characteristics at Ta=-30 to +70°C, VSS=0V

(1) MPU Interface

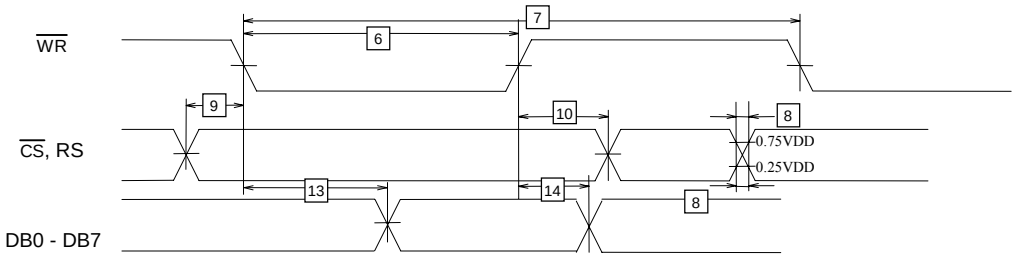
1. Read/write clock



2. Read cycle



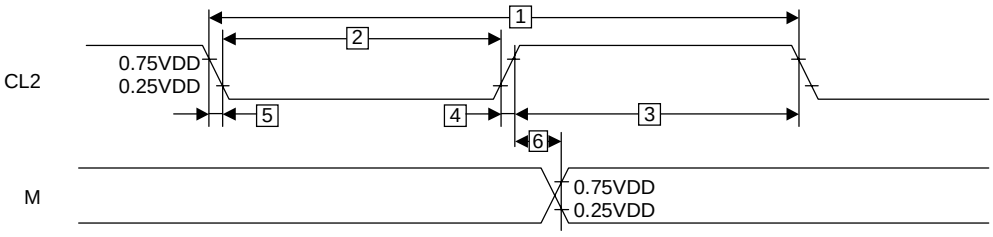
3. Write cycle



No	Item	Symbol	Conditions		Value		unit
				VDD	MIN	MAX	
1	SCK clock cycle	tsck	SCK	3.3 – 6.5	166	3340	ns
				2.7 – 6.5	249	3340	
				2.4 – 6.5	333	3340	
2	SCK_H width	pw1	SCK	2.4 – 6.5	0.45	0.55	tsck
3	SCK_L width	tr1,tf1	SCK	2.4 – 6.5	0.45	0.55	tsck
4	$\overline{RD}$, $\overline{WR}$ set-up time	tRS	SCK, $\overline{RD}$, $\overline{WR}$	4.5 - 6.5	5	40	ns
				2.4 - 4.5	5	100	
5	$\overline{RD}$, $\overline{WR}$ Hold time	tRH	SCK, $\overline{RD}$, $\overline{WR}$	4.5 - 6.5	5	40	ns
				2.4 - 4.5	5	100	
6	$\overline{RD}$, $\overline{WR}$ pulse width	pw1	$\overline{RD}$, $\overline{WR}$	2.4 – 6.5	3	6	tsck
7	ENABLE cycle time	tcyc1	$\overline{RD}$	2.4 – 6.5	12		tsck
		tcyc2	$\overline{WR}$	2.4 – 6.5	12		
8	Rising/Falling time	tr1, tf1	$\overline{RD}$	4.5 - 6.5		20	ns
				2.4 - 4.5		40	
9	Address set-up time	tAS1	$\overline{CS}$, RS, $\overline{RD}$	4.5 - 6.5	40		ns
				2.4 - 4.5	40		
		tAS2	$\overline{CS}$, RS, $\overline{WR}$	4.5 - 6.5	40		ns
				2.4 - 4.5	40		
10	Address Hold time	tAH1	$\overline{CS}$, RS, $\overline{RD}$	2.4 – 6.5	0.5		tsck
		tAH2	$\overline{CS}$, RS, $\overline{WR}$	2.4 – 6.5	0.5		
11	Data delay time	tDDR1	$\overline{RD}$, DB0 - DB7, CL=50pF	2.4 – 6.5		2	tsck
12	Data Hold time	tDHR1	$\overline{RD}$, DB0 - DB7, CL=50pF	4.5 - 6.5	20		ns
				2.4 – 6.5	20		
13	Data set-up time	tDSW1	$\overline{WR}$, DB0 - DB7, CL=50pF	2.4 – 6.5		1.5	tsck
14	Data Hold time	tDHW1	$\overline{WR}$, DB0 - DB7, CL=50pF	2.4 – 6.5	1		tsck

CL: Loading Capacity

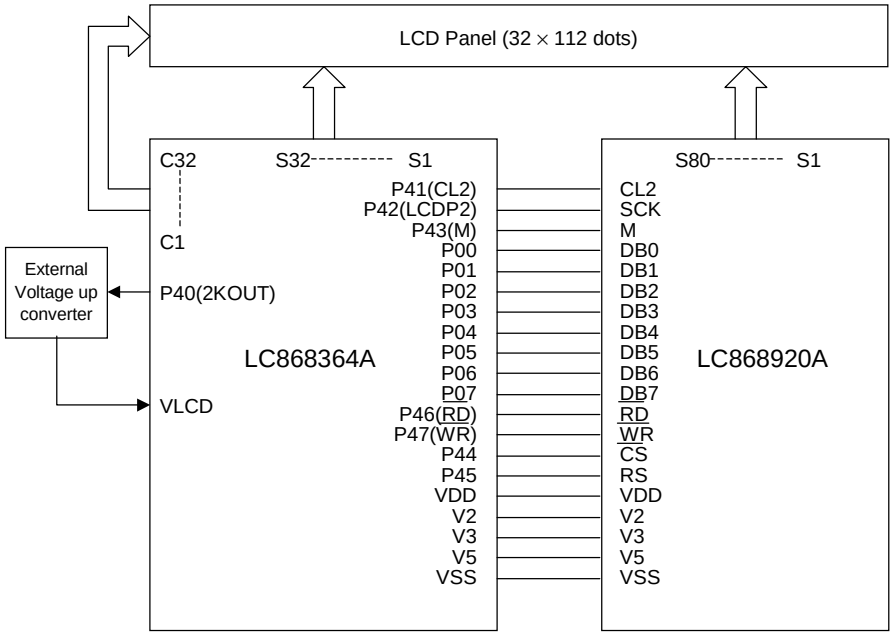
(2) Display Control Timing at Ta=-30 to +70°C, VSS=0V



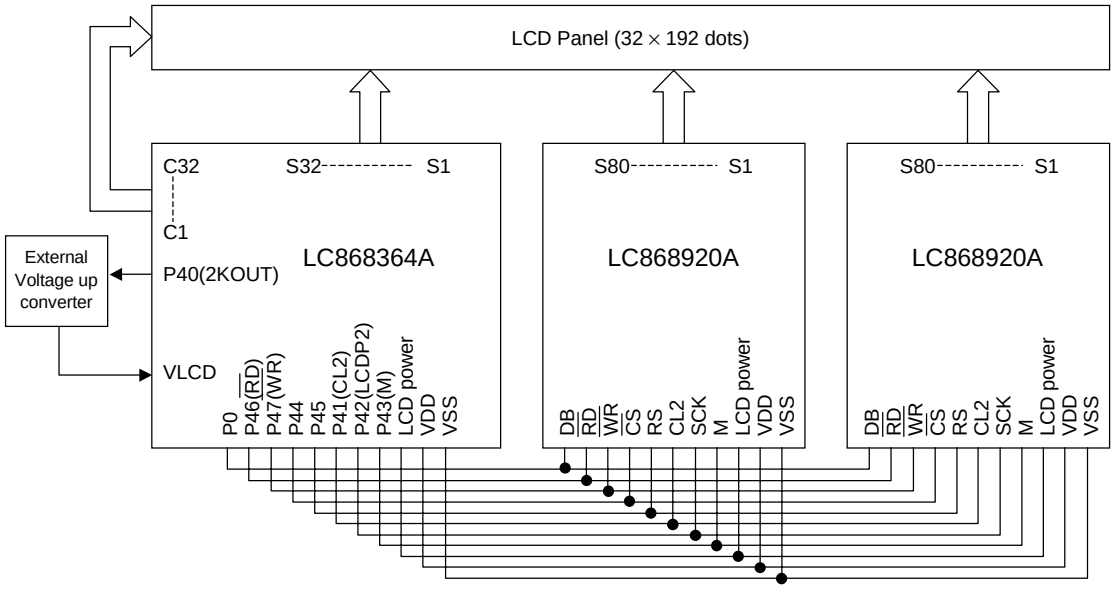
No	Item	Symbol	Conditions		Value		unit
				VDD	MIN	MAX	
1	Clock cycle	tCL2	CL2	2.4 - 6.5	30	31	µs
2	Low level pulse width	tWLCL2	CL2	2.4 - 6.5	13		µs
3	High level pulse width	tWHCL2	CL2	2.4 - 6.5	13		µs
4	Rising time	tr	CL2	4.5 - 6.5		20	ns
				2.4 - 4.5		50	
5	Falling time	tf	CL2	4.5 - 6.5		20	ns
				2.4 - 4.5		50	
6	M delay time	tDM	M	4.5 - 6.5		60	ns
				2.4 - 4.5		100	

Example circuit for reference

1. 32 × 112 dots



2. 32 × 192 dots

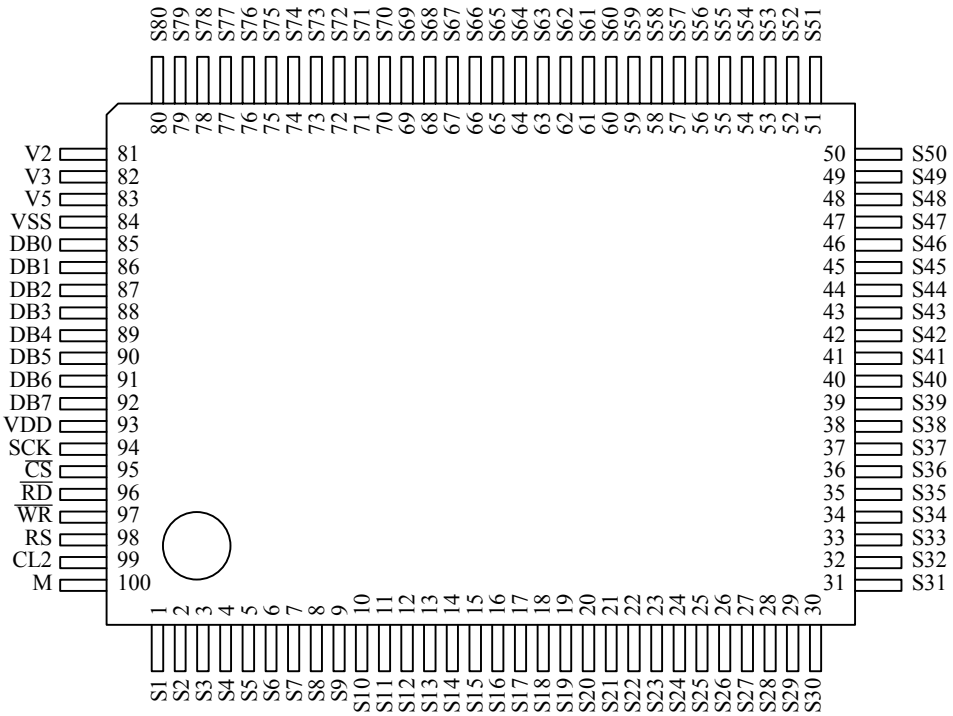


■ Evaluation Sample (ES)

Shipping Form: LC868920A: chip, Evaluation sample: QIP100E (shown below) or chip

If you use the ES in the package to design and fabricate an evaluation board, refer to the following pin assignment.

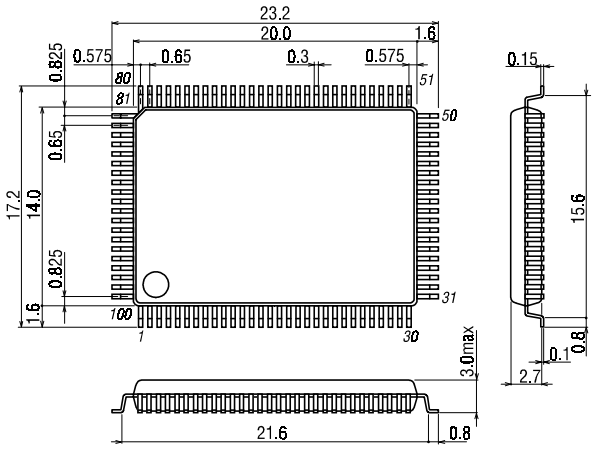
Terminal Assignment



Package Dimension

(unit : mm)

3151



SANYO : QIP-100E
(FLP100)

Functions

1. Interface control

The interface control block consists of the instruction register and the timing generator.

(Note) When accessing to registers or the display RAM of LC868920A, the system clock of LC868364A has to be either CF oscillation or RC oscillation. It will cause the irregular operation if the crystal oscillation is used in LC868364A when reading/writing data from/to LC868920A.
The STX instruction of LC868364A should be used to write data to LC868920A. The LDX instruction of LC868364A should be used to read data from LC868920A.

(1) Instruction register (4-bit data)

- When RS = '1', the lower 4-bits data of the eight bit data bus (DB0-DB7) is sent to this register.
- The following conditions have to be set to write data to the instruction register.
  1. $\overline{CS}$ = '0' : Enable the chip select.
  2. $\overline{WR}$ = '0' : Writing mode from LC868364A to LC868920A
  3. RS = '1' : Select the instruction register.
  4. Feed clock to SCK.
- The value of the instruction registers serves as the address of 7 kinds of data registers.
  The instruction register holds the data until the instruction code is rewritten. A list of instruction codes is shown below.

Instruction code				Description
DB3	DB2	DB1	DB0	
0	0	1	0	Select the horizontal word count register
0	0	1	1	Select the duty register
1	0	0	0	Select the start address register
1	0	1	0	Select the lower cursor address register
1	0	1	1	Select the upper cursor address register
1	1	1	0	Set the display data writing mode
1	1	1	1	Set the display data reading mode

Notes:

Don't write to the Test Register.
The Test Register can be specified by writing '00H' to the Instruction Register. However, setting any bits in this register will cause malfunction since this register is only used for testing.

(2) Writing to each data register

- The following indicates how to write data to the registers or the display RAM specified by the instruction register setting.
- The following conditions should be set to write data to each register or the display RAM.
  1. $\overline{CS}$ = '0' : Enable the chip select
  2. $\overline{WR}$ = '0' : Writing mode from LC868364A.to LC868920A
  3. RS = '0' : Select writing data
  4. Feed clock to SCK
- The data output from LC868364A through the 8 bits data bus (DB0 - DB7) is written to the register specified by the instruction register. (Data can not be written without a SCK clock signal.)
- By selecting the display data writing mode with the instruction register and setting the condition shown above, the output data from LC868364A through the data bus (DB0 - DB7) is written to the display RAM address specified by the cursor address. After the completion of writing, the cursor address is automatically decremeted by 1. Therefore, the data can be written contiguously to the display RAM.

(3) Reading display RAM

- Refer to "Section 2 Display control registers and display RAM (8)" about how to output the display RAM data to the data bus (DB0 - DB7).

- The following conditions are necessary to be set to read display RAM data.
  1. $\overline{CS}$ = '0' : Enable the chip select
  2. $\overline{RD}$ = '0' : Reading mode from LC868920A to LC868364A
  3. RS = '0' : Select the display RAM
  4. Feed clock to SCK.

- Each time data is read from the display RAM, the address of the display RAM (cursor address) is automatically decremented by 1.

(4) Timing generator

- The interface control block and the display are controlled by the timing signals and control signals generated in this circuit. The control signals and timing signals are used to transfer the data output from terminals DB0 - DB7 to the internal registers and to transfer data between terminals DB0 - DB7 and the display RAM. This circuit also produces the data input/output control signals and read/write timing signals.

2. Display control registers and display RAM

- The display is controlled by writing data to the instruction register and 7 internal data registers.

(1) LCD drive frequency

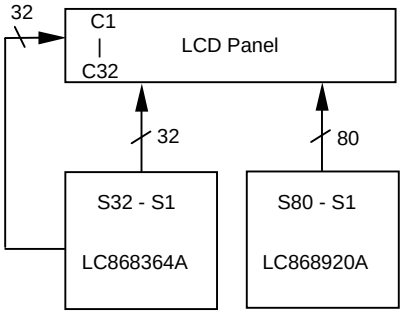
- DP indicates the number of clocks which is necessary to display 1 word (16 dots). DP is fixed to '2' in LC868920A.
- LC868920A is a segment driver to expand the LCD display capability for LC868364A. The common signal is output from LC868364A. Therefore, the number of dots to display a line may vary between the internal driver in microcontroller and the segment driver for expansion. Even if the number of display dots is different, the LCD driver frequency has to be the same on each side.

(Example 1) When selecting 32COM × 32SEG in LC868364A

The number of dots per line in microcontroller : 32 dots
The number of dots per line in LC868920A : 80 dots

The time required to display a line is the same for both the microcontroller and LC868920A by setting as follows.

LC868364A	: HP = 5	32 × 5 (Hp) = 160
LC868920A	: Dp = 2	80 × 2 (Dp) = 160



(Example 2) When selecting 16COM in LC868364A

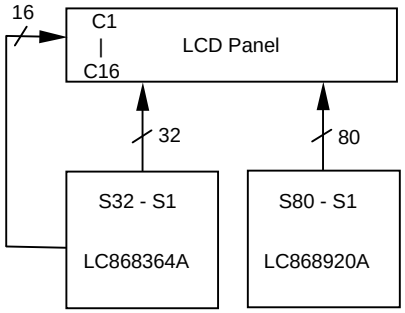
The number of dots per line in LC868920A : 80 dots

80×2 (DP) = 160

It is necessary to set as follows to have the same time required to display a line in LC868364A as in LC868920A.

32×5 (Hp) = 160

(Note) If 16COM is selected in LC868364A and LC868920A is used to expand segments, S1 to S32 segments can only be used in LC868364A and segments S33 to S48 can not be used. HP = 5 should be set to LC868364A by program.



(Note)
S33 to S48 can not be used.

(2) Horizontal word count register

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	0	0	1	0
Horizontal word count register	1	0	0	-	-	-	-	Dn-1			

- This register sets the number of horizontal words.
- Dn indicates the number of words in horizontal direction.
- The total number of horizontal dots on the LCD panel (n) is given by the following formula.

  $n = 8 \times (Dn \times 2)$ $(n \leq 80)$
- 1 to 5 (in decimal) can be set as Dn.
- The relation between the total number of horizontal dots (n), the number of horizontal words (Dn) and register settings is shown below.

Total number of horizontal dots (n)	Dn	DB2	DB1	DB0
16	1	0	0	0
32	2	0	0	1
48	3	0	1	0
64	4	0	1	1
80	5	1	0	0

(3) Duty register

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	0	0	1	1
Divider ratio register	1	0	0	0	0	Nx-1					

- This register sets the divider ratio (Nx). (Display duty = 1/Nx)
- Nx represents the divider ratio of display and 1/Nx indicates a display duty.
- 2 to 32 (in decimal) can be set as Nx.

(4) Start address register

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	1	0	0	0
Start address register	1	0	0	0	Start Address (STAD)						

- This register sets the value of display start line address.
- The display start line address shows the RAM line address of the data to be displayed in the top line on the LCD panel.
- The start address counter is a 7-bit down-counter with a preset function.
- The start address (STAD) is set to the start address counter as an initial value.
- The start address counter is decremented by 1 each time the display of a line in horizontal direction is completed on the screen.
- The start address counter takes the value 7FH on the next decrement after 0.

(5) Lower cursor address register

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	1	0	1	0
Cursor address counter (lower byte)	1	0	0	0	0	0	0	Lower cursor address (CAL)			

- Set the lower address used to read/write data from/to the display RAM in this register.
- The lower cursor address counter is a 4-bit down-counter with a preset function.
- The lower cursor address (CAL) is set to the counter as an initial value.
- This counter is decremented by 1 each time the RAM is accessed.
- If RAM is accessed when the value of this counter is "0", then Dn-1 is automatically set.
- 0 to 9 (in decimal) can be set as a lower cursor address.

(6) Upper cursor address register

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	1	0	1	1
Cursor address counter (upper byte)	1	0	0	0	Upper cursor address (CAH)						

- Set the upper addresses used to read/write data from/to the display RAM in this register.
- The upper cursor address counter is a 7-bit down-counter with a preset function.
- This counter is decremented by 1 each time the lower cursor address counter generates the underflow.
- The cursor address is written to the cursor address counter by setting data to the lower and upper cursor address registers.
- The cursor address indicates the RAM address to access display data. The data of the address specified by the cursor address is read /written from/to the display RAM.
- The cursor address consists of the 4-bit lower address and 7-bit upper address.

(7) Display RAM

a.) Writing data to Display RAM

Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	1	1	1	0
RAM	1	0	0	MSB	Display pattern data						LSB

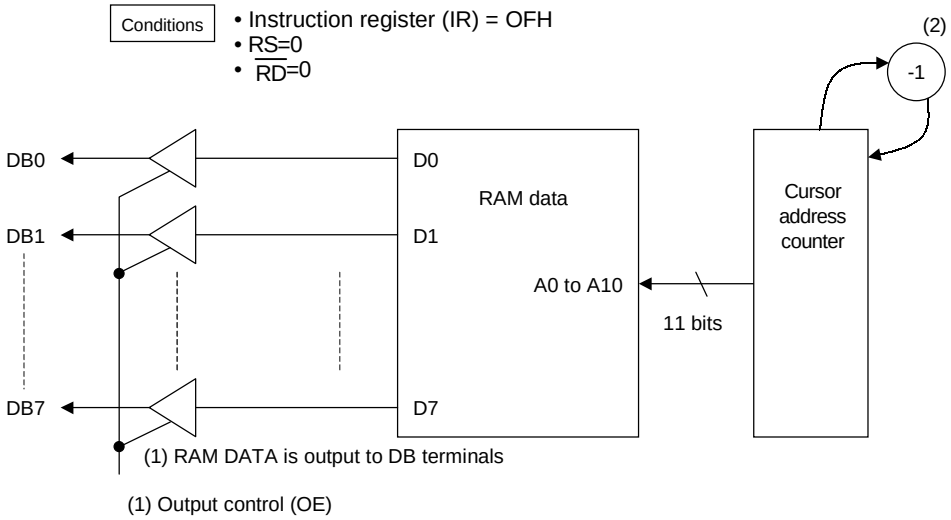
- Select the display data writing mode by setting "0EH" to the instruction register. Then set RS = 0 and write 8-bit data to the display RAM.
  The display pattern data is written to the RAM address specified by the cursor address. After writing data to RAM, the cursor address counter is automatically decremented by 1.

b.) Reading data from display RAM

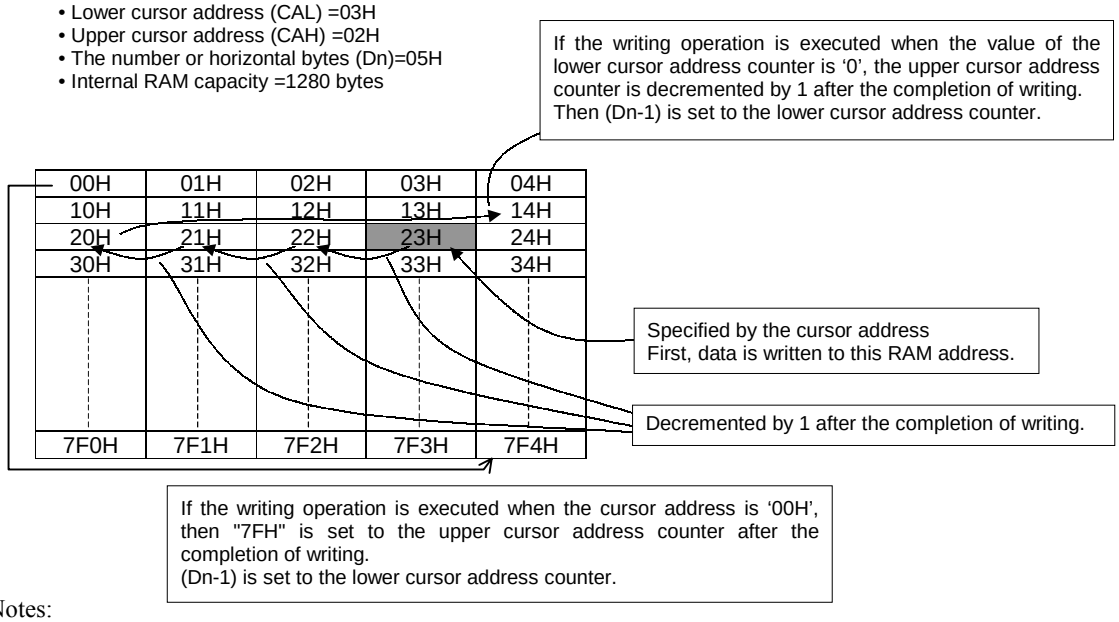
Register	$\overline{RD}$	$\overline{WR}$	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction register	1	0	1	0	0	0	0	1	1	1	1
RAM	0	1	0	MSB			Display pattern data				LSB

- Select the display data reading mode by setting '0FH' to the instruction register. Then set RS=0 and select the display RAM.
- The procedure of reading RAM data is as follows:
  (1) The RAM data of the address specified by the cursor address is output to DB0 to DB7 terminals by setting as shown above.
  (2) The cursor address counter is decremented by 1.

The following figure indicates the procedure of reading RAM data.



e.x.) Writing (reading) data to (from) display RAM
- Lower cursor address (CAL) =03H
- Upper cursor address (CAH) =02H
- The number or horizontal bytes (Dn)=05H
- Internal RAM capacity =1280 bytes



Notes:

Don't write to the Test Register.

The Test Register can be specified by writing '00H' to the Instruction Register. However, setting any bits in this register will cause malfunction since this register is only used for testing.

3. LCD driver

- 4 levels of the LCD driving voltage (V5, V3, V2, and VSS) are externally supplied. The LCD driving voltage level to be output to the segment drivers S1 to S80 vary according to the contents of the display data latch and the synchronous signal (M signal).
- The 8-bit data output from the display RAM is input to the display data latch. The input 8-bit data is latched in the display data latch for the number of bytes specified by the horizontal byte count register. This operation is repeated for the number of times that is determined by the divide ratio number.
- The LCD display voltage has to be supplied to V2, V3 and V5 terminals after all data is set to LCD display data registers and the display RAM. After power is on, if the LCD display voltage is supplied to V2, V3, and V5 terminals without setting data to the internal registers and the display RAM, uncertain display is appeared on LCD panel. Thus, supply the VSS level to V2, V3 and V5 terminals until all data required to display is set to data registers and the display RAM.
  (Actually, the LCD display voltage is supplied to this circuit from LC868364A microcontroller. Therefore, turn OFF the LCD display in LC868364A until data is set to the internal registers and the display RAM in LC868920A)

Display examples

(1) Display mode control register=01H (LCD: ON)
The total number of horizontal dots=80 (Dn=5)
Divider ratio (Nx)=32
Start address register=1FH

	S80 - - - - S73	S72 - - - - S65	S64 - - - S57	S56 - - - S49	S48 - - - S41	S40 - - - S33	S32 - - - - S25	S24 - - - S17	S16 - - - - S9	S8 - - - - - S1
C1 →	MSB (1F0H) LSB	MSB (1F1H) LSB	MSB (1F2H) LSB	MSB (1F3H) LSB	MSB (1F4H) LSB	MSB (1F5H) LSB	MSB (1F6H) LSB	MSB (1F7H) LSB	MSB (1F8H) LSB	MSB (1F9H) LSB
C2 →	MSB (1E0H) LSB	MSB (1E1H) LSB	MSB (1E2H) LSB	MSB (1E3H) LSB	MSB (1E4H) LSB	MSB (1E5H) LSB	MSB (1E6H) LSB	MSB (1E7H) LSB	MSB (1E8H) LSB	MSB (1E9H) LSB
C3 →	MSB (1D0H) LSB	MSB (1D1H) LSB	MSB (1D2H) LSB	MSB (1D3H) LSB	MSB (1D4H) LSB	MSB (1D5H) LSB	MSB (1D6H) LSB	MSB (1D7H) LSB	MSB (1D8H) LSB	MSB (1D9H) LSB
⋮										
C28→	MSB (040H) LSB	MSB (041H) LSB	MSB (042H) LSB	MSB (043H) LSB	MSB (044H) LSB	MSB (045H) LSB	MSB (046H) LSB	MSB (047H) LSB	MSB (048H) LSB	MSB (049H) LSB
C29→	MSB (030H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C30→	MSB (020H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C31→	MSB (010H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C32→	MSB (000H) LSB	MSB (001H) LSB	MSB (002H) LSB	MSB (003H) LSB	MSB (004H) LSB	MSB (005H) LSB	MSB (006H) LSB	MSB (007H) LSB	MSB (008H) LSB	MSB (009H) LSB

(2) Display mode control register=01H (LCD: ON)
The total number of horizontal dots=80 (Dn=5)
Divider ratio (Nx)=32
Start address register=1EH

	S80 - - - S73	S72 - - - S65	S64 - - - S57	S56 - - - S49	S48 - - - S41	S40 - - - S33	S32 - - - S25	S24 - - - S17	S16 - - - - S9	S8 - - - - S1
C1 →	MSB (1E0H) LSB	MSB (1E1H) LSB	MSB (1E2H) LSB	MSB (1E3H) LSB	MSB (1E4H) LSB	MSB (1E5H) LSB	MSB (1E6H) LSB	MSB (1E7H) LSB	MSB (1E8H) LSB	MSB (1E9H) LSB
C2 →	MSB (1D0H) LSB	MSB (1D1H) LSB	MSB (1D2H) LSB	MSB (1D3H) LSB	MSB (1D4H) LSB	MSB (1D5H) LSB	MSB (1D6H) LSB	MSB (1D7H) LSB	MSB (1D8H) LSB	MSB (1D9H) LSB
C3 →	MSB (1C0H) LSB	MSB (1C1H) LSB	MSB (1C2H) LSB	MSB (1C3H) LSB	MSB (1C4H) LSB	MSB (1C5H) LSB	MSB (1C6H) LSB	MSB (1C7H) LSB	MSB (1C8H) LSB	MSB (1C9H) LSB
⋮										
C28→	MSB (030H) LSB	MSB (041H) LSB	MSB (042H) LSB	MSB (043H) LSB	MSB (044H) LSB	MSB (045H) LSB	MSB (046H) LSB	MSB (047H) LSB	MSB (048H) LSB	MSB (049H) LSB
C29→	MSB (020H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C30→	MSB (010H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C31→	MSB (000H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C32→	MSB (7F0H) LSB	MSB (7F1H) LSB	MSB (7F2H) LSB	MSB (7F3H) LSB	MSB (7F4H) LSB	MSB (7F5H) LSB	MSB (7F6H) LSB	MSB (7F7H) LSB	MSB (7F8H) LSB	MSB (7F9H) LSB

(3) Display mode control register=01H (LCD: ON)

The total number of horizontal dots=80 (Dn=5)
Divider ratio (Nx)=16
Start address register=0FH

	S80 - - - S73	S72 - - - S65	S64 - - - S57	S56 - - - S49	S48 - - - S41	S40 - - - S33	S32 - - - S25	S24 - - - S17	S16 - - - - S9	S8 - - - - - S1
C1 →	MSB (0F0H) LSB	MSB (0F1H) LSB	MSB (0F2H) LSB	MSB (0F3H) LSB	MSB (0F4H) LSB	MSB (0F5H) LSB	MSB (0F6H) LSB	MSB (0F7H) LSB	MSB (0F8H) LSB	MSB (0F9H) LSB
C2 →	MSB (0E0H) LSB	MSB (0E1H) LSB	MSB (0E2H) LSB	MSB (0E3H) LSB	MSB (0E4H) LSB	MSB (0E5H) LSB	MSB (0E6H) LSB	MSB (0E7H) LSB	MSB (0E8H) LSB	MSB (0E9H) LSB
C3 →	MSB (0D0H) LSB	MSB (0D1H) LSB	MSB (0D2H) LSB	MSB (0D3H) LSB	MSB (0D4H) LSB	MSB (0D5H) LSB	MSB (0D6H) LSB	MSB (0D7H) LSB	MSB (0D8H) LSB	MSB (0D9H) LSB
⋮										
C12→	MSB (040H) LSB	MSB (041H) LSB	MSB (042H) LSB	MSB (043H) LSB	MSB (044H) LSB	MSB (045H) LSB	MSB (046H) LSB	MSB (047H) LSB	MSB (048H) LSB	MSB (049H) LSB
C13→	MSB (030H) LSB	MSB (031H) LSB	MSB (032H) LSB	MSB (033H) LSB	MSB (034H) LSB	MSB (035H) LSB	MSB (036H) LSB	MSB (037H) LSB	MSB (038H) LSB	MSB (039H) LSB
C14→	MSB (020H) LSB	MSB (021H) LSB	MSB (022H) LSB	MSB (023H) LSB	MSB (024H) LSB	MSB (025H) LSB	MSB (026H) LSB	MSB (027H) LSB	MSB (028H) LSB	MSB (029H) LSB
C15→	MSB (010H) LSB	MSB (011H) LSB	MSB (012H) LSB	MSB (013H) LSB	MSB (014H) LSB	MSB (015H) LSB	MSB (016H) LSB	MSB (017H) LSB	MSB (018H) LSB	MSB (019H) LSB
C16→	MSB (000H) LSB	MSB (001H) LSB	MSB (002H) LSB	MSB (003H) LSB	MSB (004H) LSB	MSB (005H) LSB	MSB (006H) LSB	MSB (007H) LSB	MSB (008H) LSB	MSB (009H) LSB

(4) Display mode control register=01H (LCD: ON)

The total number of horizontal dots=64 (Dn=4)
Divider ratio (Nx)=16
Start address register=1FH

	S64 - - - S57	S56 - - - S49	S48 - - - S41	S40 - - - S33	S32 - - - S25	S24 - - - S17	S16 - - - - S9	S8 - - - - S1
C1 →	MSB (1F0H) LSB	MSB (1F1H) LSB	MSB (1F2H) LSB	MSB (1F3H) LSB	MSB (1F4H) LSB	MSB (1F5H) LSB	MSB (1F6H) LSB	MSB (1F7H) LSB
C2 →	MSB (1E0H) LSB	MSB (1E1H) LSB	MSB (1E2H) LSB	MSB (1E3H) LSB	MSB (1E4H) LSB	MSB (1E5H) LSB	MSB (1E6H) LSB	MSB (1E7H) LSB
C3 →	MSB (1D0H) LSB	MSB (1D1H) LSB	MSB (1D2H) LSB	MSB (1D3H) LSB	MSB (1D4H) LSB	MSB (1D5H) LSB	MSB (1D6H) LSB	MSB (1D7H) LSB
⋮								
C12→	MSB (140H) LSB	MSB (141H) LSB	MSB (142H) LSB	MSB (143H) LSB	MSB (144H) LSB	MSB (145H) LSB	MSB (146H) LSB	MSB (147H) LSB
C13→	MSB (130H) LSB	MSB (131H) LSB	MSB (132H) LSB	MSB (133H) LSB	MSB (134H) LSB	MSB (135H) LSB	MSB (136H) LSB	MSB (137H) LSB
C14→	MSB (120H) LSB	MSB (121H) LSB	MSB (122H) LSB	MSB (123H) LSB	MSB (124H) LSB	MSB (125H) LSB	MSB (126H) LSB	MSB (127H) LSB
C15→	MSB (110H) LSB	MSB (111H) LSB	MSB (112H) LSB	MSB (113H) LSB	MSB (114H) LSB	MSB (115H) LSB	MSB (116H) LSB	MSB (117H) LSB
C16→	MSB (100H) LSB	MSB (101H) LSB	MSB (102H) LSB	MSB (103H) LSB	MSB (104H) LSB	MSB (105H) LSB	MSB (106H) LSB	MSB (107H) LSB