Ordering number:ENN3945A

CMOS IC

LC83010N, 83010NE

Audio Digital Signal Processor

Overview

The LC83010N, 83010NE is a single-chip digital signal processor (DSP). It is designed for use in the application fields such as a digital processing of audio signals.
The LC83010N, 83010NE CMOS processor has various on-chip filtering circuits such as a graphic equalizer for reproduction of sound quality. It also has simulation circuit for reverberation (sound reflection and echo), so that sound field with surround and delay can be created.

The LC83010N and LC83010NE are upgraded versions of the LC83010 and the LC83010E. The LC83010N and LC83010NE have a 64fs clock output that enables improved interfacing with external A/D converters. TEST5 has been renamed FS640/T5 and incorporates both the new clock output and the original test output.

Features

LSI functions

- Dual Harvard Architecture: Enables simultaneous processing (multiply and addition) of stereo signals in a single instruction cycle.
  The LC83010N, LC83010NE processor has the following two independent units:
  · Multiplier : 24 bits × 16 bits (fixed-point decimal)
  · ALU : 32-bit arithmetic calculation, 24-bit arithmetic and logical operations.
  · ACCumulator (ACC) : 32 bits
  · Temporal Registers (TMP0 to TMP7) : 32-bit for each
  · Internal Memory Data RAM 128 × 24 bits
  Coefficient RAM 256 × 16 bits
  Constant ROM 256 × 24 bits
- Program memory Capacity (RAM) : 320 × 32 bits
- A variety of I/O interfaces.
  · Audio signal I/O :
  1 channel for input (applicable to various formats)
  3 channel for output (applicable to up to 4 types of data format)
  · Surround DRAM access signal :
  16 accesses/CH Max. (within 1 fs)
  Up to 2 256K (64K × 4 bits) DRAMs or 1M (256K × 4 bits) DRAMs can be directly connected to this chip.
  · Uses external DRAMS with RAS access times of 120 ns or lower.
  · Serial input/output interface with a microcomputer.
  Synchronous 8-bit serial input : 1
  [Mail box (16 bits × 8) function available]
  Synchronous 8-bit serial output : 1
- Interrupt function (Vectored interrupt with the INT pin)
- Stack Nesting Levels : 4
- On-chip Interval Timer :
  12 bits (timer clock = sampling frequency)
- Cycle time : 108ns (sampling frequency = 48kHz)
- Single 5V power supply.
- Package : 64-pin DIPs (LC83010N).
  80-pin QFPs (LC83010NE).
  Note) When soldering QFP devices, do not use the solder dip method.
- Evaluation chip : LC83EV010N (PGA100)
  · Applications
  · Graphic Equalizer
  · Power calculation for spectrum analyzer display
  · Sound field creation (using external DRAMs)
  · 4 Speakers + REC output

Development Environment

- Software Tools
  · Assembler
  · Debugger with simulation
- Hardware Tools
  · IBM PC-AT compatible machines or AX personal computers
  · In Circuit Emulator (ICE)

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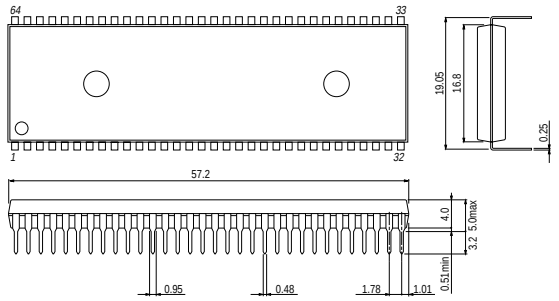
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

unit:mm

3071-DIP64S

[LC83010N]

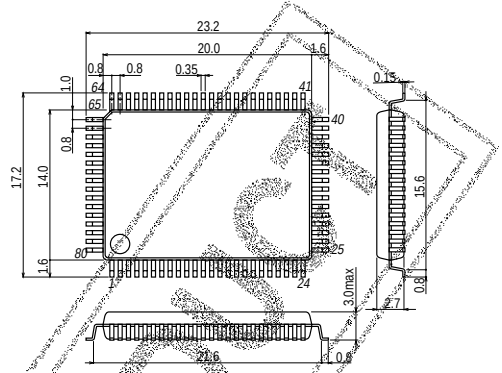


SANYO : DIP64S

unit:mm

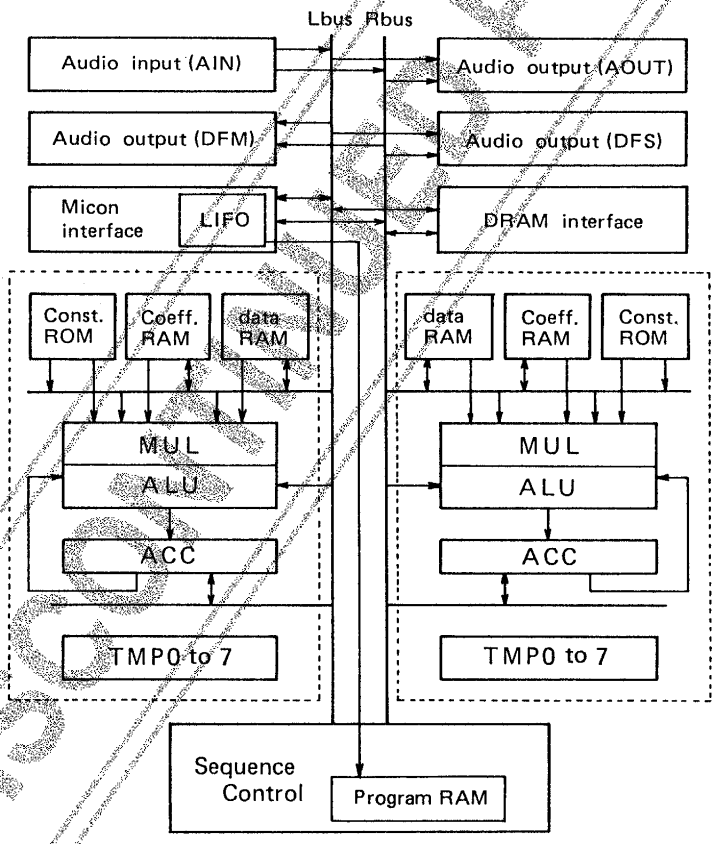
3174-QIP80E

[LC83010NE]



SANYO : QIP80E

Block Diagram



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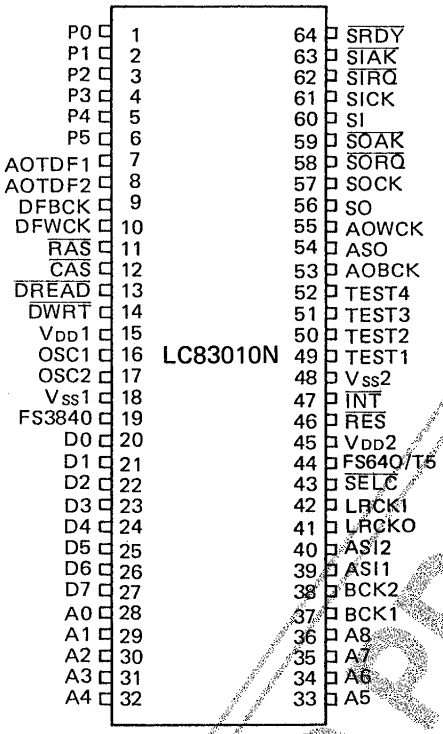
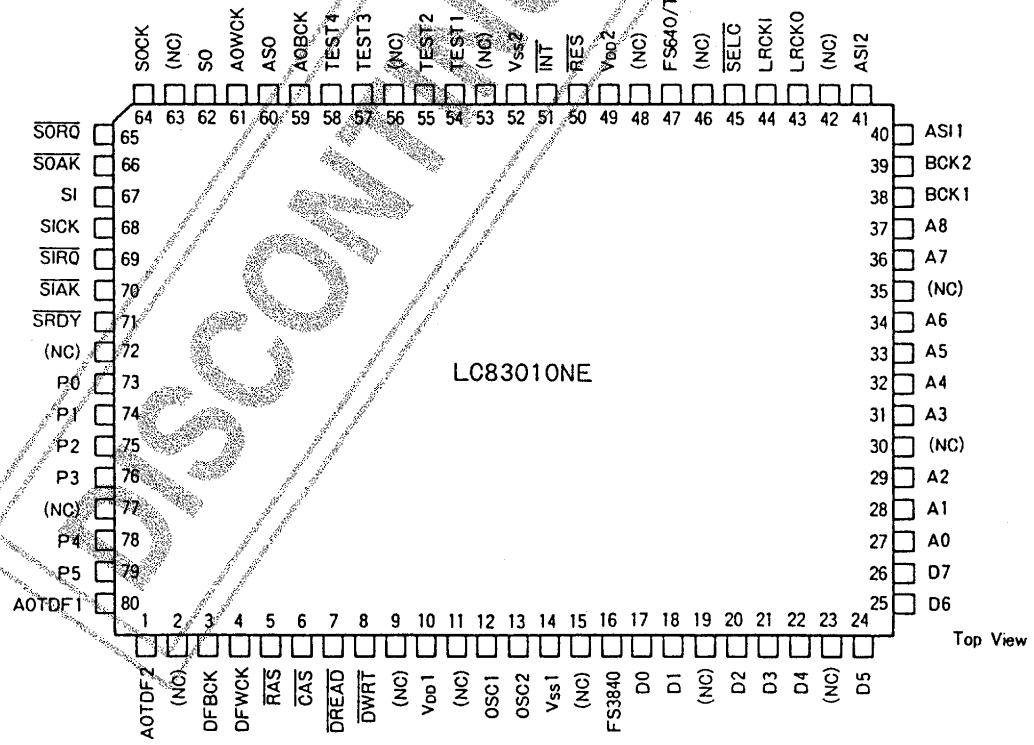
Pin Assignments

(DIP64S)



Top view

(QIP80E)



Top View

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Pin Function

	Pin Name	I/O	Functional Description
	V_{DD}1, 2	I	+5V power supply pins (These pins should be connected to the positive power source.)
	V_{SS}1, 2	I	GND power supply pins (These pins should be connected to the ground level.)
Audio I/F (Interface)	ASI1	I	Audio data serial input 1
	ASI2	I	Audio data serial input 2
	BCK1	I	Bit clock input pin for ASI1 data
	BCK2	I/O	Bit clock input pin for ASI2 data (I/O selectable by CR)
	LRCKI	I	Input pin for L/R channel distinguish signal (H: L channel data ; L: R channel data)
	LRCKO	O	Input pin for L/R channel distinguish signal (H: L channel data ; L: R channel data)
	ASO	O	Audio data serial output
	AOBCK	O	Bit clock output pin for ASO data (for 32fs and 48fs)
	AOWCK	O	Word clock output pin for ASO data
	AOTDF1	O	Serial output pin for audio data (for high presence 1)
	AOTDF2	O	Serial output pin for audio data (for high presence 2)
	DFBCK	O	Bit clock output pin for AOTDF1 and AOTDF2 data (for 32fs and 48fs)
	DFWCK	O	Word clock output pin for AOTDF1 and AOTDF2 data
DRAM I/F	$\overline{RAS}$	O	Output pin for RAS signal to external DRAMs
	$\overline{CAS}$	O	Output pin for CAS signal to external DRAMs
	$\overline{DREAD}$	O	Output pin for data read signal to external DRAMs
	$\overline{DWRT}$	O	Output pin for data write signal to external DRAMs
	A0 to 8	O	Output pins for address signals to external DRAMs (64K × 4 bits: A0 to A7, 256K × 4 bits: A0 to A8)
	D0 to 7	I/O	Input/output pins for data transfer with external DRAMs. In the single DRAM configuration mode, pins D0 to D3 are used. In the double DRAM configuration mode, pins D0 to D7 are used.
Microcomputer I/F	SI	I	Input pin for serial data from control microcomputer (8-bit serial data)
	SICK	I	Serial clock input pin for SI data
	$\overline{SIRQ}$	I	Request signal input pin for serial data input
	$\overline{SIAK}$	O	Output pin for Acknowledge response to the input request signal from a microcomputer
	$\overline{SRDY}$	I	Input pin for a Ready signal from a controlling microcomputer indicating the end of a data transfer
	SO	O	Output pin for serial data to a controlling microcomputer (8-bit serial data)
	SOCK	I	Serial clock input pin for SO data
	$\overline{SORQ}$	I	Request signal input pin for serial data output
	$\overline{SOAK}$	O	Output pin for Acknowledge response to the output request signal from a microcomputer
	P0 to 5	I/O	General-purpose Input/Output ports (with on-chip pull-up resistor)
	OSC1	I	Pin for connection with a crystal oscillator or for clock input from an external source. (384fs)
	OSC2	O	Pin for connection with a crystal oscillator (should be left open in external clock input mode)
Control pins	FS384O	O	384fs output pin
	$\overline{INT}$	I	Interrupt request input pin (with on-chip pull-up resistor)
	$\overline{RES}$	I	Reset input pin (with on-chip pull-up resistor)
	$\overline{SELC}$	I	L/R channel signal select input pin with on-chip pull-down resistor ; L: external (LRCKI), H: internal (internal divider output)
	TEST 1 to 4	I	Test signal input pins. Normally, these pins should be connected to the ground level.
	FS64O/T5	O	Test signal output pins. 64fs clock output/test output. FS64O/T5 funcitons as a test output in test mode and as a 64fs clock output for external A/D converters during normal operation.

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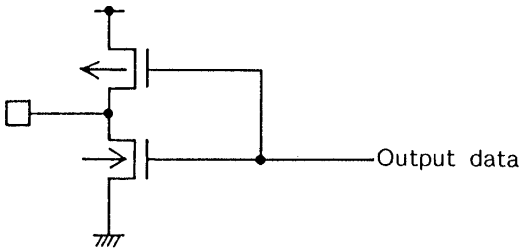
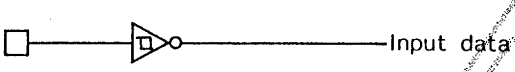
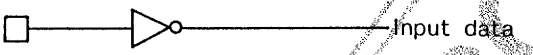
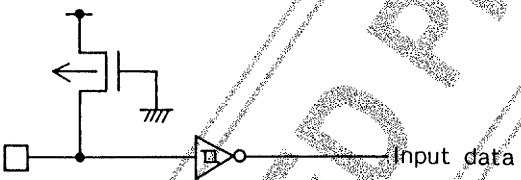
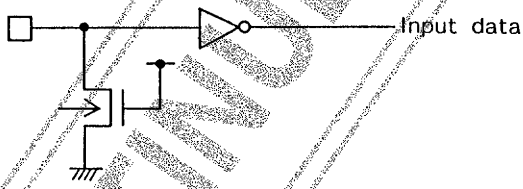
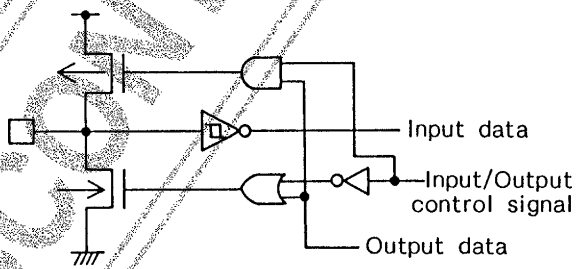
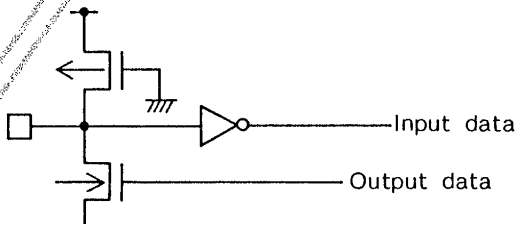
Pin Configuration Types

Level specification	Circuit type	Pin Name
TTL level output		ASO, AOBCK AOWCK, LRCKO, AOTDF1, AOTDF2, DFWCK, A0 to A8, FS384O, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$, FS64O/T5
CMOS medium level current output		SO, $\overline{SOAK}$, $\overline{SIAK}$
Schmitt input		$\overline{SOCK}$, SI, SICK, $\overline{SORQ}$, $\overline{SIRQ}$, SRDY
L level Schmitt input		BCK1, ASI1, ASI2, LRCKI
Normal input		TEST1 to 4
Input with internal pull-up resistor		$\overline{RES}$, $\overline{INT}$
Input with internal pull-down resistor		$\overline{SELC}$
TTL level output Low level Schmitt input		BCK2, D0 to D7
Pu MOS medium current output Normal input		P0 to P5

DISCONTINUED PRODUCT

Specifications

Absolute Maximum Ratings at Ta = 25˚C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{DD}max		−0.3 to +7.0	V	
Output voltage	V01	OSC2 output	Up to the voltage produced by oscillation	V	
	V02	Pins except for the OSC2	−0.3 to V_{DD} +0.3	V	
Input voltage	V_{IN}		−0.3 to V_{DD} +0.3	V	
Peak output current	$I_{OP}1$	Audio I/F, DRAM I/F	−2 to +4	mA	1
	$I_{OP}2$	Microcomputer I/F	−2 to +10	mA	2
	$I_{OP}3$	P0 to P5	−0.5 to +10	mA	3
Average output current	$I_{OA}1$	Audio I/F: Per pin	−2 to +4	mA	4
	$I_{OA}2$	Audio I/F, DRAM I/F: Per pin	−2 to +4	mA	5
	$I_{OA}3$	Microcomputer I/F: Per pin	−2 to +10	mA	2
	$I_{OA}4$	P0 to P5: Per pin	−0.5 to +10	mA	3
	$\Sigma I_{OA}1$	Audio I/F: Total	−11 to +45	mA	4
	$\Sigma I_{OA}2$	Audio I/F, DRAM I/F: Total	−4 to +15	mA	5
	$\Sigma I_{OA}3$	Microcomputer I/F: Total	−4 to +15	mA	2
	$\Sigma I_{OA}4$	P0 to P5: Total	−3 to +30	mA	3
Allowable power dissipation	Pd max	Ta=–30 to +70˚C	600	mW	
Operating temperature	Topr		−30 to +70	˚C	
Storage temperature	Tstg		−40 to +125	˚C	

* When soldering QFP devices, do not use the solder dip method.

Allowable Operating Conditions at Ta = –30 to +70˚C, V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, unless otherwise noted

Parameter			Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit	Note
Operating supply voltage			V_{DD}		4.75		5.25	V	
Input high-level voltage			$V_{IH}1$	Audio I/F, DRAM I/F	2.4			V	6
			$V_{IH}2$	P0 to P5, SELC, TEST1 to 4	$0.7V_{DD}$			V	
			$V_{IH}3$	$\overline{RES}$, $\overline{INT}$, Microcomputer I/F	$0.75V_{DD}$			V	7
Input low-level voltage			$V_{IL}1$	Audio I/F, DRAM I/F			0.8	V	6
			$V_{IL}2$	P0 to P5, SELC, TEST1 to 4			$0.3V_{DD}$	V	
			$V_{IL}3$	$\overline{RES}$, $\overline{INT}$, Microcomputer I/F			$0.25V_{DD}$	V	7
Operating frequency (Instruction cycle time)			f_{OP} (TCYC)	Up to 1% crystal oscillation error is allowed. max: 48kHz × 384 × 1.01	12.17 (165)		18.62 (107)ns	MHz (ns)	
External clock input conditions	Frequency		f_{EXT}	Applies to the OSC1 pin. See figure 1. (OSC1: input, OSC2: open)	12.17		18.62	MHz	
	Pulse width		f_{EXTH} f_{EXTL}		20			ns	
	Rise time Fall time		f_{EXTR} f_{EXTF}				10	ns	
Self-oscillation conditions	Crystal oscillation	oscillation frequency	f_{EXT}	OSC1, OSC2, See figure 2.			18.62	MHz	
		oscillation stablizing period	t_{EXTS}	See figure 3.				ms	
Audio data input conditions	Transfer bit clock cycle		t_{BCYC}	Applies to the BCK1 and BCK2 pins. See figure 4.	325			ns	
	Transfer bit clock pulse width		t_{BCW}		100			ns	
	Data set up time		t_S		75			ns	
	Data hold time		t_H		75			ns	

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Parameter		Symbol	Conditions	Ratings			Unit	Note
				min	typ	max		
Serial I/O clock conditions	Serial clock cycle	t_{SCYC}	Applies to the microcomputer interface. See figure 5. (Applies to the SICK, SOCK and SI pins.)	650			ns	
	Serial clock pulse width	t_{SCW}		325			ns	
	Data set up time	t_{SS}		75			ns	
	Data hold time	t_{SH}		75			ns	
DRAM input conditions	Data set up time	t_{DS}	Applies to the data input from external DRAM. See figure 6. (Timings between $\overline{RAS}$, $\overline{CAS}$ and D0 to D7)	41			ns	8
	Data hold time	t_{DH}		0			ns	8

Electrical Characteristics at Ta = –30 to +70˚C, V_{DD} = 4.75V to 5.25 V, V_{SS} = 0V, unless otherwise noted

Parameter		Symbol	Conditions	Ratings			Unit	Note
				min	typ	max		
Input low-level current		$I_{IL}1$	$\overline{RES}$, $\overline{INT}$, $V_{IN}=V_{SS}$	–250			µA	
		$I_{IL}2$	P0 to P5, $V_{IN}=V_{SS}$	–1			mA	
Input high-level current		I_{IH}	$\overline{SELC}$, Input pin with pull-down resistor			250	µA	
Output high-level voltage		$V_{OH}1$	I_{OH}=–0.4mA	4.0			V	1
		$V_{OH}2$	I_{OH}=–50µA	V_{DD}–1.2			V	2, 3
Output low-level voltage		$V_{OL}1$	I_{OH}=2mA			0.4	V	1
		$V_{OL}2$	I_{OH}=10mA			1.5	V	2, 3
Input leakage current			$V_{IN}=V_{SS}$ to V_{DD}	–10		+10	µA	
Output-off leakage current		I_{OFF}	$V_O=V_{SS}$, V_{DD}	–40		+40	µA	
Input/output capacitance						10	pF	
Audio data output timing	Output data hold time	t_{OH}	Applies to audio data output. See figure 7.	20			ns	
	Output data delay	t_{OD}				100	ns	
Microcomputer I/F output delay	Output data delay	t_{SD}	Applies to serial data output. See figure 8.			100	ns	
Access timings for external DRAM	$\overline{RAS}$ H pulse width	t_{RP}	Data output timing for external DRAM. See figure 9. (Note) DRAM which has RAS access time below 120ns should be used.	95			ns	8
	$\overline{RAS}$ L pulse width	t_{RAS}		150			ns	8
	$\overline{CAS}$ H pulse width	t_{CP}		80			ns	8
	$\overline{CAS}$ L pulse width	t_{CAS}		101			ns	8
	$\overline{RAS}$ address set up time	t_{RS}		0			ns	8
	$\overline{RAS}$ address hold time	t_{RH}		20			ns	8
	$\overline{CAS}$ address set up time	t_{CS}		0			ns	8
	$\overline{CAS}$ address hold time	t_{CH}		40			ns	8
	$\overline{DWRT}$ pulse width	t_W		50			ns	8
	$\overline{CAS}$-before-WRITE set up time	t_{WC}		0			ns	8
	Data set up time	t_{SD}		0			ns	8
	Data hold time	t_{HD}		50			ns	8
Crystal oscillation		C1, C2	OSC1, OSC2, See figure 2.		20		pF	
Current drain		I_{DD}	V_{DD}1, 2, 18.62MHz external clock		50	100	mA	

(Note 1) TTL level output pins: ASO, AOBCK, AOWCK, LRCKO, BCK2, AOTDF1, AOTDF2, DFBCK, DFWCK, D0 to D7, A0 to A8, FS384O, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$ and FS64O/T5
(Note 2) CMOS medium current outputs: SO, $\overline{SOAK}$, and $\overline{SIAK}$
(Note 3) Pu MOS medium current outputs: P0 to P5
(Note 4) TTL level outputs (first group): ASO, AOBCK, AOWCK, LRCKO, A0 to A8, D0 to D7, FS384O and BCK2
(Note 5) TTL level outputs (second group): AOTDF1, AOTDF2, DFWCK, $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$, and DFBCK
(Note 6) L level Schmitt inputs pin: BCK1, BCK2, ASI1, ASI2, LRCKI, and D0 to D7
(Note 7) Schmitt input pins: $\overline{RES}$, $\overline{INT}$, SOCK, SI, SICK, $\overline{SORQ}$, $\overline{SIRQ}$, and $\overline{SRDY}$
(Note 8) The maximum load capacitance of $\overline{RAS}$, $\overline{CAS}$, $\overline{DREAD}$, $\overline{DWRT}$, D0 to D7 and A0 to A8 is 50pF.

DISCONTINUED PRODUCT

Figure 1. External input clock waveform (OSC1)

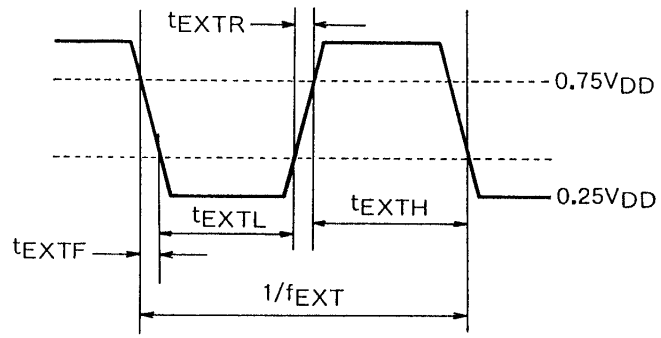

Figure 2. Crystal oscillation circuit

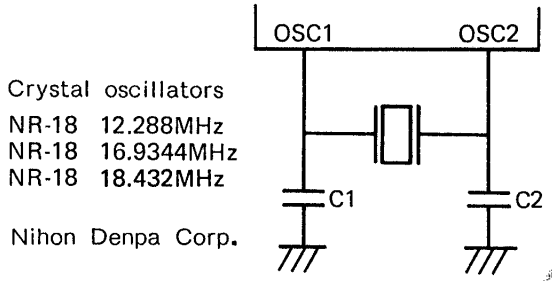

Figure 3. Oscillation stabilizing period

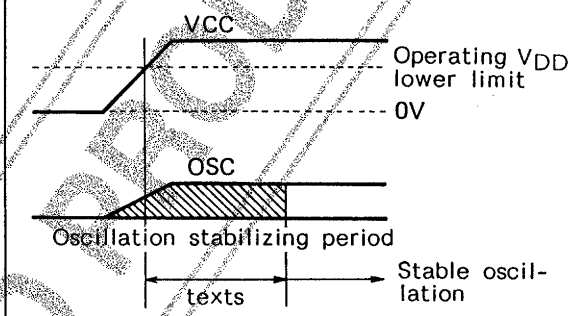

Figure 4. Audio data input conditions

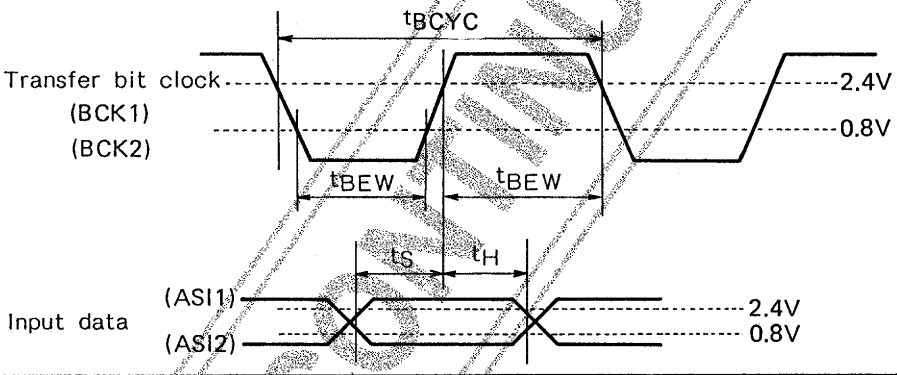

Figure 5. Microcomputer Interface

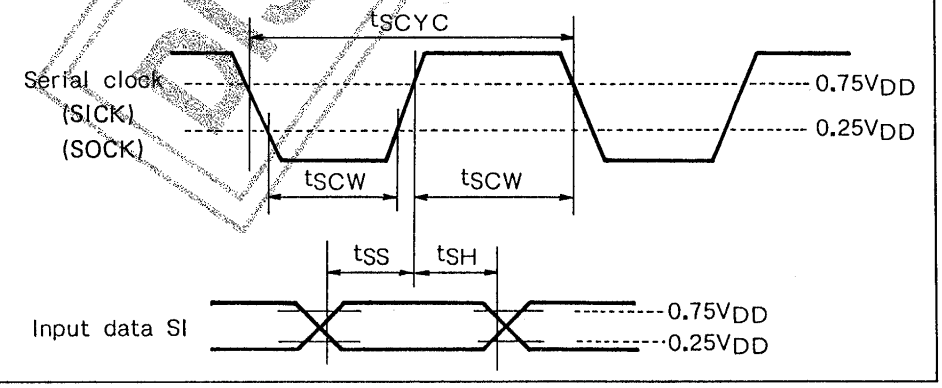

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Figure 6. External DRAM data input condition ($\overline{DREAD}$ = L)

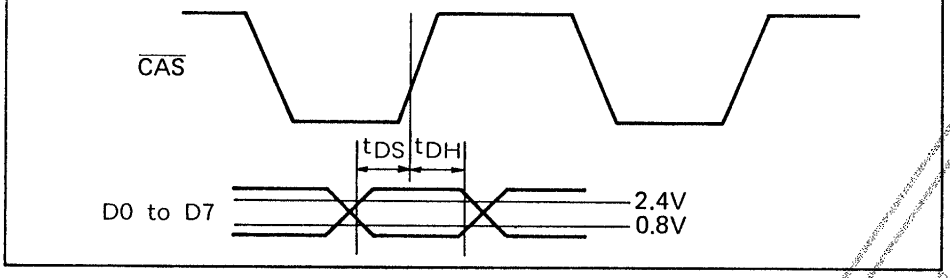


Figure 7. Audio data output timing

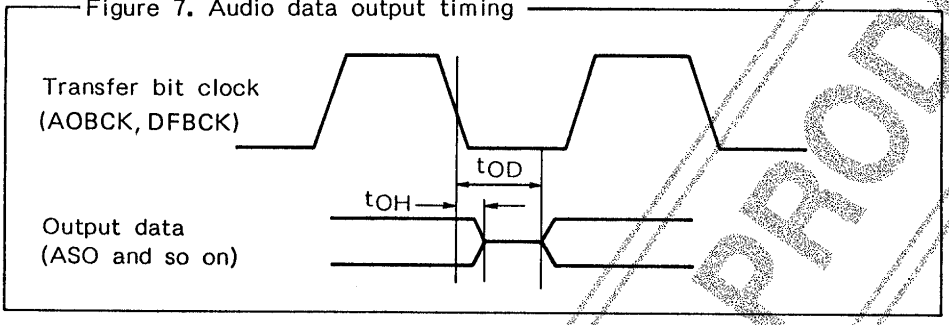


Figure 8. Microcomputer interface serial output timing

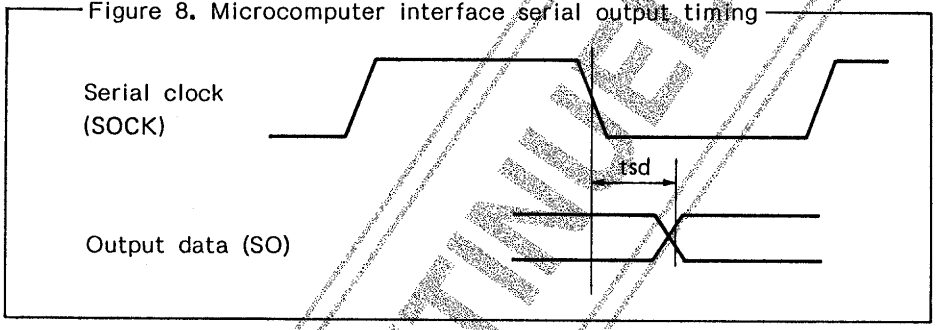
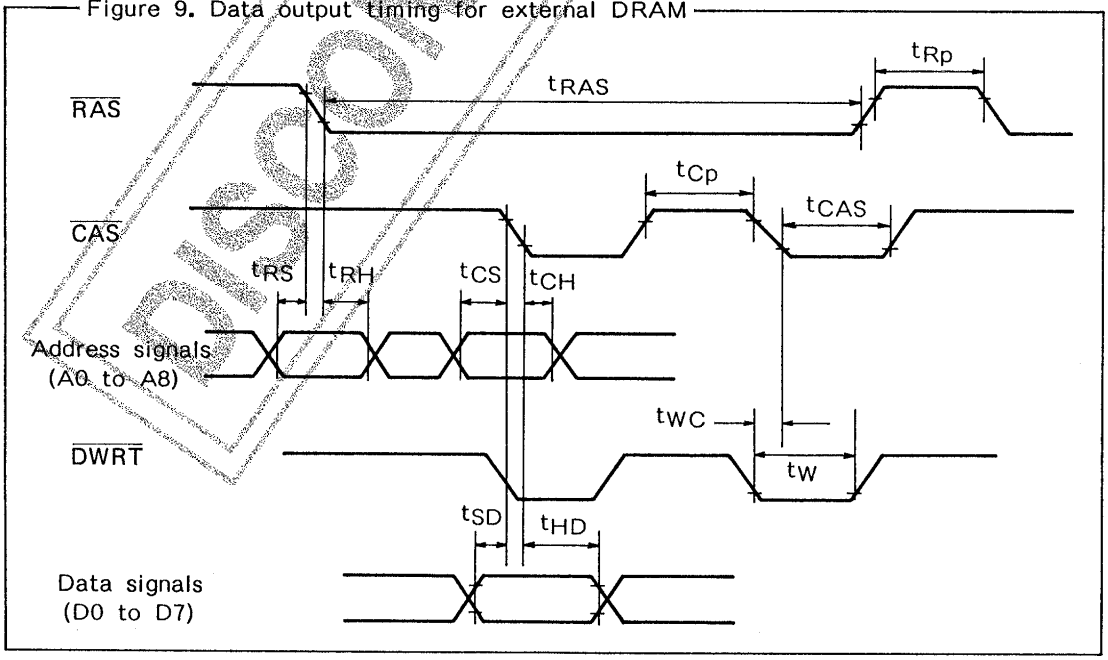


Figure 9. Data output timing for external DRAM



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Program Load to The LC83010N

- Boot procedure -

Programs must be loaded (boot strap) into the LC83010N (D²SP) from an external control unit (microcomputer) because its internal program memory consists of RAMs. The capacity of the program memory is 320 words × 32 bits.
The procedural flow to load a 320-word program into the D²SP from a controlling microcomputer is shown in Figure A-1.

(1) Reset the entire system (microcomputer and D²SP) or reset the D²SP from the controlling microcomputer. After the D²SP is reset, it then enters the Boot mode.
(2) Transfer the program to the D²SP from the microcomputer. The program is transferred to the D²SP in 8-bit synchronous serial communication mode.
The program data of 8 bits × 16 data (equal to 4 instructions) is transferred to the D²SP continuously from the microcomputer, and followed by the SRDY signal. The D²SP stores that program data of 4 instructions to the internal mail box. The program data is then moved to the program RAM at the moment when the SRDY signal reaches the D²SP.
(3) The operations discussed in (2) are repeated 80 times until the program data transfer of 320 instructions from the microcomputer to the D²SP is complete.
(4) The D²SP automatically starts the program execution when the program loading of 320 instructions is complete. The program is transferred to the D²SP from the microcomputer in that manner.

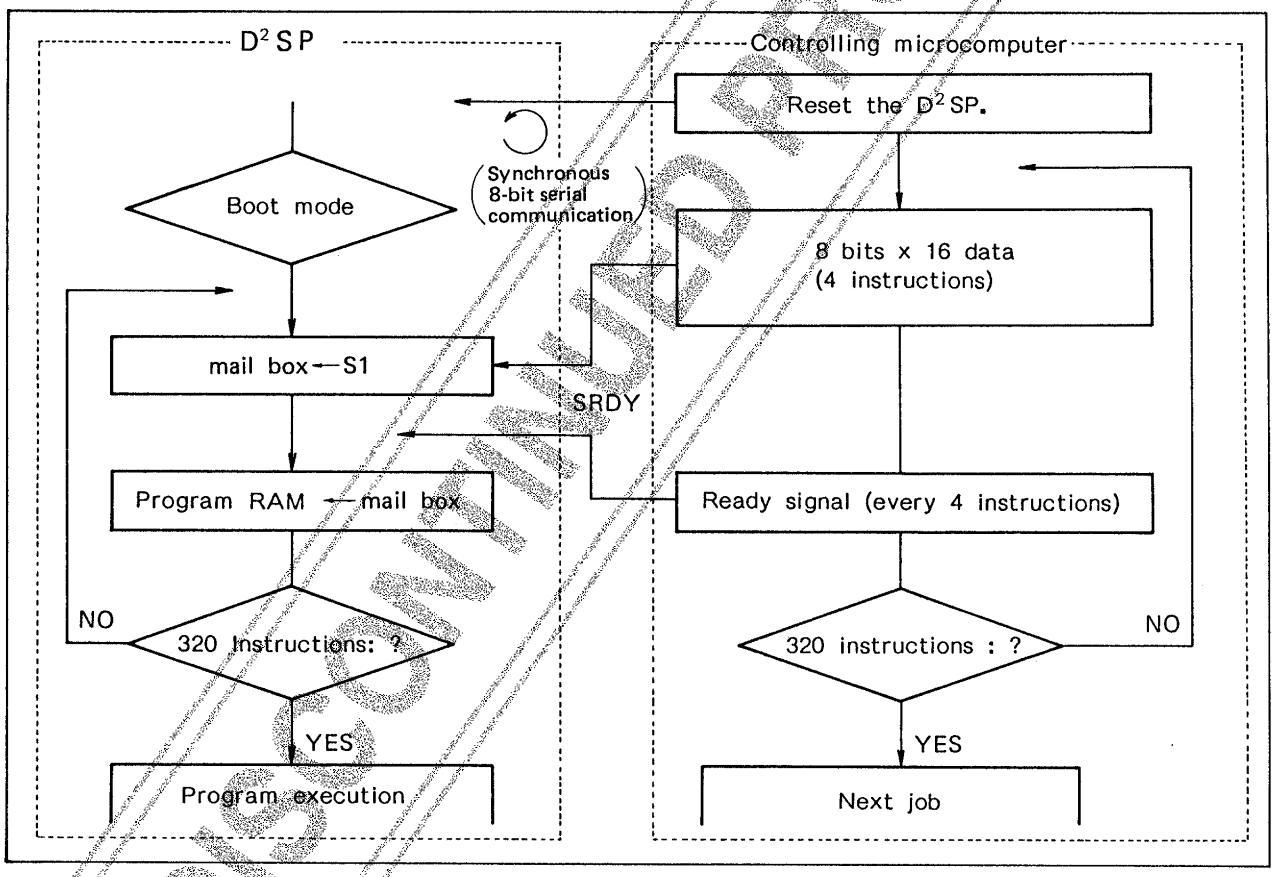

Figure A-1. Example Program Boot Flow (D²SP ← Microcomputer)

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Figure A-2 gives the outline of an example program Boot system.

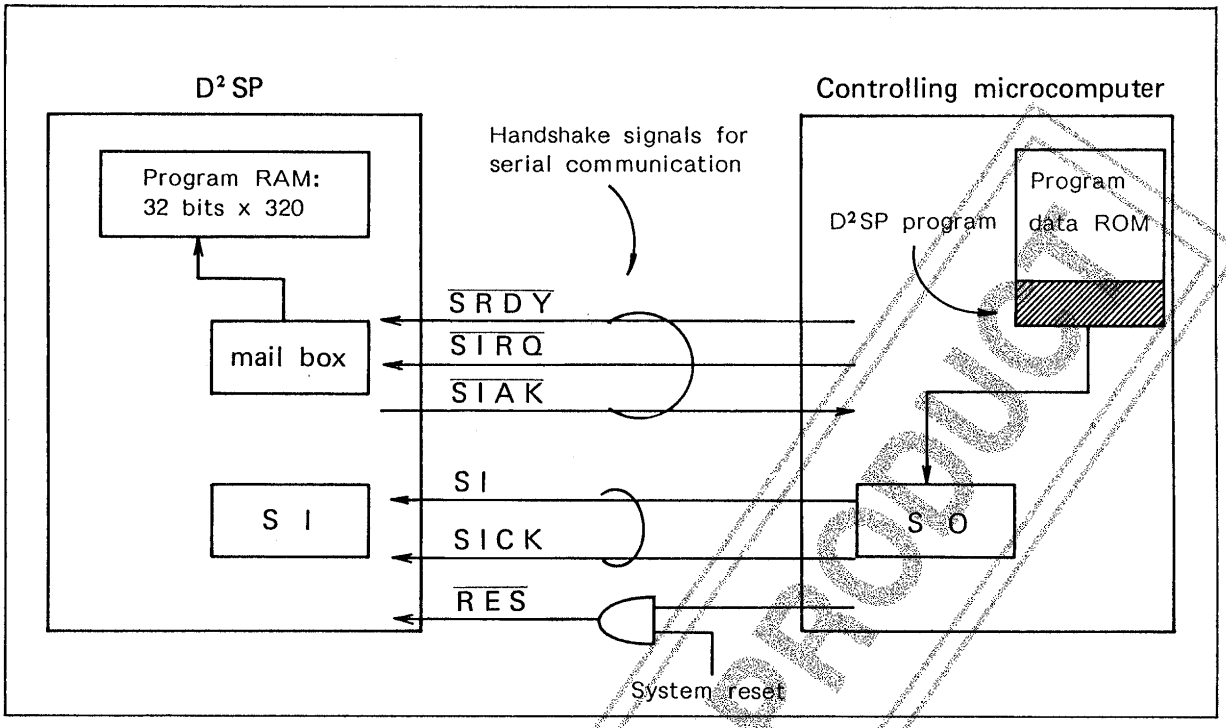

Figure A-2. Outline of an Example Program Boot System

Development Tool System

- Program development flow -

Development tools are provided to help the user to easily develop application programs for the D²SP. These development tools are divided into two groups: software support tool group and hardware support tool group. The software support tool group consists of an assembler, debugger and simulator.

The hardware support tool group is realized as an In-Circuit Emulator (ICE).

Figure A-3 shows the applications development flow for the D²SP system.

(1) Write an application source program.

(2) Check the source program for syntax errors with the assembler. If every syntax error is corrected, the assembler generates a HEX program file.

(3) Check the HEX file for operational errors with the simulator. If the desired operations are not successful, start the debugger to find what caused logical errors.

(4) If program operations are checked successfully, use the ICE to evaluate the audio signal output.
First, evaluate sound signals only with the ICE. In this evaluation process, the delay memory and microcomputer of the ICE are used.
Second, start the total evaluation on an application system. In this evaluation stage, the AD/DA converters, microcomputer, and delay memory on the user application system are used.
Figure A-4 shows the entire program development tool system for the D²SP.
The software tools such as the assembler, debugger, simulator can be run on an IBM PC-AT compatible machine or an AX personal computer. The ICE is also controlled by such a host personal computer.

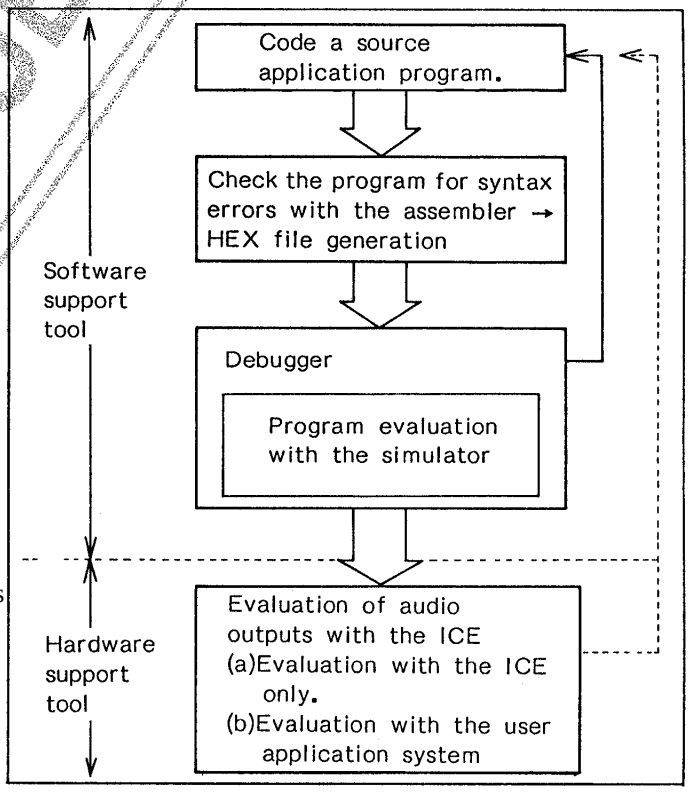

Figure A-3. Applications Development Flow

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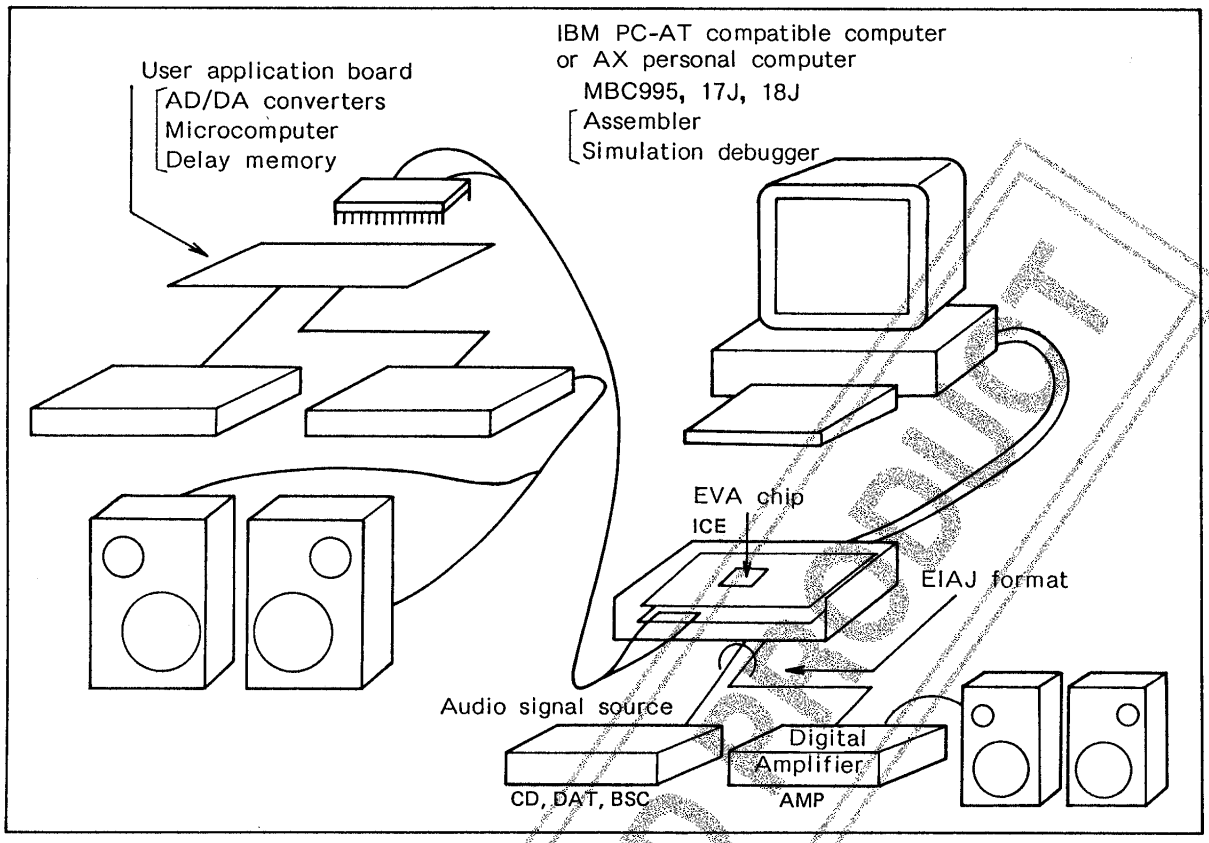

Figure A-4. Entire Support Tool System for Microprogram Development

(1) Debugger

The debugger is a software support tool designed to realize virtual D²SP functional circuits. In this virtually emulated D²SP environment, user application programs can be evaluated as if they were executed on the real chip. The debugger is used mainly for logics analysis and detailed data analysis.
Major functions of the debugger are listed in the table below, with brief explanation for each.

· Display and Edit instructions
These instructions can be used to display the contents of memory and registers on a screen and to update them.
· Memory Fill instruction
This instruction is used to fill a specified memory address range with a desired value.
· Move instruction
This instruction is used to transfer the data in a specified memory address range to another range.
· Memory Load and Save instructions
These instructions are used to transfer data between memory and disk. The memory load instruction enables the data transfer from a disk file to memory while the memory save instruction allows the data transfer from memory to a disk file.
· Assemble and Unassemble instructions
The assemble instruction is used to convert mnemonics into machine codes.
The unassemble instruction is used to convert memory data back to mnemonics.
· Emulation instruction control instruction and Break point instruction
These instructions are used to execute the D²SP program and trace its operations. The break point instruction is used to set a point where the program execution stops.

Table Major debugger functions

CONTINUED ON NEXT

(2) Outline of the simulator functions

The application programs can be tested in the following sequence:

· Inputting digital audio signals to the D²SP chip,
· Executing a program,
· Converting the audio output into analog signals, and
· Measuring the analog signals with an oscilloscope or frequency characteristics meter (or sweep meter).

The simulator enables the above operations on a personal computer.

Figure A-5 shows the signal waveform measurement.

This simulator has the following three measurement functions:

1) Audio output waveforms (sine waves) with respect to audio input waveforms (sine waves)
2) Frequency characteristics of audio output (AOUT)
3) Impulse response characteristics of audio output

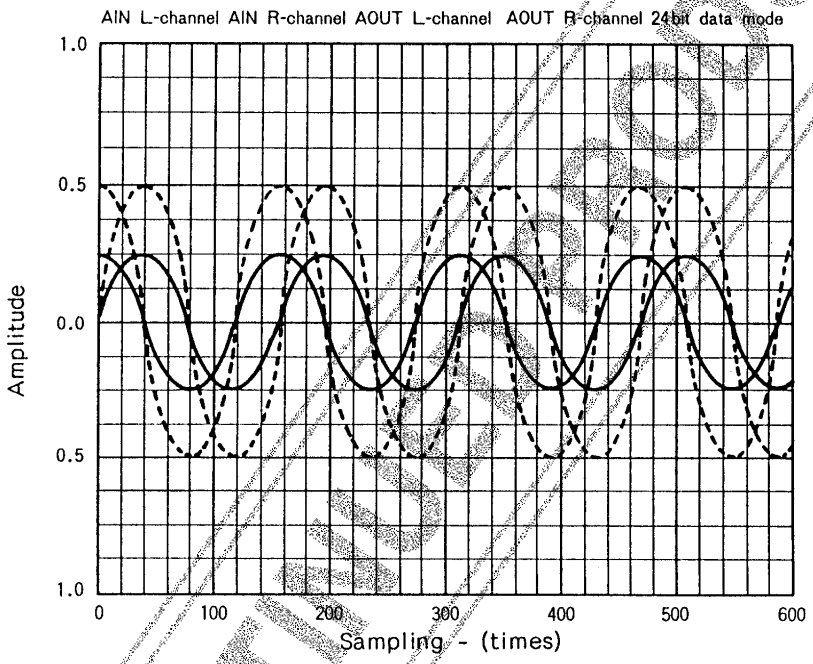

Figure A-5. Display of Various Waveforms

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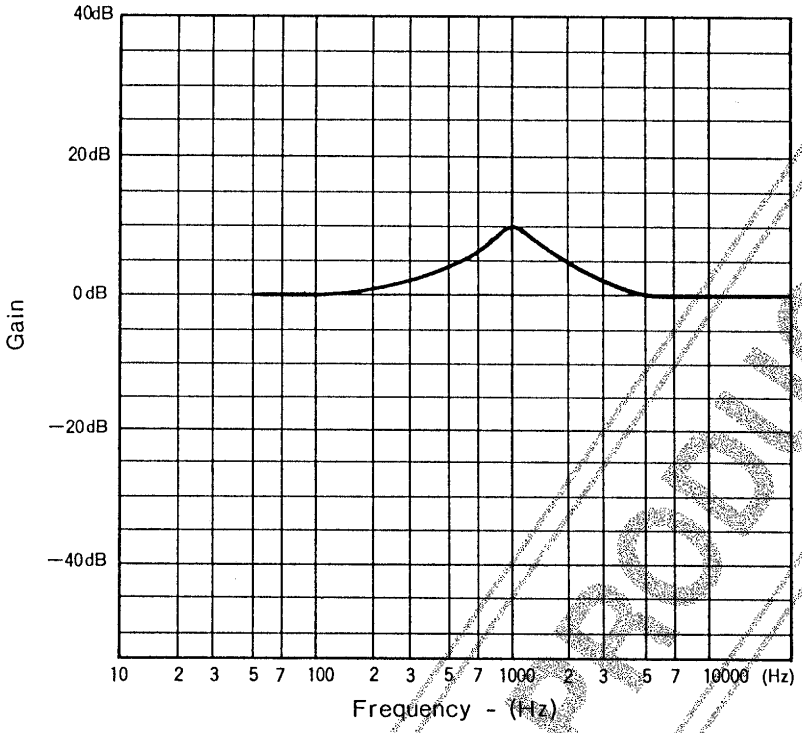

Figure A-6. Display of Frequency Characteristics

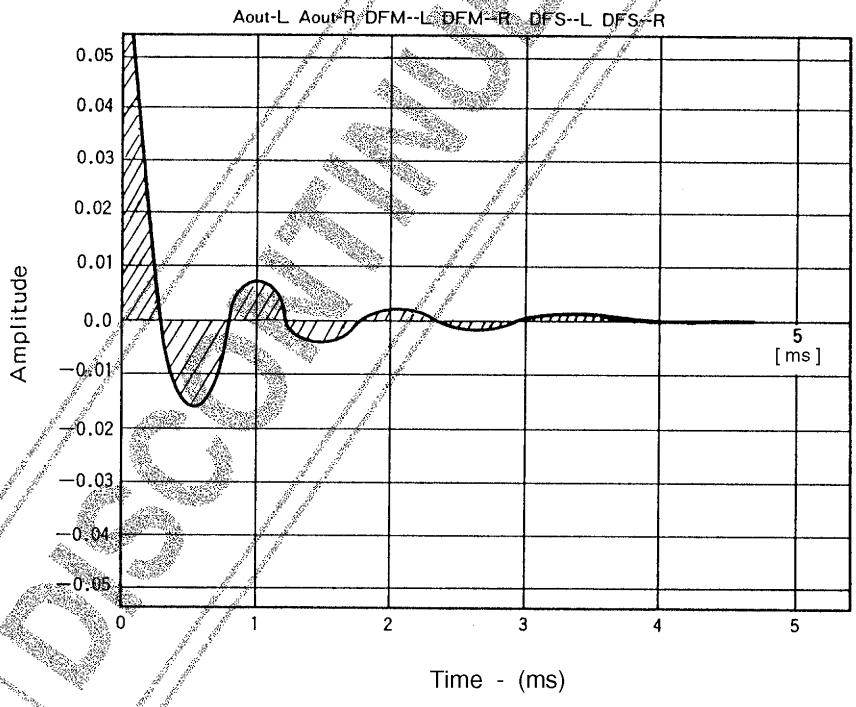

Figure A-7. Impulse Response Waveforms (Limit Cycle Characteristic)

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(3) ICE outline

The In-Circuit Emulator (ICE) provides an operating environment where the application program already checked by the simulation debugger is executed and then outputs audio signals. The ICE functions can be divided into two: One is the program evaluation by outputting audio signals only on the ICE. In this evaluation method, delay can be produced by the DRAM in the ICE system. The other is the final program evaluation by connecting a user application board to the ICE system. In this test method, the interfaces to the controlling microcomputer and other various peripheral ICs on the application board can be evaluated. Figure A-8 shows the ICE system configuration for the entire evaluation using a user application board.

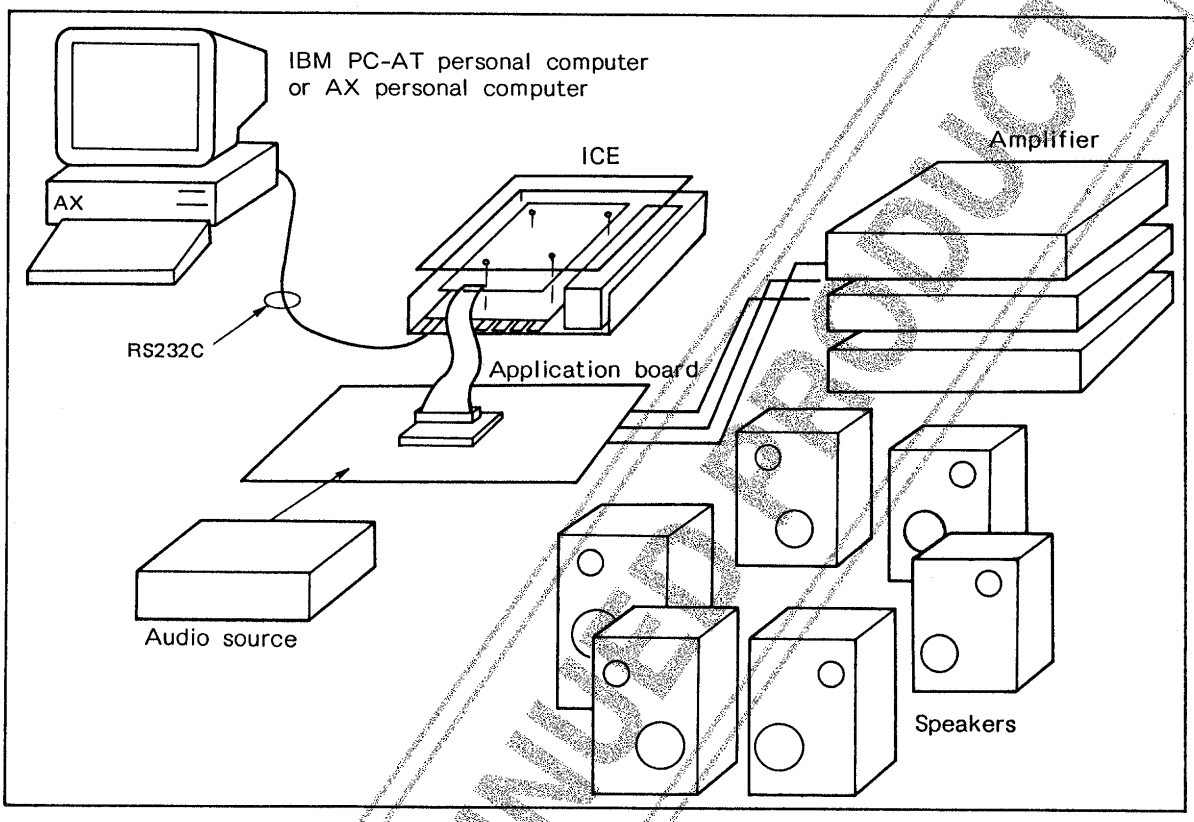

Figure A-8. Final Evaluation System Configuration with an Application Board and ICE

ICE functions

· The ICE has debugging functions.

· The ICE consists of unique hardware functions specifically designed as the ICE for audio DSP.

(a) ICE debugging functions

(1) Execution command : Allows the program execution to continue until a break point is detected. It also enables the program execution in the step mode or in the trace mode.

(2) Break function : Enables the user to set a desired break point.

(3) The edit dump command is useful in displaying the conditions of a specified memory area after the break of program execution. The register edit command is used to convert the contents of a present specified register.

(4) The memory dump command is useful in displaying the contents of a specified memory area when the program execution breaks. On the other hand, the edit command is used to edit the contents of a specified memory area when the program execution breaks.

(5) Program modification and confirmation : Enables the user to modify part of the program and to check how it works.

(6) Other functions : Memory management facility and so on. For details, refer the sections following section 8-3.

(b) Unique ICE hardware configuration

(1) Audio data input/output : Digital Interface Receiver (DIR).
This function allows direct input of audio digital data. Digital Interface Transmitter (DIT). This function allows direct output of 3-channel digital audio data.

(2) DRAM : Delay DRAM for audio signal. 256k (64k × 4 bits) × 2. 1M (256k × 4 bits) × 2

(3) Evaluation function of serial input/output : Z80 microcomputer for evaluating serial input/output. This control unit makes an access to the D^2SP instead of any controlling microcomputer to adjust the serial input/output operations.

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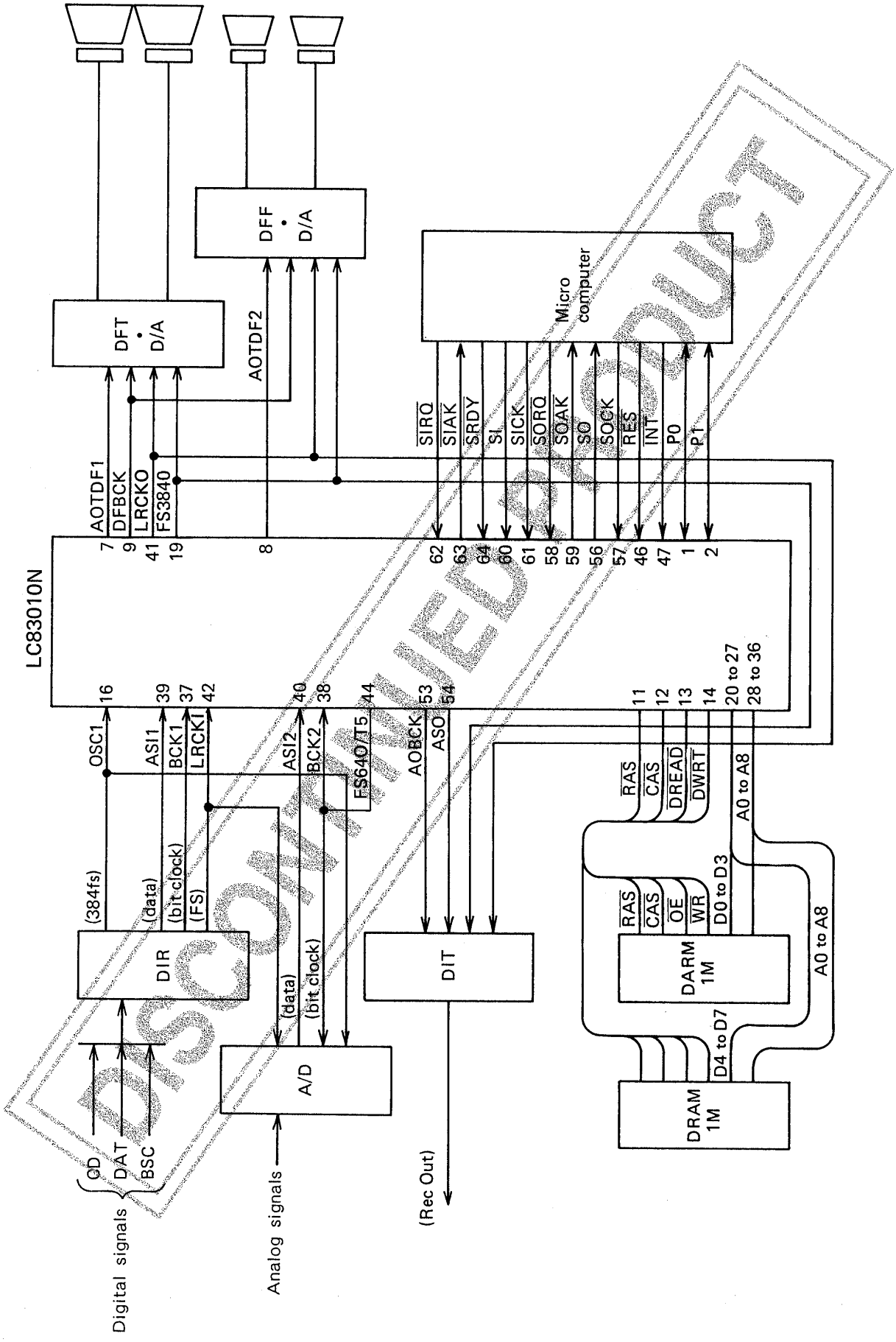
Example Application System



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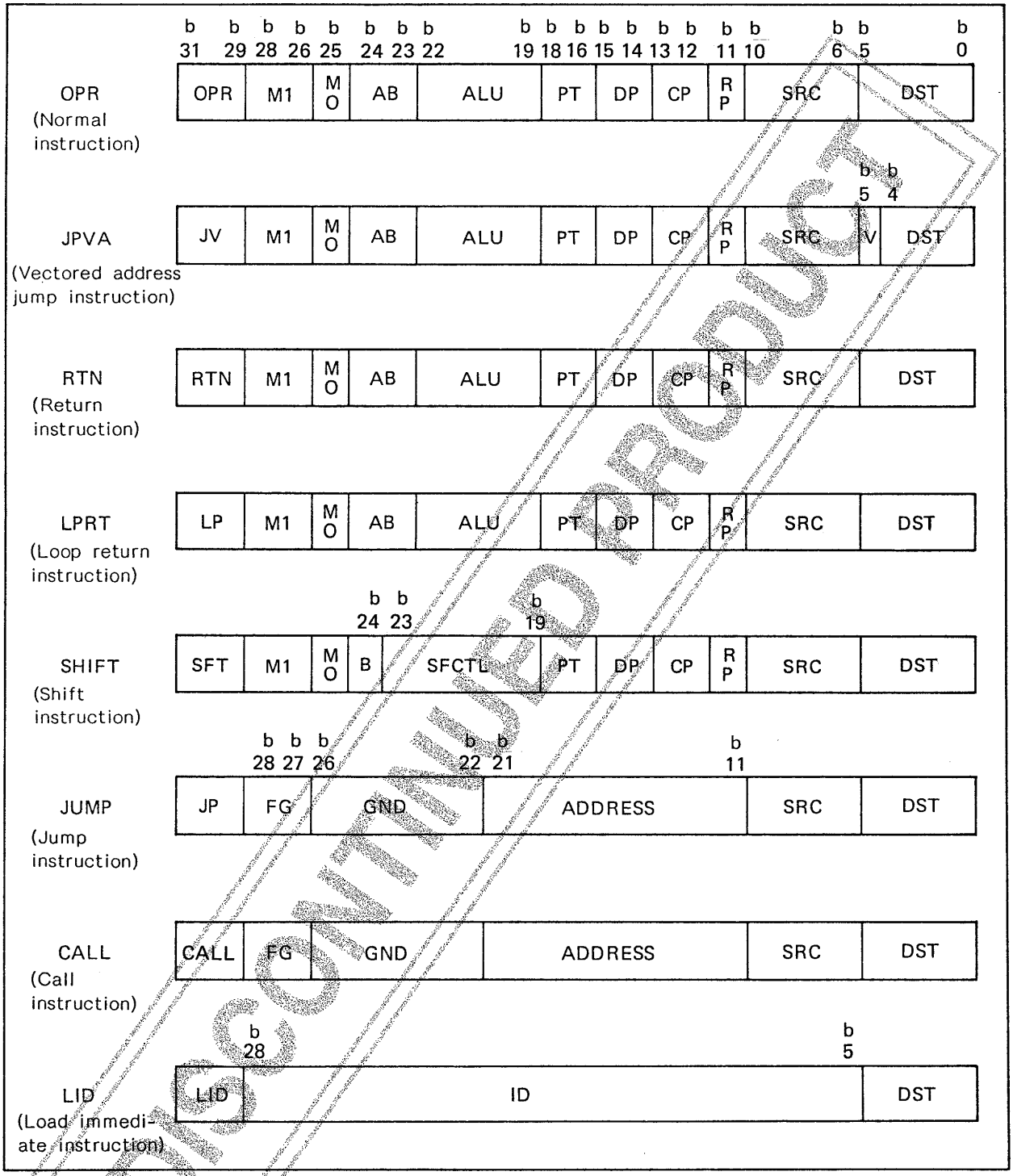
Instruction Bit Map

The instruction bit map is shown below.



Instruction Bit Map Diagram

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