Ordering number:ENN2721

CMOS IC

# LC82C55

## Programmable Peripheral Interface

## Overview

The LC82C55 Programmable Peripheral Interface IC is a pin-compatible CMOS version of the industry-standard 8255 device.

The 24 input/output pins may be programmed to operate in 3 different modes. Basic input/output, strobed input/output, and bi-directional input/output modes are available. All inputs and outputs are fully TTL compatible, and the device is easily interfaced to standard microprocessors.

The LC82C55 is fabricated using a Si-gate CMOS process for low operating and standby power consumption.

The LC82C55 operates on a single 5V power supply and is available in standard 40-pin plastic DIP packages.

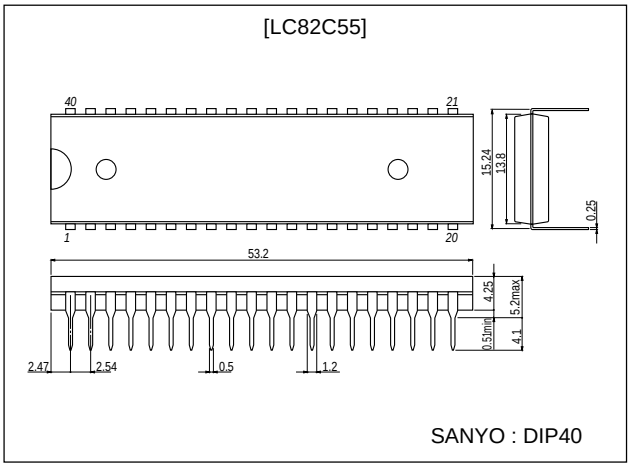
## Features

- 24 programmable input/output pins.
- Flexible input/output modes.
- Individual bit set/reset capability.
- Compatible with standard microprocessors.
- Zero wait-state operation with an 8MHz CPU. ($T_{RD}$ = 120ns)
- Fully TTL compatible $I_{OL}$ = 2.5mA.
- Low-power CMOS process.
- Single 5V power supply.

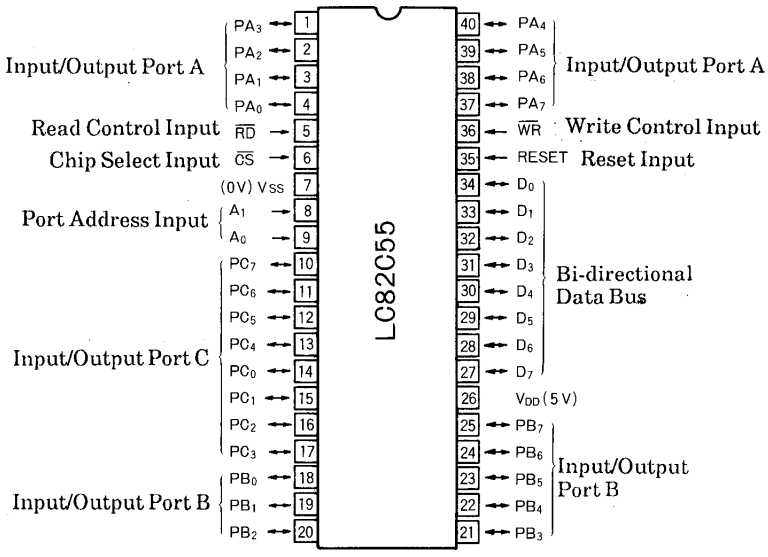
## Package Dimensions

unit:mm

3013A-DIP40




**Pin Assignment** (Top view)







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# Specifications

## Absolute Maximum Ratings at $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | | –0.3 to +7 | V |
| Input voltage | $V_{IN}$ | | –0.3 to $V_{DD}$ +0.3 | V |
| Allowable power dissipation | Pd max | | 1 | W |
| Operating temperature | Topr | | –20 to +75 | ˚C |
| Storage temperature | Tstg | | –65 to +150 | ˚C |

## DC Recommended Operating Conditions at Ta = –20 to +75˚C, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | 4.5 to 5.5 | V |
| Input low-level voltage | $V_{IL}$ | $V_{DD}$=5V±10% | –0.3 to +0.8 | V |
| Input high-level voltage | $V_{IH}$ | $V_{DD}$=5V±10% | 2.0 to $V_{DD}$+0.3 | V |

## Electrical Characteristics(1)

## DC Characteristics at Ta = –20 to +75˚C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Output low-level voltage | $V_{OL}$ | $I_{OL}$=2.5mA | | | 0.45 | V |
| Output high-level voltage | $V_{OH}$ | $I_{OH}$=–400µA | 2.4 | | | V |
| Input leakage current | $I_{IL}$ | $V_{IN}$=$V_{DD}$ to 0V | | | ±10 | µA |
| Output float leakage current | $I_{OFL}$ | $V_{OUT}$=$V_{DD}$ to 0V | | | ±10 | µA |
| Current drain 1 (Normal operation) | $I_{DD}1$ | | | | 10 | mA |
| Current drain 2 (Stand-by mode) | $I_{DD}2$ | | | | 10 | µA |
| Input capacitance | $C_{IN}$ | $f_c$ = 1MHz, unmeasured pins held at 0V. | | | 10 | pF |
| I/O pin capacitance | $C_{I/O}$ | | | | 20 | pF |

## Electrical Characteristics(2)

## AC Characteristics at Ta = –20 to +75˚C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

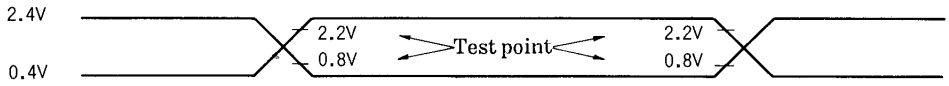
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| [Bus timing (read cycle)] | | | | | | |
| Address stable before $\overline{RD}$ ↓ | $t_{AR}$ | | 0 | | | ns |
| Address stable after $\overline{RD}$ ↑ | $t_{RA}$ | | 0 | | | ns |
| $\overline{RD}$ pulse width | $t_{RR}$ | | 160 | | | ns |
| Data valid before $\overline{RD}$ ↓ | $t_{RD}$ | $C_L$=150pF | | | 120 | ns |
| Data valid after $\overline{RD}$ ↑ | $t_{DF}$ | $C_L$=20pF, $R_L$=2kΩ | 10 | | 85 | ns |
| Time between successive Read/write cycles | $t_{RV}$ | | 200 | | | ns |
| [Bus timing (write cycle)] | | | | | | |
| Address stable before $\overline{WR}$ ↓ | $t_{AW}$ | | 0 | | | ns |
| Address stable after $\overline{WR}$ ↑ | $t_{WA}$ | | 0 | | | ns |
| $\overline{WR}$ pulse width | $t_{WW}$ | | 120 | | | ns |
| Data valid before $\overline{WR}$ ↑ | $t_{DW}$ | | 100 | | | ns |
| Data valid after $\overline{WR}$ ↑ | $t_{WD}$ | | 0 | | | ns |
| Time between successive Read/write cycles | $t_{RV}$ | | 200 | | | ns |
| [Other bus timings] | | | | | | |
| Output after $\overline{WR}$ ↑ | $t_{WB}$ | $C_L$=150pF | | | 350 | ns |
| Port data valid before $\overline{RD}$ ↓ | $t_{IR}$ | | 0 | | | ns |
| Port data valid after $\overline{RD}$ ↑ | $t_{HR}$ | | 0 | | | ns |
| $\overline{ACK}$ pulse width | $t_{AK}$ | | 300 | | | ns |
| $\overline{STB}$ pulse width | $t_{ST}$ | | 350 | | | ns |
| Port data valid before $\overline{STB}$ ↓ | $t_{PS}$ | | 0 | | | ns |
| Port data valid after $\overline{STB}$ ↑ | $t_{PH}$ | | 150 | | | ns |
| Output after $\overline{ACK}$ ↓ | $t_{AD}$ | $C_L$=150pF | | | 300 | ns |
| Port float after $\overline{ACK}$ ↑ | $t_{KD}$ | $C_L$=20pF, $R_L$=2kΩ | 20 | | 250 | ns |

Continued on next page.

Continued from preceding page.

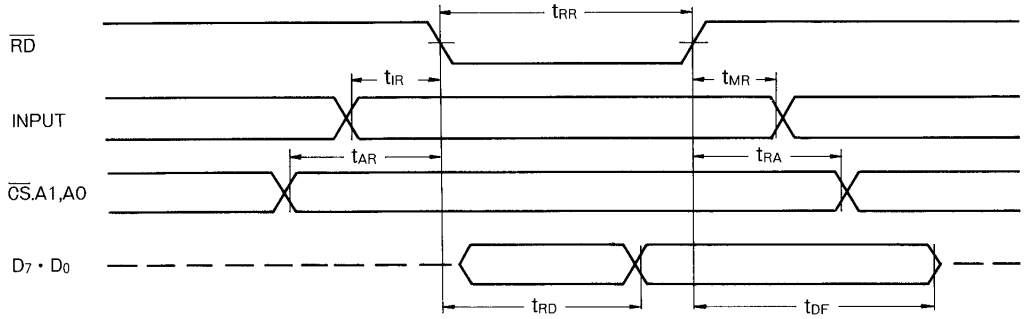
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| $\overline{OBF}$=0 after $\overline{WR}$ ↑ | $t_{WOB}$ | $C_L$=150pF | | | 300 | ns |
| $\overline{OBF}$=1 after $\overline{ACK}$ ↓ | $t_{AOB}$ | $C_L$=150pF | | | 350 | ns |
| IBF=1 after $\overline{STB}$ ↓ | $t_{SIB}$ | $C_L$=150pF | | | 300 | ns |
| IBF=0 after $\overline{RD}$ ↑ | $t_{RIB}$ | $C_L$=150pF | | | 300 | ns |
| INTR=0 after $\overline{RD}$ ↓ | $t_{RIT}$ | $C_L$=150pF | | | 400 | ns |
| INTR=1 after $\overline{STB}$ ↑ | $t_{SIT}$ | $C_L$=150pF | | | 300 | ns |
| INTR=1 after $\overline{ACK}$ ↑ | $t_{AIT}$ | $C_L$=150pF | | | 350 | ns |
| INTR=0 after $\overline{WR}$ ↓ | $t_{WIT}$ | $C_L$=150pF | | | 450 | ns |

## AC Test Input Waveform

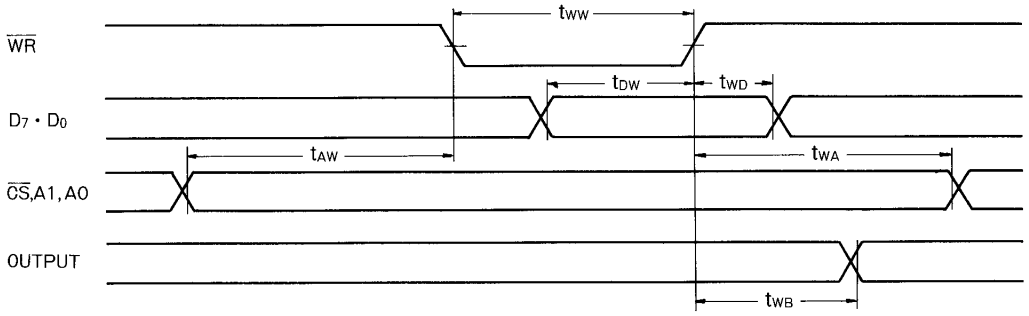



## Input/Output Waveforms

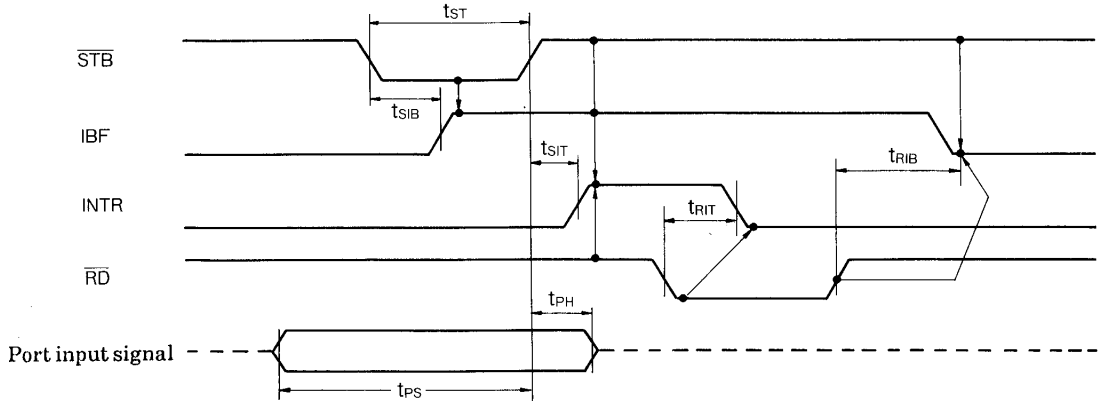
### Mode 0 (Basic Input Mode)



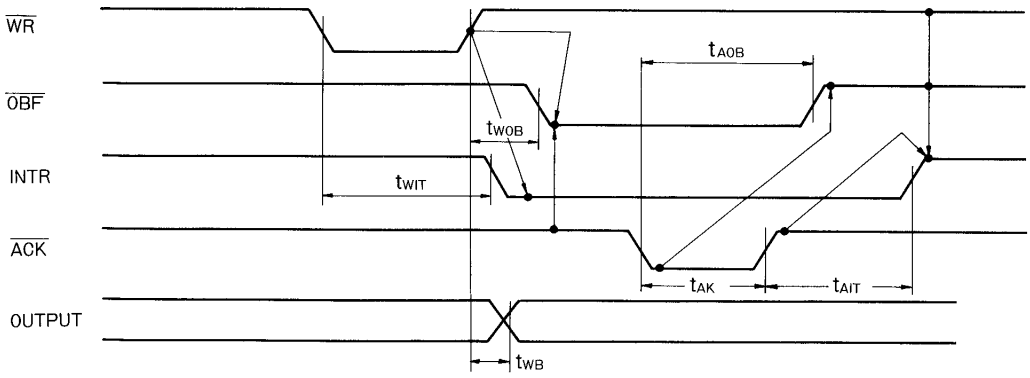

### Mode 0 (Basic Output Mode)



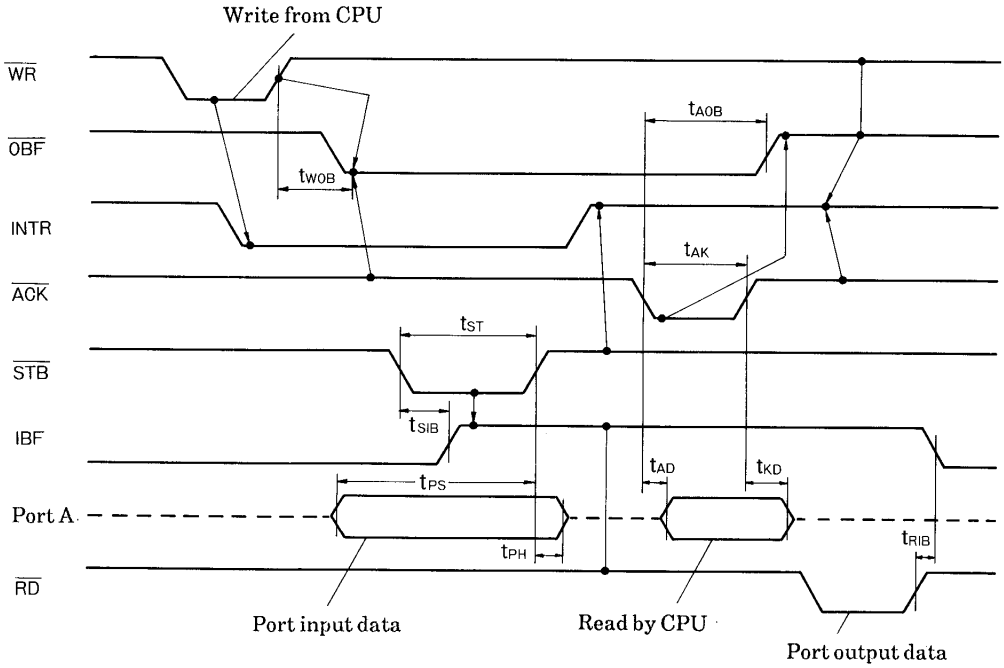

### Mode 1 (Strobed Input Mode)



### Mode 1 (Strobed Output Mode)



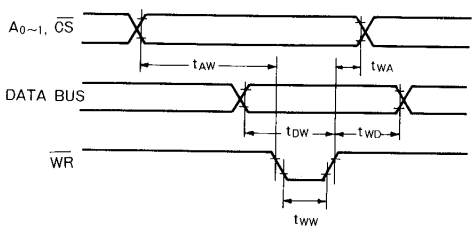

### Mode 2 (Bi-directional Bus Mode)



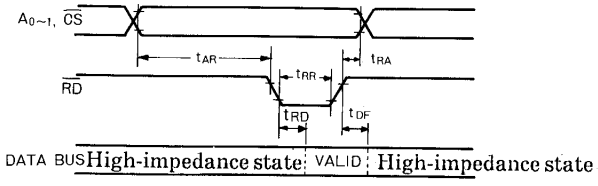

### Note

INTR = IBF · $\overline{\text{MASK}}$ · $\overline{\text{STB}}$ · $\overline{\text{RD}}$ + $\overline{\text{OBF}}$ · $\overline{\text{MASK}}$ · $\overline{\text{ACK}}$ · $\overline{\text{WR}}$

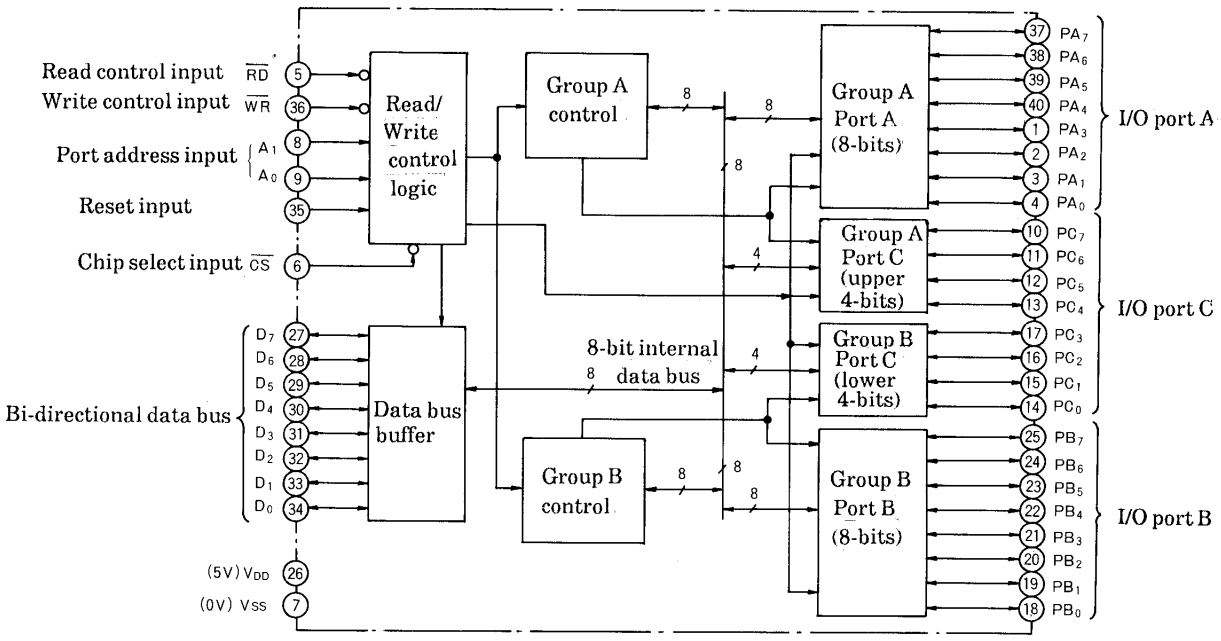
Write-cycle Timing




Read-cycle Timing



## Block Diagram




## Description of Operation

$\overline{RD}$ (read control input)

When Low, data or status word is transferred from the LC82C55 to the CPU via the data bus.

$\overline{WR}$ (write control input)

When Low, a data or control word is written from the CPU to the LC82C55.

$A_0$, $A_1$ (port address inputs)

Used to select Ports A, B and C, and the control register. Normally, the least significant 2 bits of the address bus are connected to these pins.

RESET input

A High level on this input clears the control register. All ports are set to the input mode (high-impedance state).

$\overline{CS}$ (chip select input)

A Low level on this input enables communication between the LC82C55 and CPU. When High, the data bus remains in the high-impedance state and control signals from the CPU are ignored.

Read/write control logic

This block performs the transfer of data and control words between the CPU and the internal circuitry. It receives data via the CPU interface signals and data bus, and issues commands to the port control logic.

Data bus buffer

This 8-bit, tri-state, bi-directional bus buffer interfaces the external 8-bit data bus to the LC82C55. Data control, and status information is transferred under the control of the CPU.

Group A/Group B control

Ports A, B and C are divided into the control Groups A and B, each with its own control circuitry. Group A consists of Port A and the upper 4 bits of Port C; Group B consists of port B and the lower 4-bits of Port C.

The control register is write-only.

Ports A, B and C

The operating mode of each 8-bit port is set by the CPU system software. Port A has an output latch/buffer and an input latch.

Port B has an input/output latch/buffer and an input buffer.

Port C has an output latch buffer and input buffer, and can be divided into two 4-bit ports using mode control. Each 4-bit port can be used as status and control signals for Ports A and B.

Table 1 Basic Operation

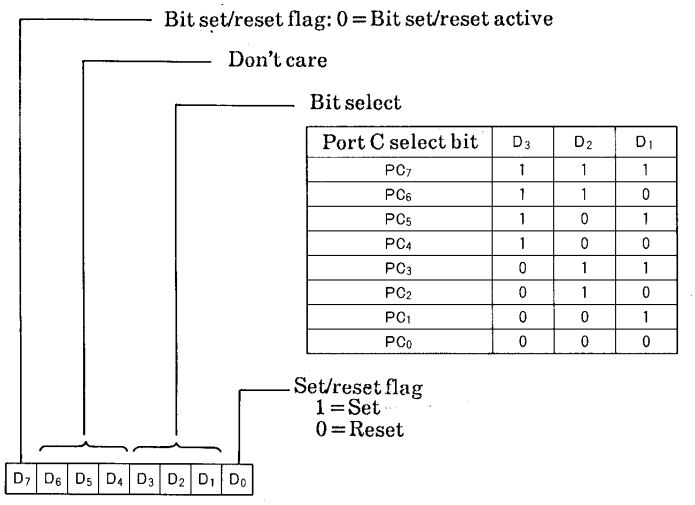
| $A_1$ | $A_0$ | $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | Function |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | Data bus ←Port A |
| 0 | 1 | 0 | 0 | 1 | Data bus ←Port B |
| 1 | 0 | 0 | 0 | 1 | Data bus ←Port C |
| 0 | 0 | 0 | 1 | 0 | Port A ← Data bus |
| 0 | 1 | 0 | 1 | 0 | Port B ← Data bus |
| 1 | 0 | 0 | 1 | 0 | Port C ← Data bus |
| 1 | 1 | 0 | 1 | 0 | Control register ← Data bus |
| × | × | 1 | × | × | Data bus is high-impedance state |
| 1 | 1 | 0 | 0 | 1 | Illegal operation |

0 : Low-level
1 : High-level

Bit Set/Reset

When Port C is used as an output port, any individual bit can be set or reset with a single control word from the CPU. This feature simplifies CPU control software in certain applications.

The bit/reset feature of Port C is also used to enable or disable the interrupt request signals from Ports A and B, when these ports are operating in Modes 1 or 2.




| Port C select bit | $D_3$ | $D_2$ | $D_1$ |
|---|---|---|---|
| $PC_7$ | 1 | 1 | 1 |
| $PC_6$ | 1 | 1 | 0 |
| $PC_5$ | 1 | 0 | 1 |
| $PC_4$ | 1 | 0 | 0 |
| $PC_3$ | 0 | 1 | 1 |
| $PC_2$ | 0 | 1 | 0 |
| $PC_1$ | 0 | 0 | 1 |
| $PC_0$ | 0 | 0 | 0 |

Figure 1. Port C Bit/Reset Control Word

Basic Operating Modes

The LC82C55 has three basic operating modes, selectable by control words from the CPU.

(1) Mode 0 : Basic input/output
(2) Mode 1 : Strobed input/output
(3) Mode 2 : Bi-directional bus

The operating modes for Groups A and B can be selected independently, however, Mode 2 operation can be selected for Group A only.

Figure 2 shows the format of the mode selection control word.

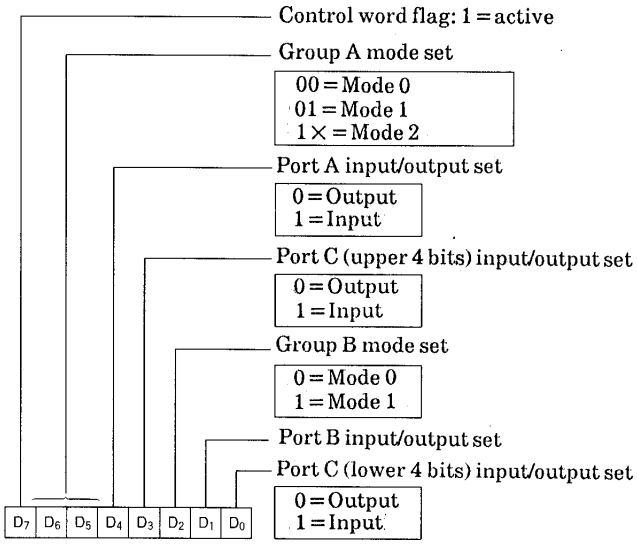



Figure 2. Mode Set Control Word

1. Mode 0 (basic input/output mode)

   Mode 0 is used for simple input/output operations for Ports A, B and C (Port C is used as two, 4-bit ports). There are no control signals such as interrupt requests or handshaking.

   Output data to a port is latched. Input data is not latched.

   Each of the two, 8-bit ports and two, 4-bit ports can be used for either input or output.

   The I/O configurations for Mode 0 are shown in Figure 3.

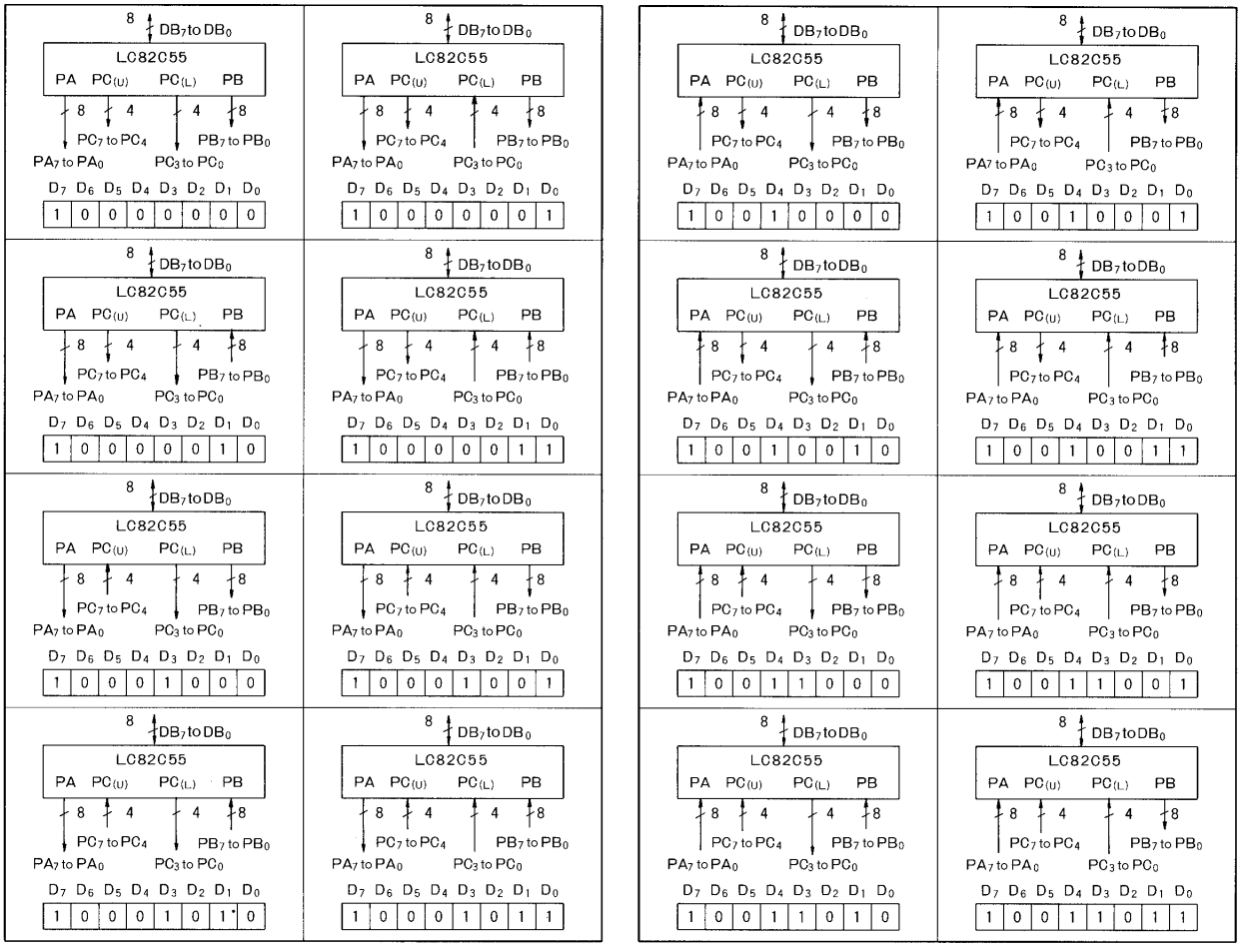



Figure 3. Mode 0 Port I/O Configurations

2. Mode 1 (strobed input/output mode)

Mode 1 can be selected independently for Groups A and B. Each group consists of an 8-bit data port and a 4-bit control/data port.

Data is transferred to or from a Mode 1 port with strobes or handshaking signals. Ports A and B provide each group's I/O signals, and Port C provides these control signals. Both input and output data are latched.

Input Mode Control Signals

$\overline{STB}$ (strobe input)

When Low, the data present on the port input pins is loaded into the input latch, $\overline{STB}$ enables the data from a peripheral device to be latched into the LC82C55 without CPU intervention.

IBF (input buffer full flag)

A High level on this output indicates that input data has been latched into the LC82C55. This flag is set on the falling edge of $\overline{STB}$ and is reset on the rising edge of $\overline{RD}$.

INTR (interrupt request output)

This active-high output can be used to interrupt the CPU when input data is strobed into the port. If the interrupt enable flag, INTE is High, INTR is set on the rising edge of the $\overline{STB}$ input. INTR is reset on the falling edge of the $\overline{RD}$ input.

$INTE_A$ and $INTE_B$ are set and reset using the bit set/reset capability of Port C. $INTE_A$ and $INTE_B$ correspond to Bits 4 and 2, respectively (PC4 and PC2) for Mode 1 input.

Examples of Mode 1 input are shown in Figure 4. The timing waveforms are shown in Figure 5.

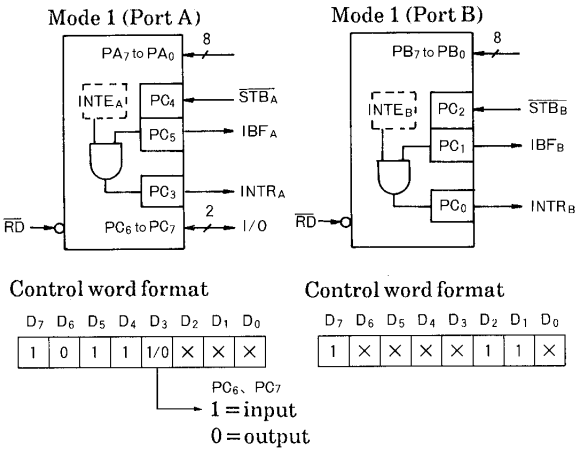



Figure 4. Mode 1 Input Configuration

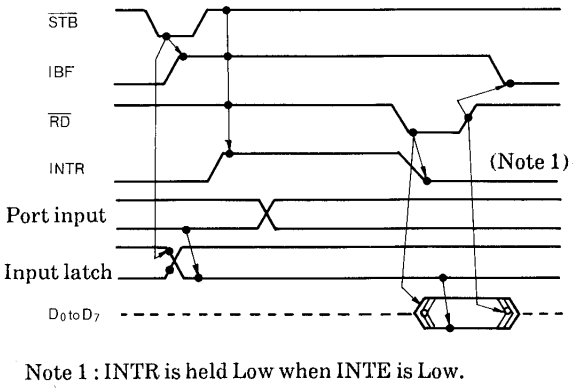



Figure 5. Mode 1 Input Timing

Output Mode Control Signals

$\overline{OBF}$ (output buffer full flag)

This active-low output indicates to a peripheral device that data is available in the port's output buffer. It is set to Low by the rising edge of the $\overline{WR}$ input, and is reset to High by the falling edge of the $\overline{ACK}$ input.

$\overline{ACK}$ (acknowledge input)

This active-low input indicates that the peripheral device has accepted data present on the port output.

INTR (interrupt request output)

This active-high output can be used to interrupt the processor when a peripheral devices accepts data from the LC82C55.

INTR is set if INTE is High (active), and both $\overline{OBF}$ and $\overline{ACK}$ are High (inactive). It is reset on the falling edge of $\overline{WR}$.

$INTE_A$ and $INTE_B$ are set and reset using the bit set/reset capability of Port C. $INTE_A$ and $INTE_B$ correspond to Bits 4 and 2, respectively (PC6 and PC2) for Mode 1 output.

Examples of the use of Port A and Port B for input/output in Mode 1 are shown in Figures 8 and 9.

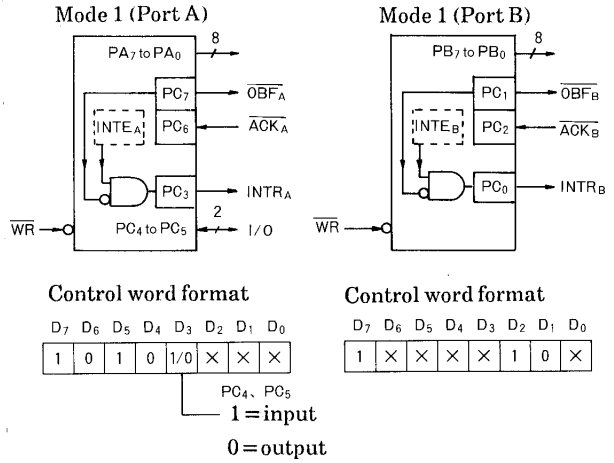
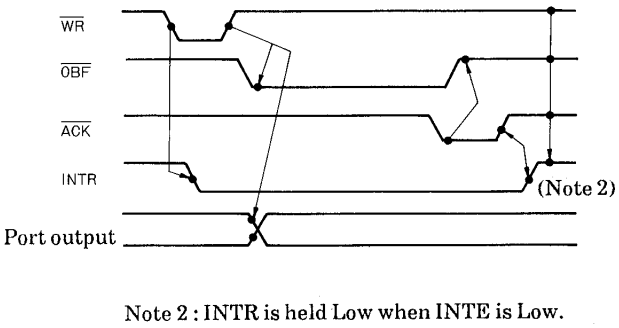



Figure 6. Mode 1 Output Configuration




Note 2 : INTR is held Low when INTE is Low.

Figure 7. Mode 1 Output Timing

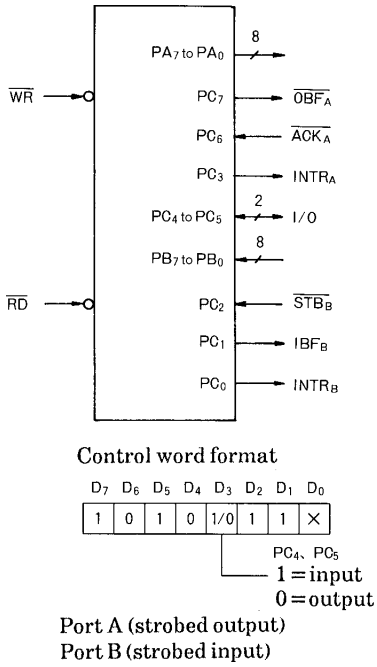



Figure 8. Mode 1 Input/Output Example

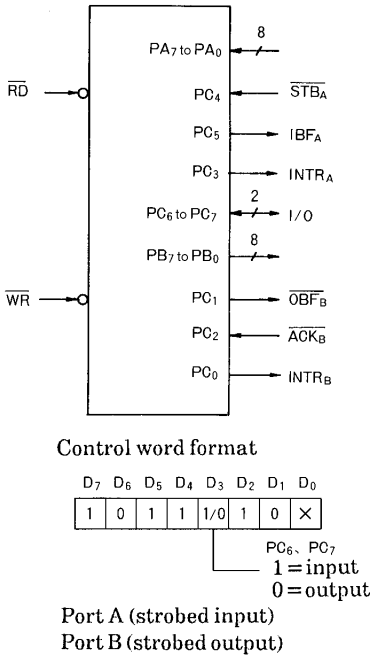



Figure 9. Mode 1 Input/Output Example

3. Mode 2 (strobed bi-directional bus)

Mode 2 provides a single 8-bit bi-directional bus. Handshaking and interrupt signals are available to control the flow of data between the peripheral device and the LC82C55.

This mode can only be used for Group A. It uses an 8-bit bi-directional data port (Port A) and a 5-bit control port (upper 5 bits of Port C). Inputs and outputs are both latched. The selection of Group B's operating mode is independent of Group A's operating mode.

Mode 2 Control Signals

$\overline{OBF}$ (output buffer full flag)

This active-low output signal indicates that the CPU has written data to the Port A output buffer.

$\overline{ACK}$ (acknowledge input)

The tri-state outputs are enabled while the $\overline{ACK}$ input is Low. When $\overline{ACK}$ is High, the output drivers are in the high-impedance state.

$\overline{STB}$ (strobe input)

When Low, the data present on the Port A pins are loaded into the input latch.

IBF (input buffer full flag)

This active-high output indicates that data has been latched into the Port A input latch.

INTR (interrupt request output)

This active-high output signal can be used to interrupt the CPU on both input and output operations. Operation is the same as in Mode 1.

There are two interrupt request control flags : INTE1 and INTE2.

INTE 1 is combined with $\overline{OBF}$ and $\overline{ACK_A}$, to generate an interrupt request on output data transfers. It is controlled by bit set/reset of DC6.

INTE 2 is combined with $\overline{IBF}$ and $\overline{STB_A}$, to generate an interrupt request on input data transfers. It is controlled by bit set/reset of DC4.

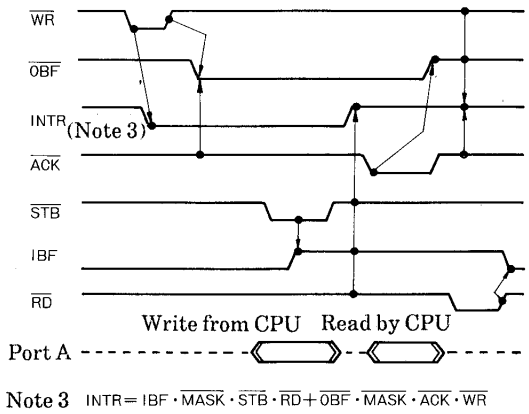



Figure 10. Mode 2 Timing Waveforms

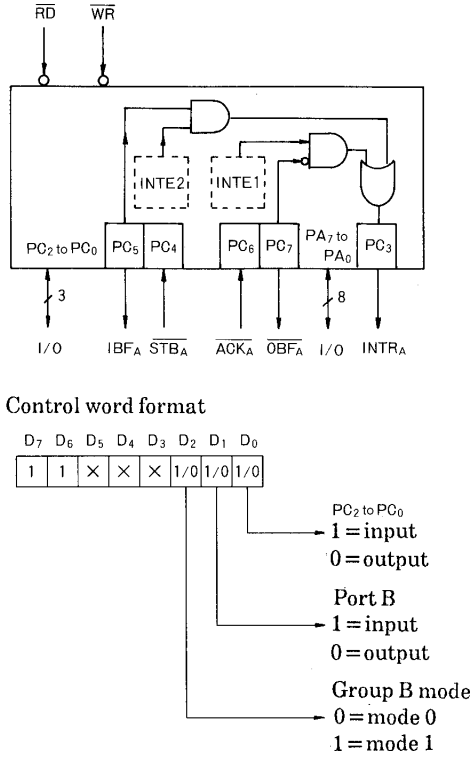



Figure 11. Mode 2 Input/Output Configuration

4. Reading Control Signals

When any of the Port C pins are used as control signals, the CPU can read these signals from Port C. These signals appear on the data bus as shown in Table 2. Note that the INTE flags are present in place of the $\overline{STB}$ and $\overline{ACK}$ signals. Port C pins not used for control or status are used as normal input or output pins, in accordance with the Port C input/output mode. Only those pins defined as Mode 0 outputs are affected by a write to Port C. Note that the INTE flags can only be changed using the appropriate bit set/reset commands.

Table 2. Port Control Signals

| Mode \ Data | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|
| Mode 1 input | I/O | I/O | $IBF_A$ | $INTE_A$ | $INTR_A$ | $INTE_B$ | $IBF_B$ | $INTR_B$ |
| Mode 1 output | $\overline{OBF_A}$ | $INTE_A$ | I/O | I/O | $INTR_A$ | $INTE_B$ | $\overline{OBF_B}$ | $INTR_B$ |
| Mode 2 | $\overline{OBF_A}$ | INTE1 | $IBF_A$ | INTE2 | $INTR_A$ | $INTE_B$ | See Note | $INTR_B$ |

**Note**

$IBF_B$ for 1 input, $OBF_B$ for Mode 1 output.

5. Control Word Tables

Table 3, 4 and 5 summarize the mode definition control words for Modes 0, 1 and 2. Note that the operating modes for both control groups can be set independently, however, these options have not been included in Tables 3 and 4. Table 6 summarizes the bit set/reset control words.

Table 3. Mode 0 Control Words

| Control Word | | | | | | | | | Group A | | Group B | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | Hexa-decimal | Port A | Port C (Upper 4 bits) | Port C (Lower 4 bits) | Port B |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | OUT | OUT | OUT | OUT |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | OUT | OUT | IN | OUT |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 | OUT | OUT | OUT | IN |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 | OUT | OUT | IN | IN |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 88 | OUT | IN | OUT | OUT |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 | OUT | IN | IN | OUT |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A | OUT | IN | OUT | IN |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8B | OUT | IN | IN | IN |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90 | IN | OUT | OUT | OUT |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91 | IN | OUT | IN | OUT |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 92 | IN | OUT | OUT | IN |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93 | IN | OUT | IN | IN |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98 | IN | IN | OUT | OUT |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 99 | IN | IN | IN | OUT |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 9A | IN | IN | OUT | IN |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9B | IN | IN | IN | IN |

Table 4. Mode 1 Control Words

| Control Word | | | | | | | | | Group A | | | | | Group B | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | Hexa-decimal | Port A | Port C | | | | | Port C | | | Port B |
| | | | | | | | | | | $PC_7$ | $PC_6$ | $PC_5$ | $PC_4$ | $PC_3$ | $PC_2$ | $PC_1$ | $PC_0$ | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | × | A4<br>A5 | OUT | $\overline{OBF_A}$ | $\overline{ACK_A}$ | OUT | | $INTR_A$ | $\overline{ACK_B}$ | $\overline{OBF_B}$ | $INTR_B$ | OUT |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | × | A5<br>A7 | OUT | $\overline{OBF_A}$ | $\overline{ACK_A}$ | OUT | | $INTR_A$ | $\overline{STB_B}$ | $IBF_B$ | $INTR_B$ | IN |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | × | AC<br>AD | OUT | $\overline{OBF_A}$ | $\overline{ACK_A}$ | IN | | $INTR_A$ | $\overline{ACK_B}$ | $\overline{OBF_B}$ | $INTR_B$ | OUT |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | × | AE<br>AF | OUT | $\overline{OBF_A}$ | $\overline{ACK_A}$ | IN | | $INTR_A$ | $\overline{STB_B}$ | $IBF_B$ | $INTR_B$ | IN |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | × | B4<br>B5 | IN | OUT | | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{ACK_B}$ | $\overline{OBF_B}$ | $INTR_B$ | OUT |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | × | B6<br>B7 | IN | OUT | | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{STB_B}$ | $IBF_B$ | $INTR_B$ | IN |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | × | BC<br>BD | IN | IN | | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{ACK_B}$ | $\overline{OBF_B}$ | $INTR_B$ | OUT |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | × | BE<br>BF | IN | IN | | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{STB_B}$ | $IBF_B$ | $INTR_B$ | IN |

Table 5. Mode 2 Control Words

| Control Word | | | | | | | | | Group A | | | | | | Group B | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | Hexa-decimal | Port A | Port C | | | | | Port C | | | Port B |
| | | | | | | | | | | $PC_7$ | $PC_6$ | $PC_5$ | $PC_4$ | $PC_3$ | $PC_2$ | $PC_1$ | $PC_0$ | |
| 1 | 1 | × | × | × | 0 | 0 | 0 | C0 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | OUT | | | OUT |
| 1 | 1 | × | × | × | 0 | 0 | 1 | C1 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | IN | | | OUT |
| 1 | 1 | × | × | × | 0 | 1 | 0 | C2 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | OUT | | | IN |
| 1 | 1 | × | × | × | 0 | 1 | 1 | C3 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | IN | | | IN |
| 1 | 1 | × | × | × | 1 | 0 | × | C4 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{ACK_B}$ | $\overline{OBF_B}$ | $INTR_B$ | OUT |
| 1 | 1 | × | × | × | 1 | 1 | × | C6 | ←→ | $\overline{OBF_A}$ | $\overline{ACK_A}$ | $IBF_A$ | $\overline{STB_A}$ | $INTR_A$ | $\overline{STB_B}$ | $IBF_B$ | $INTR_B$ | IN |

Table 6. Control Words for Port C Bit Set/Reset

| Control Word | | | | | | | | | Port C | | | | | | | | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | Hexa-decimal | $PC_7$ | $PC_6$ | $PC_5$ | $PC_4$ | $PC_3$ | $PC_2$ | $PC_1$ | $PC_0$ | |
| 0 | × | × | × | 0 | 0 | 0 | 0 | 00 | | | | | | | | 0 | |
| 0 | × | × | × | 0 | 0 | 0 | 1 | 01 | | | | | | | | 1 | |
| 0 | × | × | × | 0 | 0 | 1 | 0 | 02 | | | | | | | 0 | | |
| 0 | × | × | × | 0 | 0 | 1 | 1 | 03 | | | | | | | 1 | | |
| 0 | × | × | × | 0 | 1 | 0 | 0 | 04 | | | | | | 0 | | | Mode 1 Input : $INTE_B$ set/reset<br>Mode 1 Output : $INTE_B$ set/reset |
| 0 | × | × | × | 0 | 1 | 0 | 1 | 05 | | | | | | 1 | | | |
| 0 | × | × | × | 0 | 1 | 1 | 0 | 06 | | | | | 0 | | | | |
| 0 | × | × | × | 0 | 1 | 1 | 1 | 07 | | | | | 1 | | | | |
| 0 | × | × | × | 1 | 0 | 0 | 0 | 08 | | | | 0 | | | | | Mode 1 Input : $INTE_A$ set/reset<br>Mode 2 : $INTE_2$ set/reset |
| 0 | × | × | × | 1 | 0 | 0 | 1 | 09 | | | | 1 | | | | | |
| 0 | × | × | × | 1 | 0 | 1 | 0 | 0A | | | 0 | | | | | | |
| 0 | × | × | × | 1 | 0 | 1 | 1 | 0B | | | 1 | | | | | | |
| 0 | × | × | × | 1 | 1 | 0 | 0 | 0C | | 0 | | | | | | | Mode 1 Output : $INTE_A$ set/reset<br>Mode 2 : $INTE_1$ set/reset |
| 0 | × | × | × | 1 | 1 | 0 | 1 | 0D | | 1 | | | | | | | |
| 0 | × | × | × | 1 | 1 | 1 | 0 | 0E | 0 | | | | | | | | |
| 0 | × | × | × | 1 | 1 | 1 | 1 | 0F | 1 | | | | | | | | |

## Sample Application Circuit

1. Mode 0

A typical Mode 0 application circuit is shown in Figure 12. This circuit has 8 input pins and 16 output pins. The CPU used is the 8085.

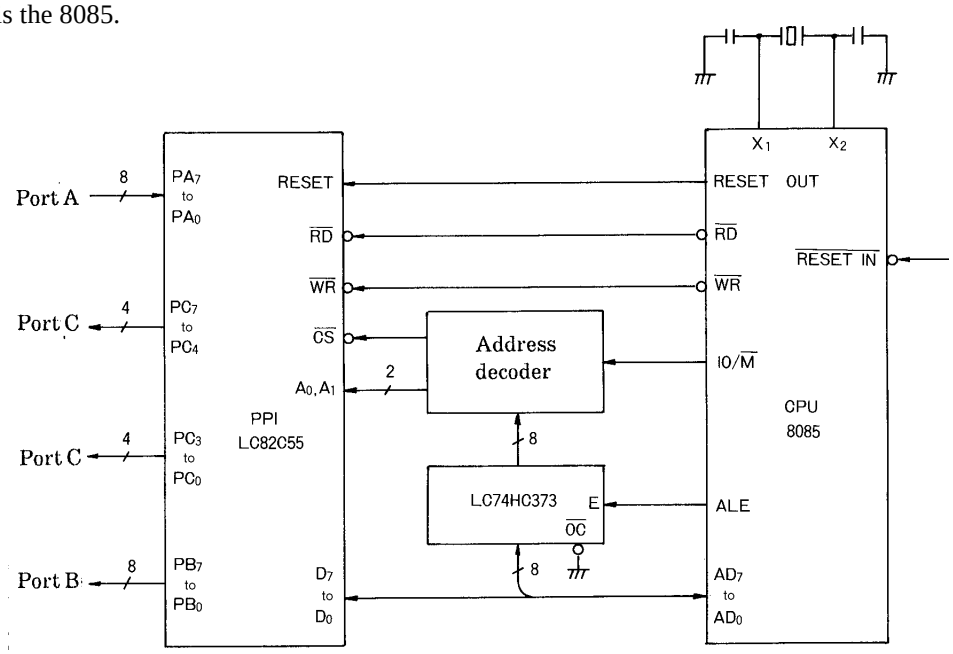



Figure 12. Mode 0 Application Circuit

The control word for this particular input/output configuration is 10010000 (90H). The PPI is initialized by the following 8085 instructions:

```
MVI     A, 90H
OUT     03H
```

The instruction sequence for reading data from Port A and writing it to Ports B and C is as follows:

```
IN      00H     Port
OUT     01H     Register
OUT     02H     Register
```

The following instruction sequence reads data from Port A, outputs it to Port B, and sets Bit 0 of Port C.

```
IN      00H         Port
OUT     01H         Register
MVI     A, 01H      Control
OUT     03H         Output
```

2. Mode 1

A typical application circuit for Mode 1 is shown in Figure 13.

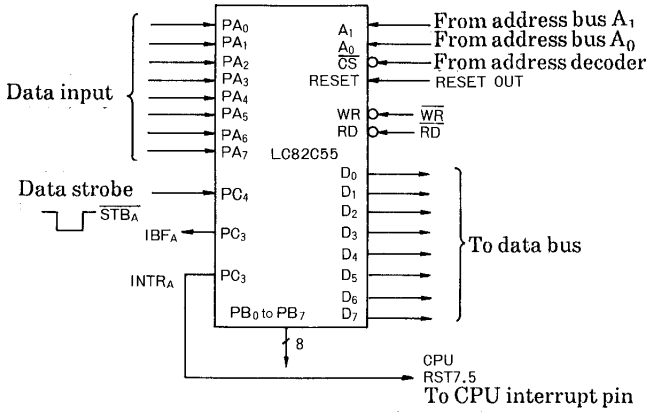



Figure 13. Mode 1 Application Circuit

The peripheral device can latch data into Port A using the input strobe signal $\overline{STB_A}$. The input buffer full flag $IBF_A$ is set to High. If interrupt request generation has been enabled by setting the $INTE_A$ flag, an interrupt request is generated on $INTR_A$. For polled operation, the CPU can check the value of the $IBF_A$ flag by reading Port C of the LC82C55.
The following program examples demonstrate the use of the Mode 1 application circuit.

```
MVI     A, B0H      Control word 10110000. Port A set to input, Ports B and C set to output.
OUT     03H         Output to control address
MVI     A, 09H      Set the INTE flag, 00001001.
OUT     03H         Output to control address
EI                  Enable processor interrupts.
HALT                Wait for input data.
```

When data is strobed into Port A by the $\overline{STB_A}$ signal, the input data is latched into the Port A input buffer. The CPU transfers control to the RST7.5 interrupt vector (003CH). A typical RST7.5 interrupt service routine is as follows:

```
        ORG   003CH     Location set to 003CH
003CH   IN    00H       Read Port A.
        EI              Enable Interrupts.
        RET             Return
```

3. Mode 2

A typical application circuit for Mode 2 is shown in Figure 14. This circuit demonstrates the use of a bi-directional Mode 2 interface in a master/slave CPU system configuration.

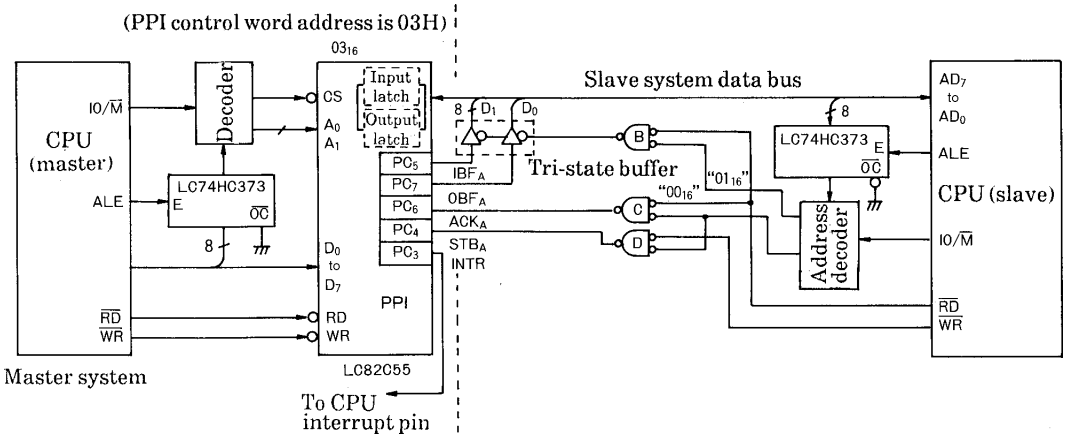



Figure 14. Mode 2 Application Circuit

The LC82C55 is mapped into the I/O address space of the master CPU. The master CPU must initialize Group A to Mode 2 operation.

The tri-state bi-direcitonal I/O pins of Port A are directly connected to the slave CPU data bus. Additional circuitry is used to allow the slave CPU to read the LC82C55 $IBF_A$ (input buffer full) and $\overline{OBF_A}$ (output buffer full) signals as Bits 1 and 0 of I/O address 01H. Port A of the LC82C55 is located at I/O address 00H. A read by the slave CPU from this address activates the $ACK_A$ input signal, and data is transferred from Port A to the slave CPU. A write activates the $\overline{STB_A}$ input signal, causing data from the slave CPU to be loaded into the input latch of Port A.

Both reads from and writes to the LC82C55 by the slave CPU can generate an interrupt to the master CPU via the LC82C55 INTR output signal. These interrupts are enabled or disabled by setting the appropriate INTE1 and INTE2 flags using the Port C bit set/reset commands.

Data transfer from master CPU to slave CPU

- The slave CPU writes a byte of data to Port A of the LC82C55 (I/O address 00H). $IBF_A$ is set to High.
- The master CPU writes a byte of data to Port A of the LC82C55. The $\overline{OBF_A}$ signal goes Low.
- The slave CPU polls the $\overline{OBF_A}$ flag (Bit 0 of I/O address 01N). When $\overline{OBF_A}$ is read as active, the slave CPU reads the data byte from Port A (I/O address 00H). $\overline{OBF_A}$ returns to High.
- The master CPU polls the status of the $\overline{OBF_A}$ and $IBF_A$ flags by reading Port C of the LC82C55. It waits for a High level on $\overline{OBF_A}$, indicating that the previous data byte has been read, before writing another byte. The $IBF_A$ flag may also be checked at this time.

Data transfer from slave CPU to the master CPU

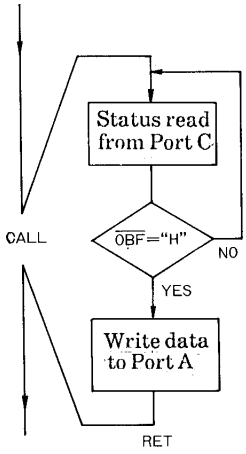
- The slave CPU writes a byte of data to Port A of the LC82C55 (I/O address 00H). $IBF_A$ is set to High.
- The master CPU checks the status of the $IBF_A$ flag by reading Port C of the LC82C55. If High, the master CPU reads a byte of data from Port A. $IBF_A$ is reset to Low.
- The slave CPU polls the $IBF_A$ flag (Bit 1 of I/O address 01H). A Low level indicates that the previous data byte has been read by the master CPU, and another byte can then be written.

The above data transfers operations have not used the INTR signal to interrupt the main CPU. If INTR is used, polling of the $\overline{OBF_A}$ and $IBF_A$ flags by the master CPU is not necessary.

Note that there are separate latches for input and output data. A complete data transfer in one direction does not have to be completed before a transfer in the opposite direction is initiated.

Program examples for the master/slave CPU system.

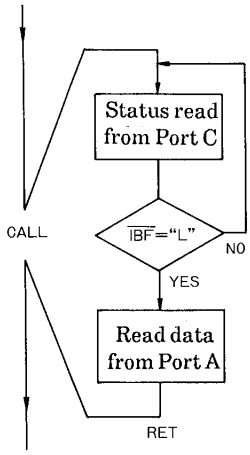
(1) Master CPU program to transfer data to the slave CPU.




Program example

```
MOUT :  PUSH   PSW
OBF :   IN     0 2 H
        ANI    8 0 H
        JNZ    OBF
        POP    PSW
        OUT    0 0 H
        RET
```

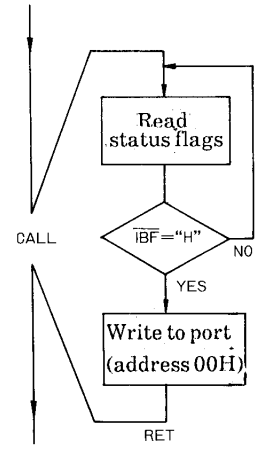
(2) Master CPU program to receive data from the slave CPU.




Program example

```
MIN :   IN     0 2 H
        ANI    2 0 H
        JZ     MIN
        IN     0 0 H
        RET
```

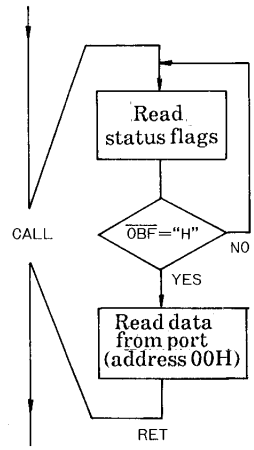
(3) Slave CPU program to transfer data to the master CPU.




Program example

```
SOUT :  PUSH   PSW
IBF :   IN     0 1 H
        ANI    0 2 H
        JNZ    IBF
        POP    PSW
        OUT    0 0 H
        RET
```

(4) Slave CPU program to receive data from the master CPU.




Program example

```
SIN :   IN     0 1 H
        ANI    0 1 H
        JZ     SIN
        IN     0 0 H
        RET
```

4. PPI address decoding

Figures 15 and 16 give examples of address decoding for a system with multiple LC82C55s.

Figures 15 and 16 both perform the same function, since the 8-bit I/O address appears on both the upper and lower halves of the 8085 address bus during an I/O operation. The example in Figure 15 de-multiplexes the lower half of the address bus from the data bus, while the Figure 16 example uses the upper half of the address bus.

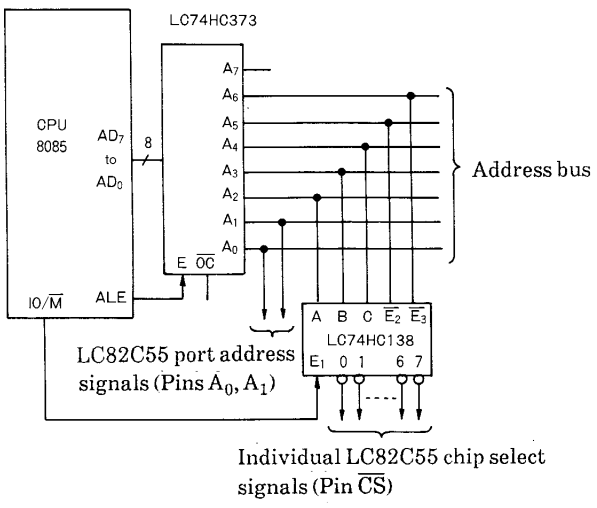



Figure 15. PPI Address Decoding (1)

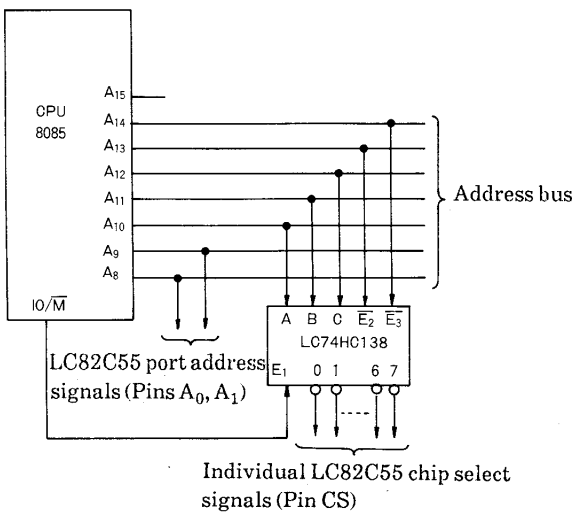



Figure 16. PPI Address Decoding (2)

5. Initial state of PPI

The LC82C55 must be reset after power up, and the operating mode set. Figure 17 shows the power-up and initialization waveforms when the ports are set to output mode.

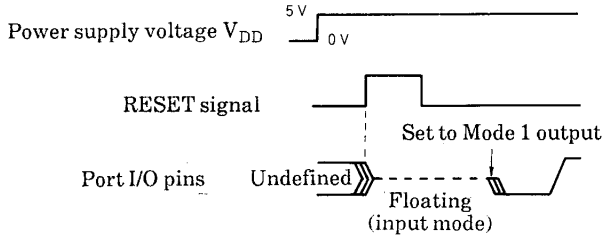



Figure 17. PPI Reset On Power-Up

**Note**

The power-up reset pulse must be at least 50μs long. Subsequent reset pulses must be at least 500ns long.