



LC7942YD

Dot-matrix LCD Driver

Overview

The LC7942YD is a common driver IC for driving large, dot-matrix LCD displays. It features a built-in 64-bit bidirectional shift register and a 4-level LCD driver. It can also be connected in cascade to increase the number of bits.

The LC7942YD is designed to be used with LC7940YD (QFP100) or LC7941YD (QFP100) segment drivers to drive large LCD panels.

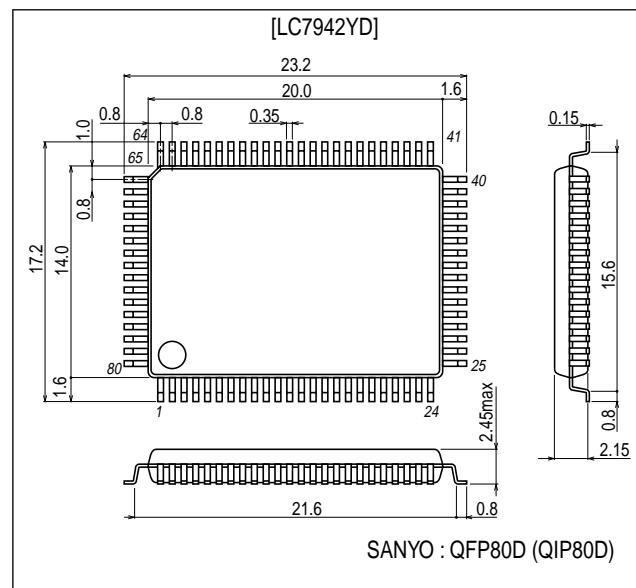
Features

- 64 built-in LCD display drive circuits
- 1/64 to 1/128 display duty cycle
- Input/outputs for cascade connection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature
 - 2.7 to 5.5V logic supply (V_{DD}) at $T_a = -20$ to $+85$ °C
 - 8 to 20 V LCD supply ($V_{DD} - V_{EE}$) at $T_a = -20$ to $+85$ °C
- CMOS process
- 80-pin flat plastic package

Package Dimensions

unit: mm

3177-QFP80D

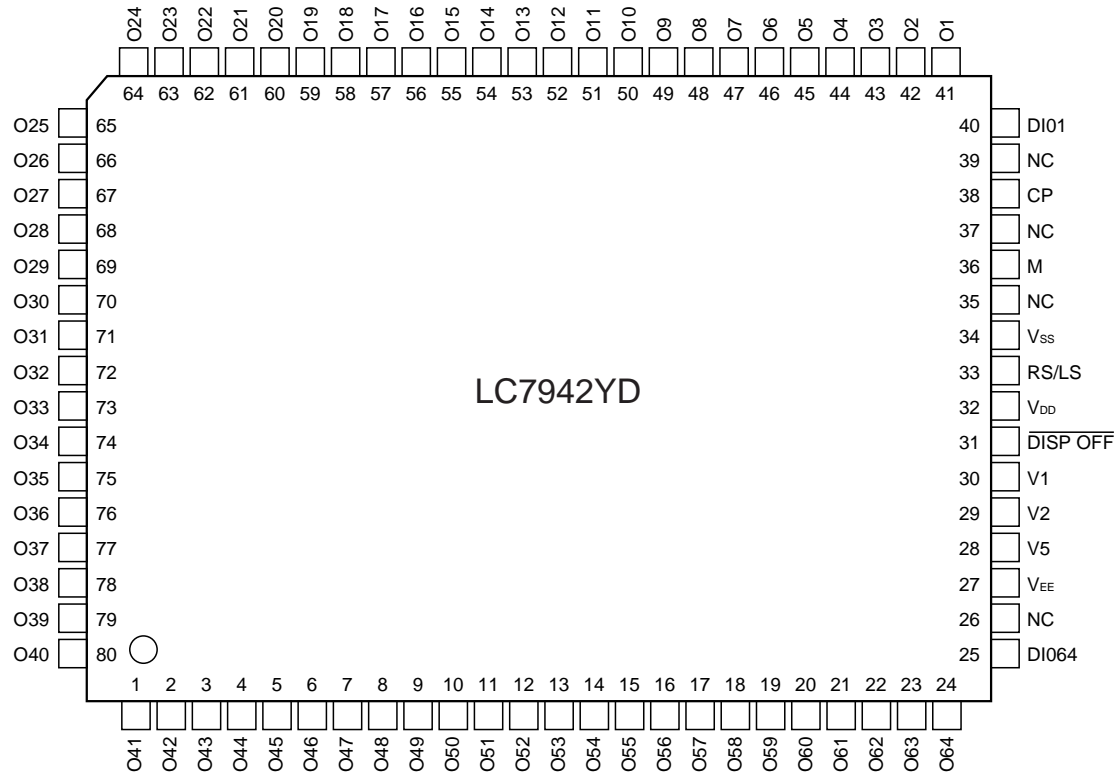


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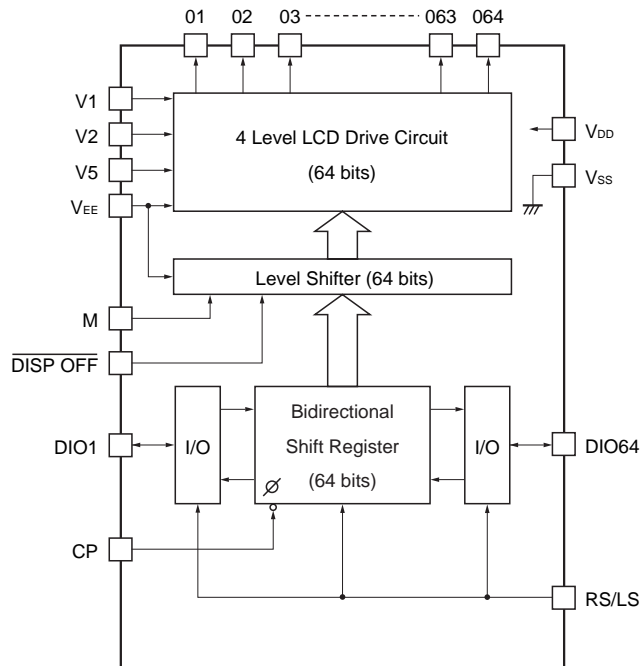
SANYO Electric Co., Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC7942YD

Pad Layout (Top view)



Block Diagram



Pin Functions

Number	Name	I/O	Function																								
32	V _{DD}	Supply	V _{DD} – V _{SS} is the logic supply. V _{DD} – V _{EE} is the LCD supply.																								
34	V _{SS}																										
27	V _{EE}																										
30	V ₁	Supply	LCD panel drive voltage supplies. V ₁ and V _{EE} are selected levels. V ₂ and V ₅ are not-selected levels.																								
29	V ₂																										
28	V ₅																										
38	CP	I	Display data input clock (falling-edge trigger).																								
40	DIO1	I/O	<table><tr><th>RS/LS</th><th>DIO1</th><th>DIO64</th><th>Shift direction</th></tr><tr><td>LOW (right shift)</td><td>Input</td><td>Output</td><td>O1 → O64</td></tr><tr><td>HIGH (left shift)</td><td>Output</td><td>Input</td><td>O64 → O1</td></tr></table>	RS/LS	DIO1	DIO64	Shift direction	LOW (right shift)	Input	Output	O1 → O64	HIGH (left shift)	Output	Input	O64 → O1												
RS/LS	DIO1	DIO64		Shift direction																							
LOW (right shift)	Input	Output		O1 → O64																							
HIGH (left shift)	Output	Input	O64 → O1																								
25	DIO64	I/O																									
33	RS/LS	I																									
36	M	I	LCD panel drive voltage output alternation control signal.																								
31	DISP OFF	I	O1 to O64 output control input pins.																								
41 to 80	O1 to O40	O	LCD drive outputs The output drive level is determined by the display data, M signal and $\overline{\text{DISPOFF}}$ input as show below.																								
1 to 24	O41 to O64		<table><tr><th>M</th><th>Q</th><th>DISPOFF</th><th>Output</th></tr><tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>V₂</td></tr><tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>V_{EE}</td></tr><tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>V₅</td></tr><tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>V₁</td></tr><tr><td>×</td><td>×</td><td>LOW</td><td>V₁</td></tr></table>	M	Q	DISPOFF	Output	LOW	LOW	HIGH	V ₂	LOW	HIGH	HIGH	V _{EE}	HIGH	LOW	HIGH	V ₅	HIGH	HIGH	HIGH	V ₁	×	×	LOW	V ₁
			M	Q	DISPOFF	Output																					
			LOW	LOW	HIGH	V ₂																					
			LOW	HIGH	HIGH	V _{EE}																					
			HIGH	LOW	HIGH	V ₅																					
HIGH	HIGH	HIGH	V ₁																								
×	×	LOW	V ₁																								
Note × = don't care (tied HIGH or LOW)																											
26	NC	–	No connection.																								
35	NC																										
37	NC																										
39	NC																										

Specifications

Absolute Maximum Ratings at Ta = 25 ±2°C, V_{SS} = 0 V

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V _{DD} max	–0.3 to +7.0	V
LCD supply voltage. See note.	V _{DD} – V _{EE} max	0 to 22	V
Input voltage	V _I max	–0.3 to V _{DD} + 0.3	V
Operating temperature range	T _{opr}	–20 to +85	°C
Storage temperature range	T _{stg}	–40 to +125	°C

Note

V_{DD} ≥ V₁ > V₂ > V₅ > V_{EE}

Allowable Operating Ranges at $T_a = -20$ to $+85$ °C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic supply voltage	V_{DD}		2.7	—	5.5	V
LCD supply voltage	$V_{DD} - V_{EE}$	See notes 1 and 2.	8	—	20	V
DIO1, DIO64, CP, M, RS/LS and DISPOFF HIGH-level input voltage	V_{IH}		$0.8V_{DD}$	—	—	V
DIO1, DIO64, CP, M, RS/LS and DISPOFF LOW-level input voltage	V_{IL}		$0.2V_{DD}$	—	—	V
CP shift clock frequency	f_{CP}		—	—	1	MHz
CP pulsewidth	t_{WC}		125	—	—	ns
DIO1 and DIO64 to CP setup time	t_{SETUP}		100	—	—	ns
DIO1 and DIO64 to CP hold time	t_{HOLD}		100	—	—	ns
CP rise time	t_R		—	—	50	ns
CP fall time	t_F		—	—	50	ns

Note

1. $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$
2. At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF, the logic supply should be cut after or simultaneously with the LCD supply.

Electrical Characteristics at $T_a = 25 \pm 2$ °C, $V_{SS} = 0$ V, $V_{DD} = 2.7$ to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DIO1, DIO64, CP, M, RS/LS and DISPOFF HIGH-level input current	I_{IH}	$V_{IN} = V_{DD}$	—	—	1	μA
DIO1, DIO64, CP, M, RS/LS and DISPOFF LOW-level input current	I_{IL}	$V_{IN} = V_{SS}$	—1	—	—	μA
DIO1 and DIO64 HIGH-level output voltage	V_{OH}	$I_{OH} = -400 \mu A$	$V_{DD} - 0.4$	—	—	V
DIO1 and DIO64 LOW-level output voltage	V_{OL}	$I_{OL} = 400 \mu A$	—	—	0.4	V
O1 to O64 driver ON resistance	R_{ON}	$V_{DD} - V_{EE} = 18$ V, $V_{DD} - V_{OL} = 0.25$ V, $V_{DD} = 4.5$ V	—	—	1.5	$k\Omega$
V_{DD} static supply current	I_{DD}	$V_{DD} - V_{EE} = 18$ V, CP = V_{DD}	—	—	100	μA
CP input capacitance	C_I	$f_{CP} = 1$ MHz	—	5	—	pF

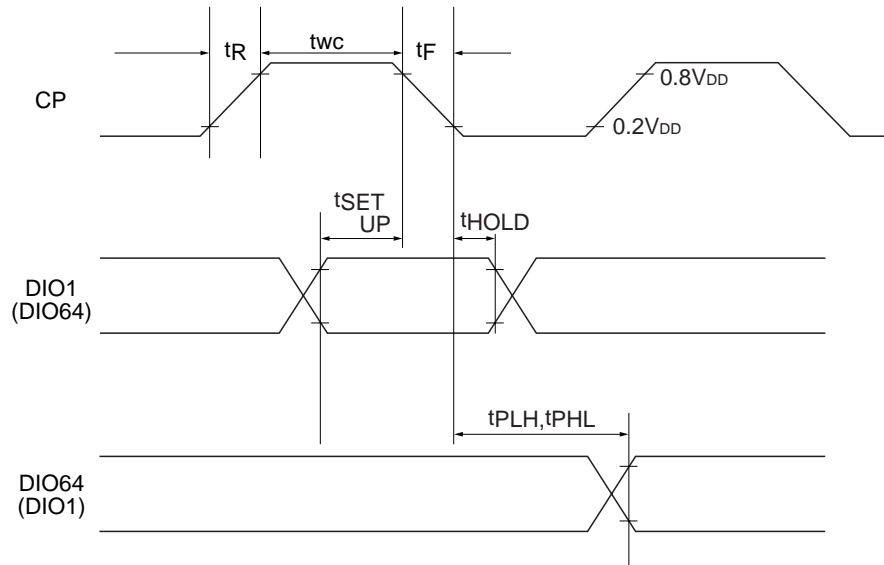
Note

$V_{DE} = V_1$ or V_2 or V_5 or V_{EE} , $V_1 = V_{EE}$, $V_2 = 10/11 \times (V_{DD} - V_{EE})$, $V_5 = 1/11 \times (V_{DD} - V_{EE})$

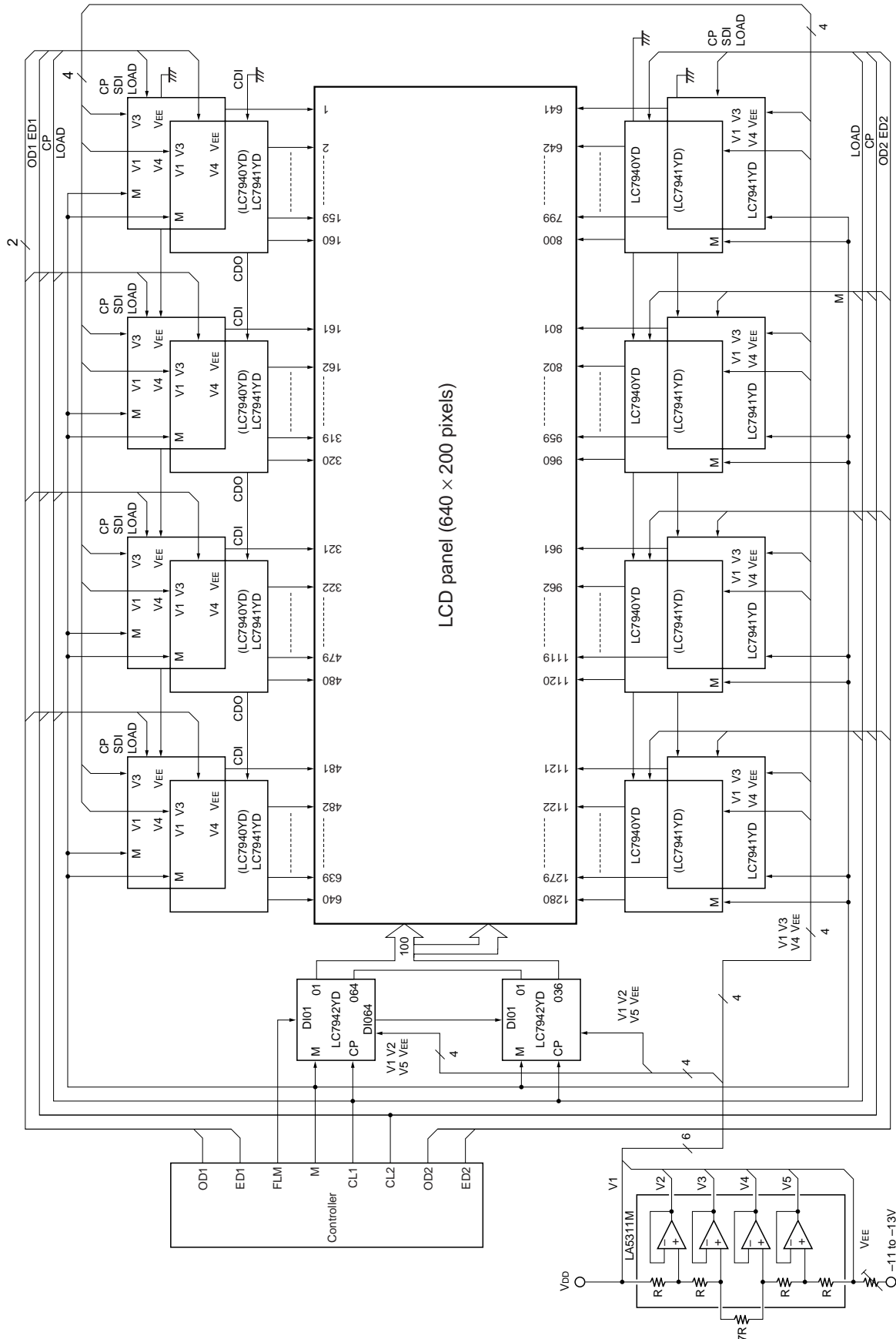
Switching Characteristics at $T_a = 25 \pm 2^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PLH}	$C_L = 30\text{ pF}$	—	—	250	ns
	t_{PHL}		—	—	250	

Switching Characteristics Waveform



LCD Panel



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