

**SANYO****LC79400D****Dot Matrix LCD Driver****Overview**

The LC79400D is a large-scale dot matrix LCD segment driver LSI. Display data transferred from the controller (4-bit parallel format) is processed through 80-bit latching and a LCD drive signal is generated. The LC79400D can be used in conjunction with common driver LC7943D (QIP80D) as well as LC79430D (QIP100D) and LC79431D (QIP100D) to drive a wide-screen LCD panel.

**Features**

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- Supports use of chip disable pin for lower large panel power supply dissipation
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include

$V_{DD}$  (logic block) : 5 V  $\pm 10\%$  /  $-20$  to  $+75$  °C

$V_{DD}-V_{EE}$  (LCD block) : 12 V to 32 V /  $-20$  to  $+75$  °C

- Data transfer clock provides maximum 3.0 MHz and supports bidirectional shift
- 4-bit parallel data input
- CMOS process
- 100-pin flat plastic package

**Specifications**

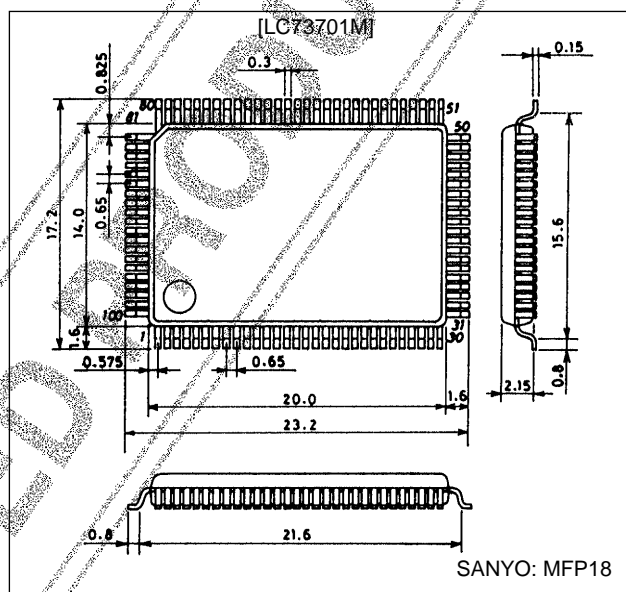
**Absolute Maximum Ratings at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0$  V**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage (logic)	$V_{DD\text{ max}}$		$-0.3$ to $+7.0$	V
Maximum supply voltage (LCD)	$V_{DD}-V_{EE\text{ max}}^{*1}$		0 to 35	V
Maximum input voltage	$V_i\text{ max}$		$-0.3$ to $V_{DD} + 0.3$	V
Storage temperature range	$T_{stg}$		$-40$ to $+125$	°C

Note: 1. The voltages  $V_1$ ,  $V_3$ ,  $V_4$ ,  $V_7$ ,  $V_{DD}$  and  $V_{EE}$  must obey the relationships:  $V_{DD} \geq V_1 > V_3 > V_4 > V_{EE}$ ,  $V_{DD} - V_3 \leq 7V$ ,  $V_4 - V_{EE} \leq 7V$ .

**Package Dimensions**

unit : mm

**3180-QFP100D**

# LC79400D

## Allowable Operating Ranges at Ta = -20 to +75°C, V<sub>SS</sub> = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage (logic)	V <sub>DD</sub>		4.5		5.5	V
Supply voltage (LCD)	V <sub>DD</sub> - V <sub>EE</sub>	*2, *3	12		32	V
Input high-level voltage	V <sub>IH</sub>	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, DISP OFF	0.8 V <sub>DD</sub>			V
Input low-level voltage	V <sub>IL</sub>	DI1 to 4, CP, LOAD, CDR, CDL R/L, M, DISP OFF			0.2 V <sub>DD</sub>	V
CP (shift clock)	f <sub>CP</sub>	CP			3.0	MHz
CP (pulse width)	t <sub>WC</sub>	CP	100			ns
LOAD pulse width	t <sub>WL</sub>	LOAD	100			ns
Setup time	t <sub>SETUP</sub>	DI1 to 4 → CP	80			ns
Hold time	t <sub>HOLD</sub>	DI1 to 4 → CP	80			ns
CP → LOAD	t <sub>CL1</sub>	CP → LOAD	0			ns
	t <sub>CL2</sub>	CP → LOAD	100			ns
LOAD → CP	t <sub>LC</sub>	LOAD → CP	63			ns
Rise/Fall time	t <sub>R</sub>	CP			50	ns
	t <sub>F</sub>	CP			50	ns
	t <sub>RL</sub>	LOAD			50	ns
	t <sub>FL</sub>	LOAD			50	ns

Note:2. The voltages V<sub>1</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>7</sub>, V<sub>DD</sub> and V<sub>EE</sub> must obey the relationships: V<sub>DD</sub> ≥ V<sub>1</sub> > V<sub>3</sub> > V<sub>4</sub> > V<sub>EE</sub>, V<sub>DD</sub> - V<sub>3</sub> ≤ 7V, V<sub>4</sub> - V<sub>EE</sub> ≤ 7V.

3. When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

## Electrical Characteristics at Ta = 25±2°C, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 5 V±10%

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub> ; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, DISP OFF			1	μA
Input low-level current	I <sub>IL</sub>	V <sub>IN</sub> = V <sub>SS</sub> ; LOAD, CP, CDR (CDL), R/L, DI1 to DI4, M, DISP OFF	-1			μA
Output high-level voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA; CDL (CDR)	V <sub>DD</sub> - 0.4			V
Output low-level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 400 μA; CDL (CDR)			0.4	V
Driver on resistor	R <sub>ON1</sub>	V <sub>DD</sub> - V <sub>EE</sub> = 30 V,  V <sub>DE</sub> - V <sub>O</sub>   = 0.5 V*4; Q1 to Q80		1.5	3.0	kΩ
	R <sub>ON2</sub>	V <sub>DD</sub> - V <sub>EE</sub> = 20 V,  V <sub>DE</sub> - V <sub>O</sub>   = 0.5 V*4; O1 to O80		2.0	3.5	kΩ
Standby current dissipation	I <sub>ST</sub>	CDR (CDL) = V <sub>DD</sub> ; V <sub>DD</sub> - V <sub>EE</sub> = 30 V CP = 3.0 MHz, no-load output: V <sub>SS</sub>			200	μA
Operation current dissipation	I <sub>SS</sub> *5	V <sub>DD</sub> - V <sub>EE</sub> = 30 V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V <sub>SS</sub>			4.0	mA
	I <sub>SS</sub> *6	V <sub>DD</sub> - V <sub>EE</sub> = 30 V, CP = 3 MHz, LOAD = 14 kHz, M = 35 Hz; V <sub>EE</sub>			0.1	mA
Input capacity	C <sub>I</sub>	f = 3.0 MHz; CP		5		pF

Note:4. V<sub>DE</sub> = V<sub>1</sub> or V<sub>3</sub> or V<sub>4</sub> or V<sub>EE</sub>, V<sub>1</sub> = V<sub>DD</sub>, V<sub>3</sub> = 15/17 (V<sub>DD</sub> - V<sub>EE</sub>), V<sub>4</sub> = 2/17 (V<sub>DD</sub> - V<sub>EE</sub>)

5. I<sub>SS</sub> current flows from V<sub>DD</sub> to V<sub>SS</sub>.

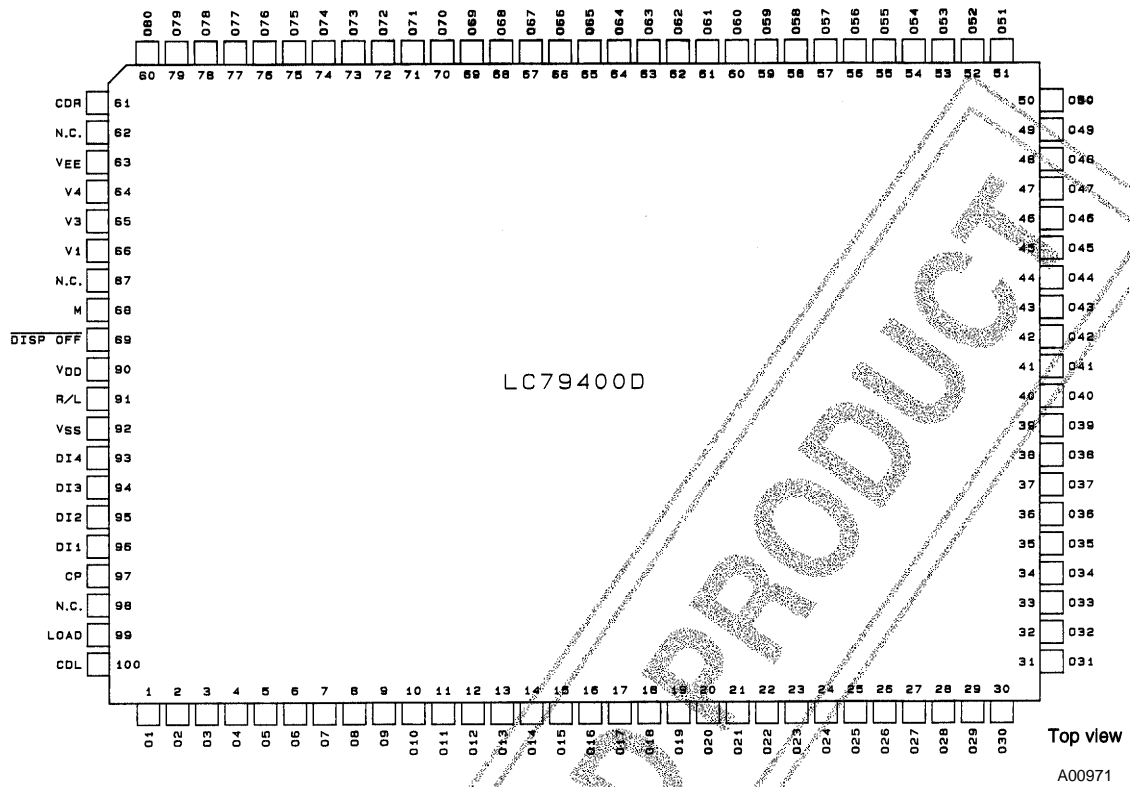
6. I<sub>EE</sub> current flows from V<sub>DD</sub> to V<sub>EE</sub>.

## Switching Characteristics at Ta = 25±2°C, V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 5 V±10%

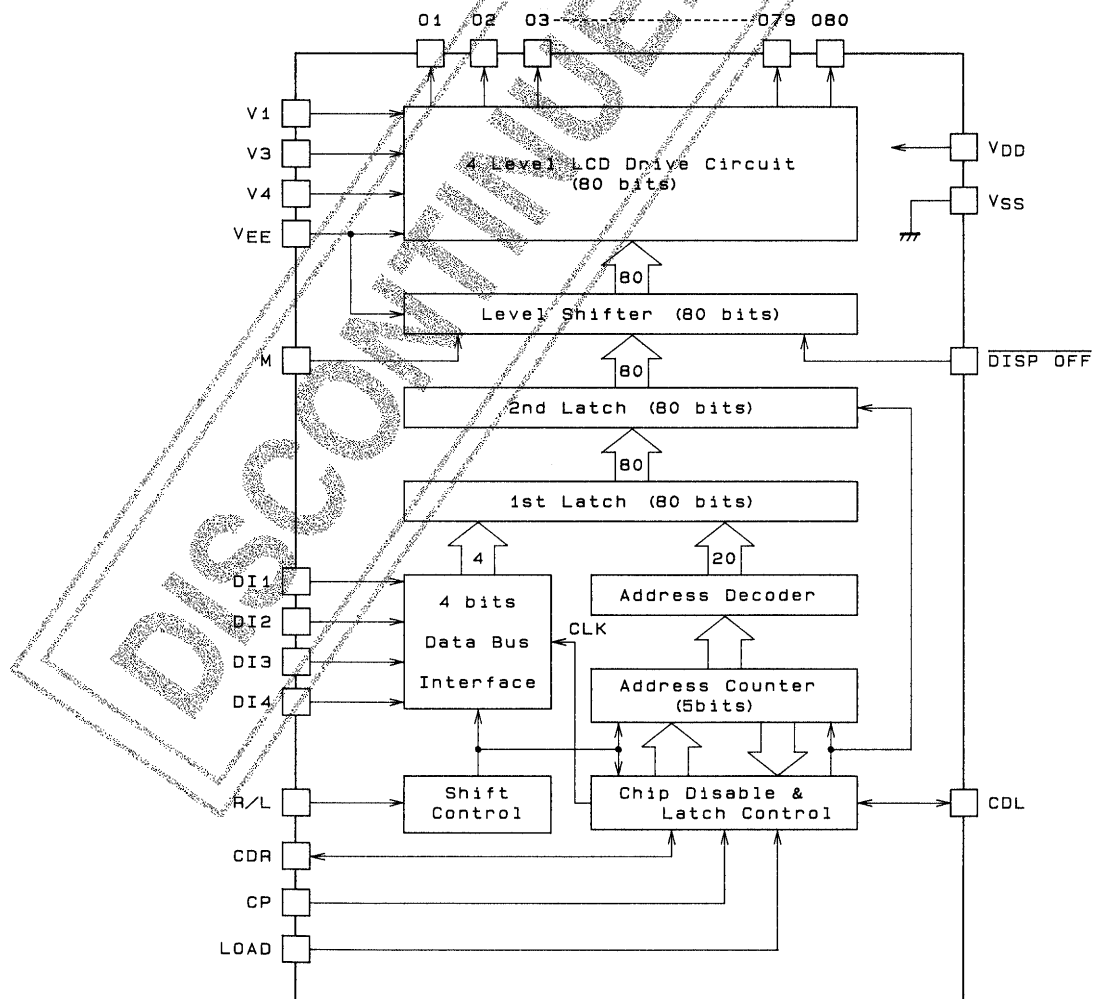
Parameter	Symbol	Conditions	min	typ	max	Unit
Output delay time	t <sub>D</sub>	Load = 15 pF; CDR (CDL)			200	ns

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## Pin Assignment



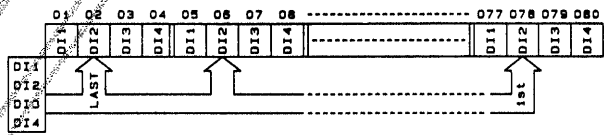
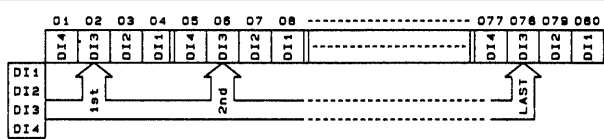
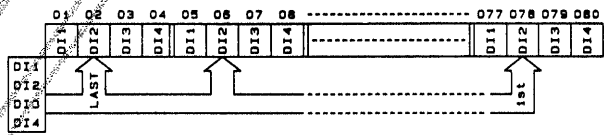
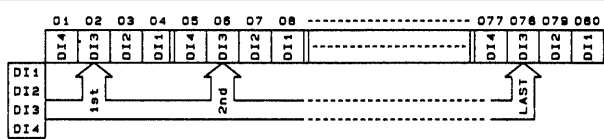
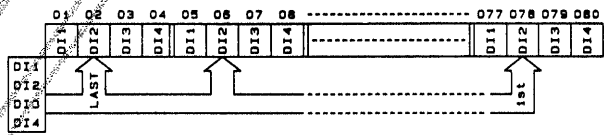
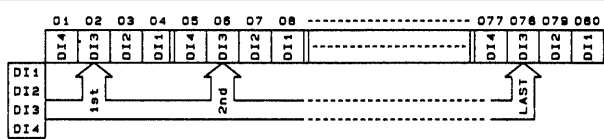
## Equivalent Circuit Block Diagram



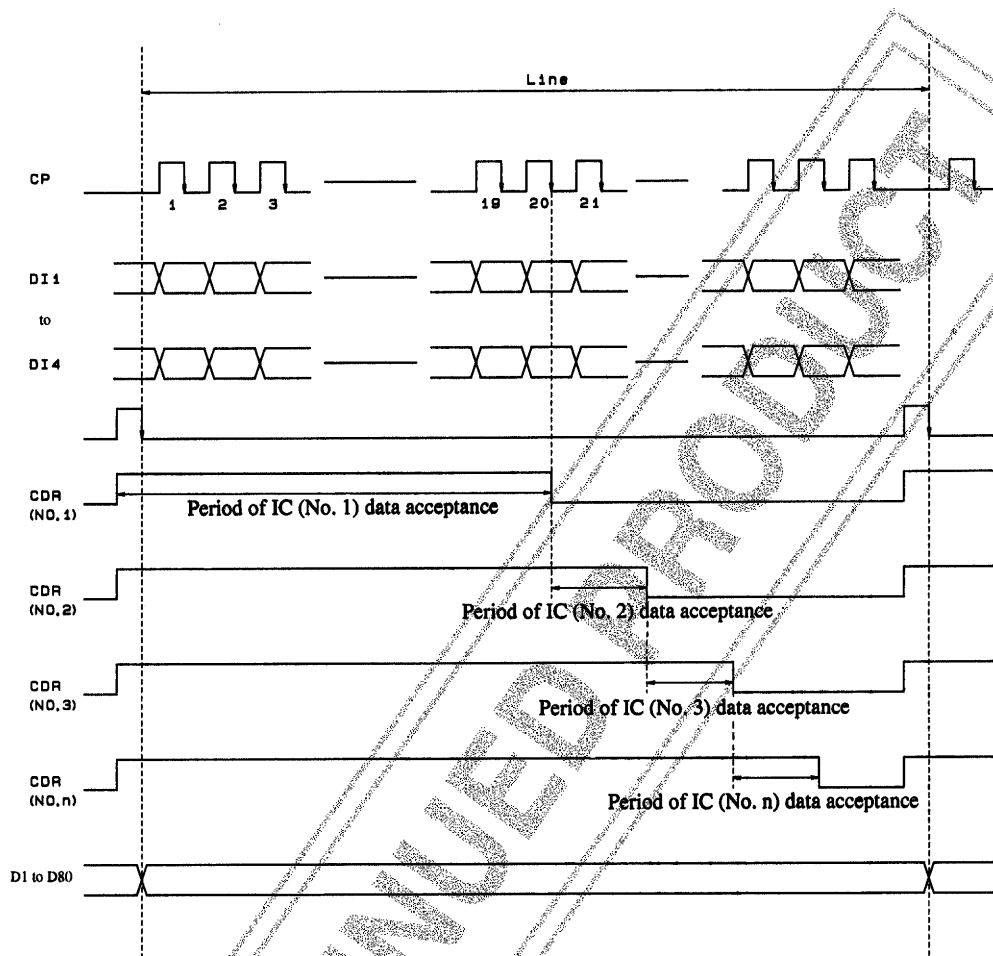
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# LC79400D

## Pin Descriptions

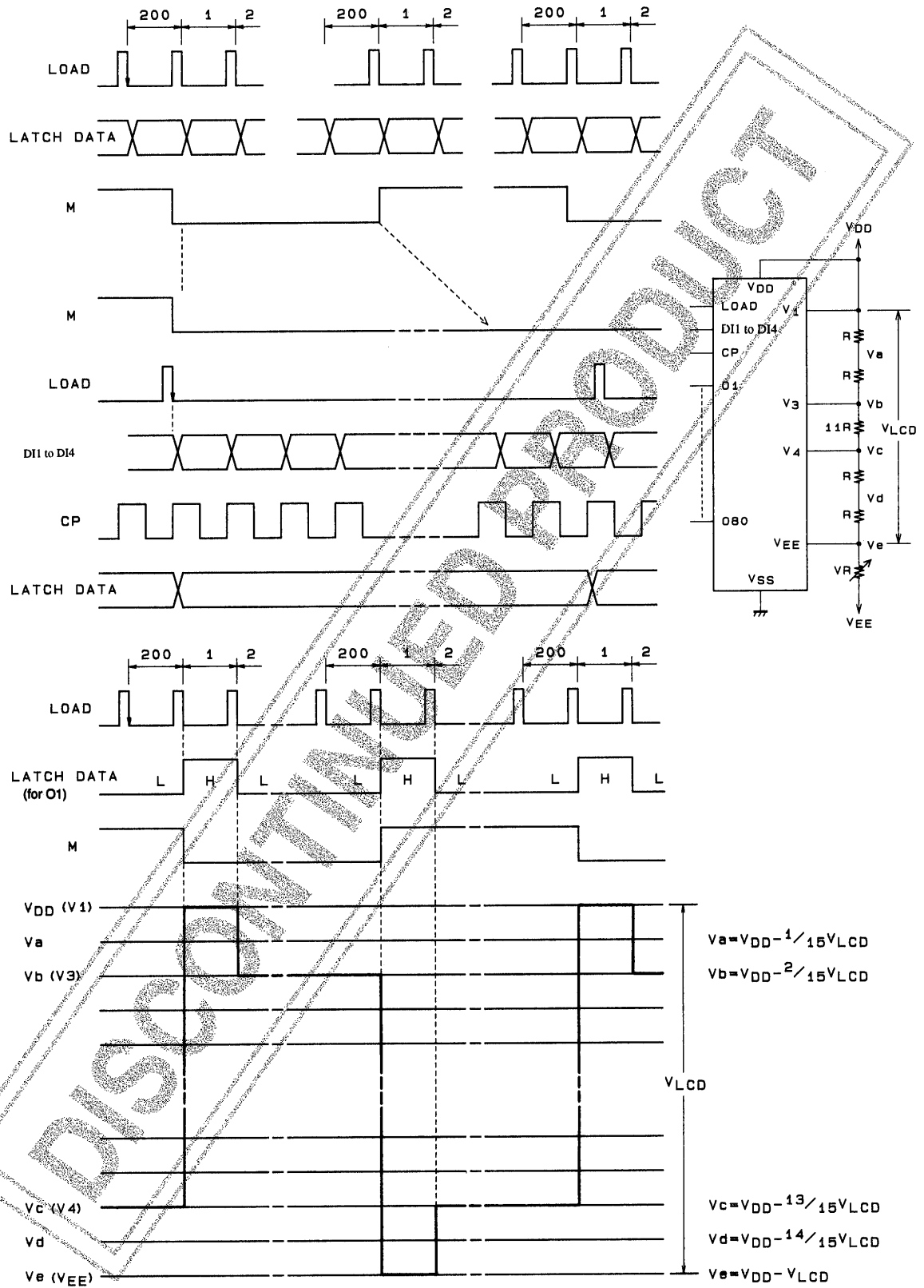
Pin No	Pin name	Input/Output	Functions																							
90	V <sub>DD</sub>	Power supply	V <sub>DD</sub> and V <sub>SS</sub> : Power supply for logic section																							
92	V <sub>SS</sub>																									
83	V <sub>EE</sub>		V <sub>DD</sub> and V <sub>EE</sub> : Power supply for LCD drive circuit																							
86	V1	Power supply	LCD drive level power supply																							
85	V3		V1 and V <sub>EE</sub> : Select level																							
84	V4		V3 and V4 : Nonselect level																							
97	CP	Input	Display data shift clock (triggering on the trailing edge)																							
81	CDR	Input/Output	Chip disable pin																							
100	CDL	Input/Output	H level : Data not accepted L level : Data accepted																							
<table><tr><th>Pin Name</th><th>Input/Output</th><th>R/L</th><th>Pin Description</th></tr><tr><td>CDR</td><td>Input</td><td>L</td><td>Control input pin for the IC's internal disable F/F.</td></tr><tr><td>CDL</td><td>Output</td><td></td><td>Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.</td></tr><tr><td>CDL</td><td>Input</td><td>H</td><td>Control input pin for the IC's internal disable F/F.</td></tr><tr><td>CDR</td><td>Output</td><td></td><td>Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.</td></tr></table>				Pin Name	Input/Output	R/L	Pin Description	CDR	Input	L	Control input pin for the IC's internal disable F/F.	CDL	Output		Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.	CDL	Input	H	Control input pin for the IC's internal disable F/F.	CDR	Output		Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.			
Pin Name	Input/Output	R/L	Pin Description																							
CDR	Input	L	Control input pin for the IC's internal disable F/F.																							
CDL	Output		Output pin of the IC's internal disable F/F. Connects to the next stage CDR pin when establishing a cascade connection.																							
CDL	Input	H	Control input pin for the IC's internal disable F/F.																							
CDR	Output		Output pin of the IC's internal disable F/F. Connects to the next stage CDL pin when establishing a cascade connection.																							
99	LOAD	Input	Display data latch clock (triggering on the trailing edge). On the trailing edge, output levels switch in response to the particular combination of display data, M and DISP OFF signals.																							
93	DI4	Input	<table><tr><th>R/L</th><th>Input data and latch address</th></tr><tr><td>L</td><td></td></tr><tr><td>H</td><td></td></tr></table>	R/L	Input data and latch address	L		H																		
R/L	Input data and latch address																									
L																										
H																										
94	DI3																									
95	DI2																									
96	DI1																									
88	M	Input	LCD drive output alternating signal																							
91	R/L	Input	Input pin which performs input/output switching for CDR and CDL pins and directional shift for 4-bit parallel input data.																							
1	O1	Output	LCD drive output																							
2	O2																									
79	O79																									
80	O80																									
<table><tr><th>M</th><th>Q</th><th>DISP OFF</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V4</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V<sub>EE</sub></td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table> <p>*Don't care (To be set to either "H" or "L")</p>			M	Q	DISP OFF	Output	L	L	H	V3	L	H	H	V1	H	L	H	V4	H	H	H	V <sub>EE</sub>	*	*	L	V1
M	Q	DISP OFF	Output																							
L	L	H	V3																							
L	H	H	V1																							
H	L	H	V4																							
H	H	H	V <sub>EE</sub>																							
*	*	L	V1																							
89	DISP OFF	Input	Input pin which controls output pins O1 to O80. V1 level is output from O1 to O80 pin output during the low level input interval (See logic table).																							

## Operation Timing (for R/L = H)

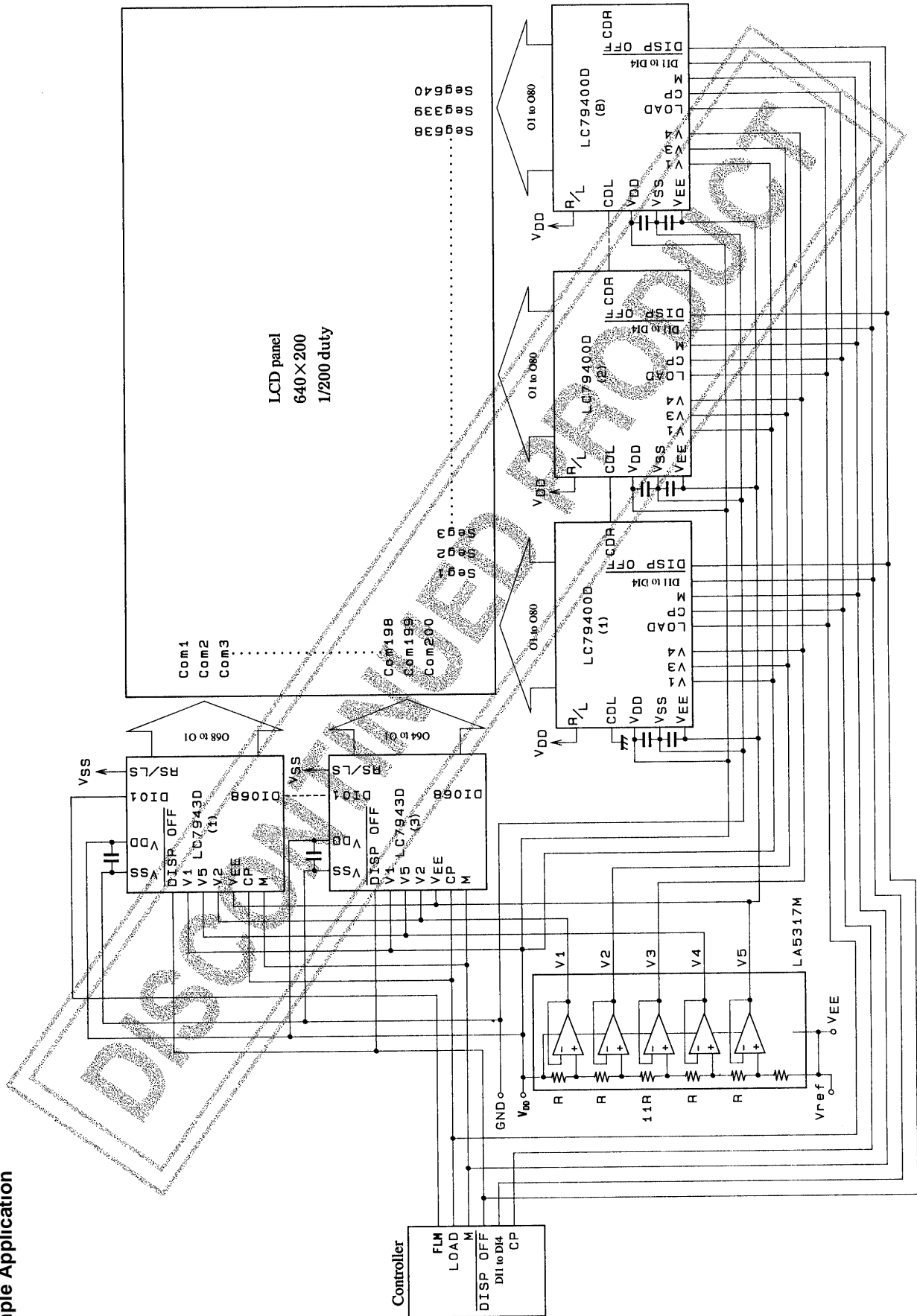


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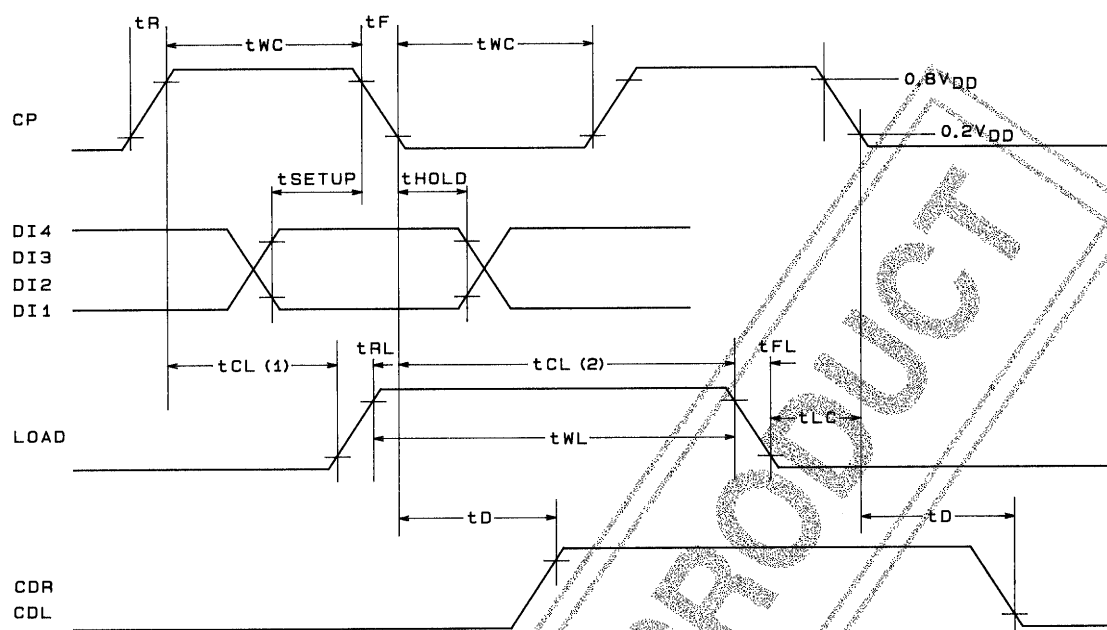
Time Chart (1/200 Duty 1/15 Bias) Switching Characteristics



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## Switching Characteristics



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