



# LC7935AN

## General-Purpose 32-Bit Shift Register Latch Driver

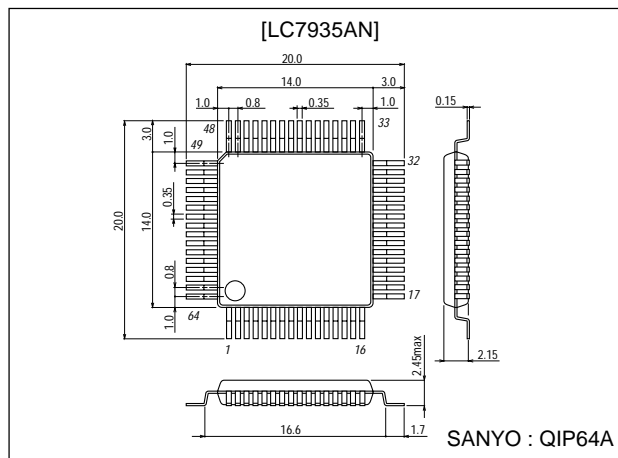
### Features

- High-speed, high-voltage silicon gate CMOS device.
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock (CLOCK).
- 32-bit latch data is changed on the negative transition of the LATCH pad and is held on the positive transition.
- The STROBE pad, BEO pad can be used to exercise on/off control of the output driver.
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads).
- Maximum ratings of driver output:  $V_O = 28V$ ,  $I_{OL} = 30mA$ .
- Logic unit operating voltage:  $V_{DD} = 4.5$  to  $5.5V$ .

### Package Dimensions

unit:mm

3057-QIP64A



### Specifications

Absolute Maximum Ratings at  $T_a = 25^\circ C$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}$		-0.3 to +7.0	V
Input voltage	$V_I$		-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_{O1}$	$S_{OUT}$ output	-0.3 to $V_{DD} + 0.3$	V
	$V_{O2}$	D1 to D32 output, output Tr off	28	V
Output current	$I_O$	D1 to D32 output, per output	30	mA
Allowable power dissipation	Pd max	$T_a = 70^\circ C$	450	mW
Operating temperature	Topr		-10 to +70	$^\circ C$
Storage temperature	Tstg		-35 to +125	$^\circ C$

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## Allowable Operating Conditions at Ta = -10 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	4.5		5.5	V
H-level input voltage	V <sub>IH</sub>	S <sub>IN</sub> , CLOCK, LATCH, BEO, $\overline{\text{STROBE}}$	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
L-level input voltage	V <sub>IL</sub>	S <sub>IN</sub> , CLOCK, LATCH, BEO, $\overline{\text{STROBE}}$	V <sub>SS</sub> (L)		0.2V <sub>DD</sub>	V
Clock frequency	f <sub>CLK</sub>	CLOCK: Duty: 50%			5.0	MHz
Clock pulse width	t <sub>WΦ</sub>	CLOCK	75			ns
Clock rise/fall time	t <sub>r</sub> , t <sub>f</sub>	CLOCK			200	ns
Data setup time	t <sub>DS</sub>	S <sub>IN</sub> , CLOCK	100			ns
Data hold time	t <sub>DH</sub>	S <sub>IN</sub> , CLOCK	50			ns
Latch pulse width	t <sub>WL</sub>	LATCH	100			ns

## Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
H-level input current	I <sub>IH1</sub>	S <sub>IN</sub> , CLOCK, LATCH			10	μA
	I <sub>IH2</sub>	BEO	12		72	μA
L-level input current	I <sub>IL1</sub>	S <sub>IN</sub> , CLOCK, LATCH	-10			μA
	I <sub>IL2</sub>	$\overline{\text{STROBE}}$	-72		-12	μA
H-level output voltage	V <sub>OH</sub>	S <sub>OUT</sub> : V <sub>DD</sub> =5V, I <sub>OH</sub> =-0.5mA	V <sub>DD</sub> -0.5			V
L-level output voltage	V <sub>OL1</sub>	S <sub>OUT</sub> : V <sub>DD</sub> =5V, I <sub>OL</sub> =0.5mA			0.5	V
	V <sub>OL2</sub>	D1 to D32: V <sub>DD</sub> =5V, I <sub>OL</sub> =30mA			0.5	V
Output OFF-state leakage current	I <sub>OFF</sub>	D1 to D32: V <sub>O</sub> =24V			20	μA
Input capacitance	C <sub>IN</sub>	CLOCK		5.0		pF
Operating current drain	I <sub>DD</sub>	V <sub>DD</sub> : V <sub>DD</sub> =5V, f <sub>CLK</sub> =5MHz, All outputs : no load			5	mA

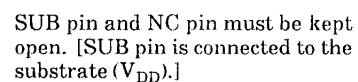
## Switching Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock latch delay width	t <sub>CL</sub>	CLOCK, LATCH: V <sub>DD</sub> =5V	100			ns
Latch clock delay width	t <sub>LC</sub>	CLOCK, LATCH: V <sub>DD</sub> =5V	0			ns
H-level output propagation delay time	t <sub>PLH1</sub>	LATCH, D1 to D32: V <sub>DD</sub> =5V, Dn: R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =15pF			400	ns
	t <sub>PLH2</sub>	BEO, $\overline{\text{STROBE}}$ : V <sub>DD</sub> =5V, Dn: R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =15pF			300	ns
	t <sub>PLH3</sub>	CLOCK, S <sub>OUT</sub> : V <sub>DD</sub> =5V, S <sub>OUT</sub> : C <sub>L</sub> =15pF			200	ns
L-level output propagation delay time	t <sub>PHL1</sub>	LATCH, D1 to D32: V <sub>DD</sub> =5V, Dn: R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =15pF			200	ns
	t <sub>PHL2</sub>	BEO, $\overline{\text{STROBE}}$ , D1 to D32: V <sub>DD</sub> =5V, Dn: R <sub>L</sub> =1.0kΩ, C <sub>L</sub> =15pF			100	ns
	t <sub>PHL3</sub>	CLOCK, S <sub>OUT</sub> : V <sub>DD</sub> =5V, S <sub>OUT</sub> : C <sub>L</sub> =15pF			200	ns

## Driver ON/OFF Truth Table

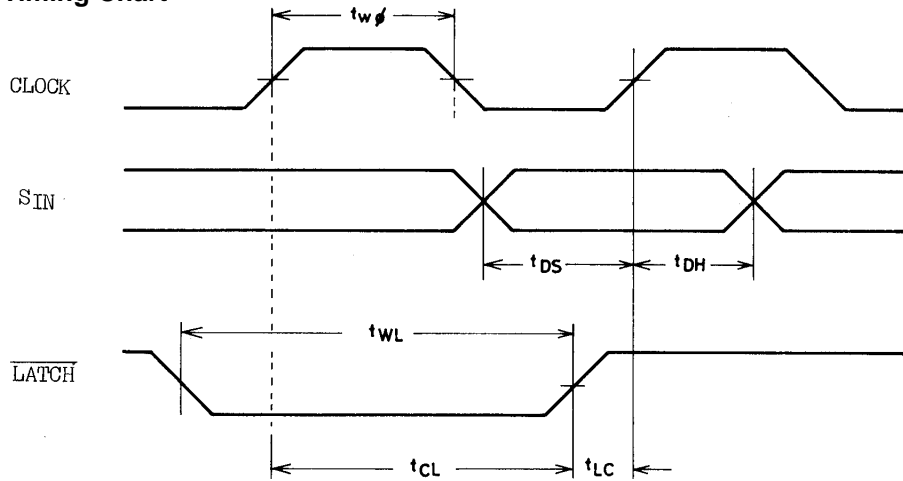
Latch Data (Q)	BEO	$\overline{\text{STROBE}}$	Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

### Equivalent Circuit Block Diagram

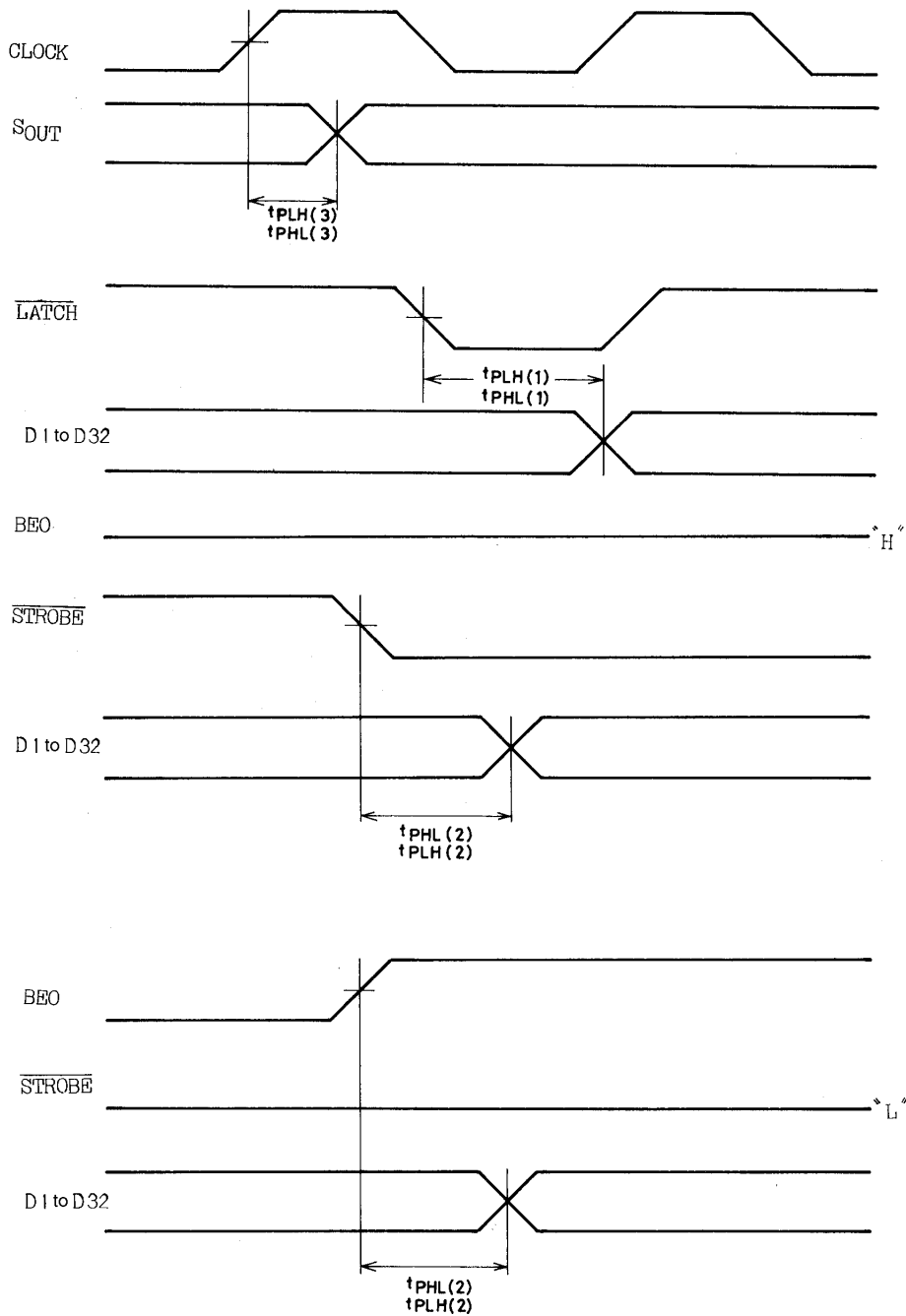


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Input Data Timing Chart



Output Data Timing Chart



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