Ordering number:ENN3183A

CMOS IC

LC7935AN

General-Purpose 32-Bit Shift Register Latch Driver

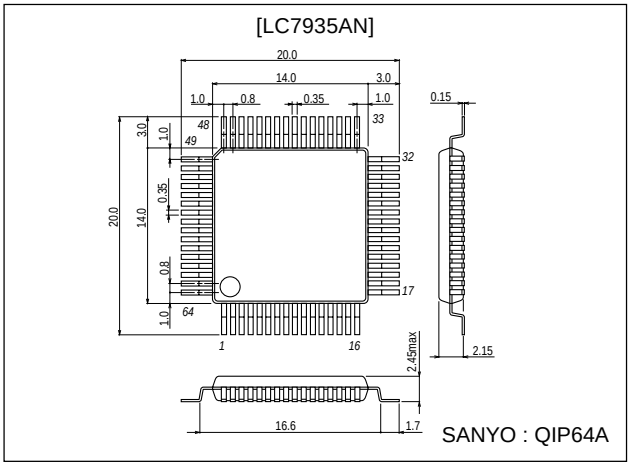
Features

- High-speed, high-voltage silicon gate CMOS device.
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock (CLOCK).
- 32-bit latch data is changed on the negative transition of the $\overline{\text{LATCH}}$ pad and is held on the positive transition.
- The $\overline{\text{STROBE}}$ pad, BEO pad can be used to exercise on/off control of the output driver.
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads).
- Maximum ratings of driver output: V_O = 28V, I_{OL} = 30mA.
- Logic unit operating voltage: V_{DD} = 4.5 to 5.5V.

Package Dimensions

unit:mm

3057-QIP64A



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}		−0.3 to +7.0	V
Input voltage	V_I		−0.3 to V_{DD} +0.3	V
Output voltage	V_O1	S_{OUT} output	−0.3 to V_{DD} +0.3	V
	V_O2	D1 to D32 output, output Tr off	28	V
Output current	I_O	D1 to D32 output, per output	30	mA
Allowable power dissipation	Pd max	Ta=70°C	450	mW
Operating temperature	Topr		−10 to +70	˚C
Storage temperature	Tstg		−35 to +125	˚C

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Allowable Operating Conditions at Ta = –10 to +70˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
H-level input voltage	V_{IH}	S_{IN}, CLOCK, $\overline{LATCH}$, BEO, $\overline{STROBE}$	$0.8V_{DD}$		V_{DD}	V
L-level input voltage	V_{IL}	S_{IN}, CLOCK, $\overline{LATCH}$, BEO, $\overline{STROBE}$	V_{SS}(L)		$0.2V_{DD}$	V
Clock frequency	f_{CLK}	CLOCK: Duty: 50%			5.0	MHz
Clock pulse width	$t_{W\Phi}$	CLOCK	75			ns
Clock rise/fall time	t_r, t_f	CLOCK			200	ns
Data setup time	t_{DS}	S_{IN}, CLOCK	100			ns
Data hold time	t_{DH}	S_{IN}, CLOCK	50			ns
Latch pulse width	t_{WL}	$\overline{LATCH}$	100			ns

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
H-level input current	$I_{IH}1$	S_{IN}, CLOCK, $\overline{LATCH}$			10	µA
	$I_{IH}2$	BEO	12		72	µA
L-level input current	$I_{IL}1$	S_{IN}, CLOCK, $\overline{LATCH}$	–10			µA
	$I_{IL}2$	$\overline{STROBE}$	–72		–12	µA
H-level output voltage	V_{OH}	S_{OUT}: V_{DD}=5V, I_{OH}=–0.5mA	V_{DD}–0.5			V
L-level output voltage	$V_{OL}1$	S_{OUT}: V_{DD}=5V, I_{OL}=0.5mA			0.5	V
	$V_{OL}2$	D1 to D32: V_{DD}=5V, I_{OL}=30mA			0.5	V
Output OFF-state leakage current	I_{OFF}	D1 to D32: V_O=24V			20	µA
Input capacitance	C_{IN}	CLOCK		5.0		pF
Operating current drain	I_{DD}	V_{DD}: V_{DD}=5V, f_{CLK}=5MHz, All outputs : no load			5	mA

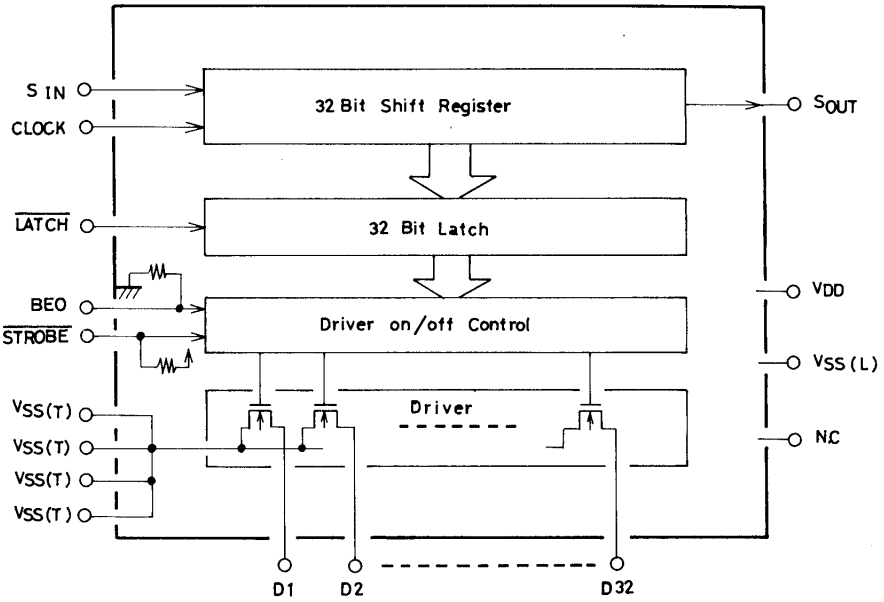
Switching Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock latch delay width	t_{CL}	CLOCK, $\overline{LATCH}$: V_{DD}=5V	100			ns
Latch clock delay width	t_{LC}	CLOCK, $\overline{LATCH}$: V_{DD}=5V	0			ns
H-level output propagation delay time	$t_{PLH}1$	LATCH, D1 to D32: V_{DD}=5V, Dn: R_L=1.0kΩ, C_L=15pF			400	ns
	$t_{PLH}2$	BEO, $\overline{STROBE}$: V_{DD}=5V, Dn: R_L=1.0kΩ, C_L=15pF			300	ns
	$t_{PLH}3$	CLOCK, S_{OUT}: V_{DD}=5V, S_{OUT}: C_L=15pF			200	ns
L-level output propagation delay time	$t_{PHL}1$	$\overline{LATCH}$, D1 to D32: V_{DD}=5V, Dn: R_L=1.0kΩ, C_L=15pF			200	ns
	$t_{PHL}2$	BEO, $\overline{STROBE}$, D1 to D32: V_{DD}=5V, Dn: R_L=1.0kΩ, C_L=15pF			100	ns
	$t_{PHL}3$	CLOCK, S_{OUT}: V_{DD}=5V, S_{OUT}: C_L=15pF			200	ns

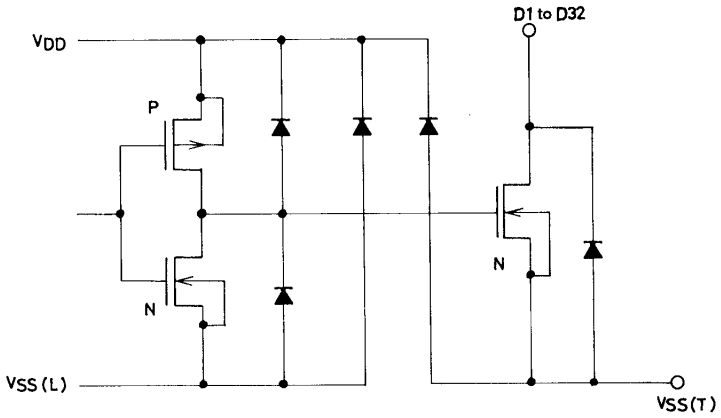
Driver ON/OFF Truth Table

Latch Data (Q)	BEO	$\overline{STROBE}$	Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

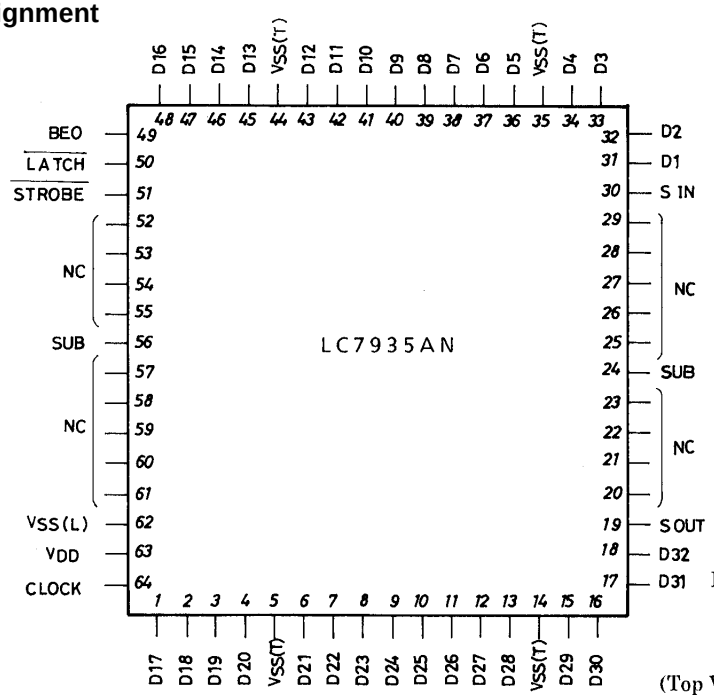
Equivalent Circuit Block Diagram



Output Driver Section Equivalent Circuit



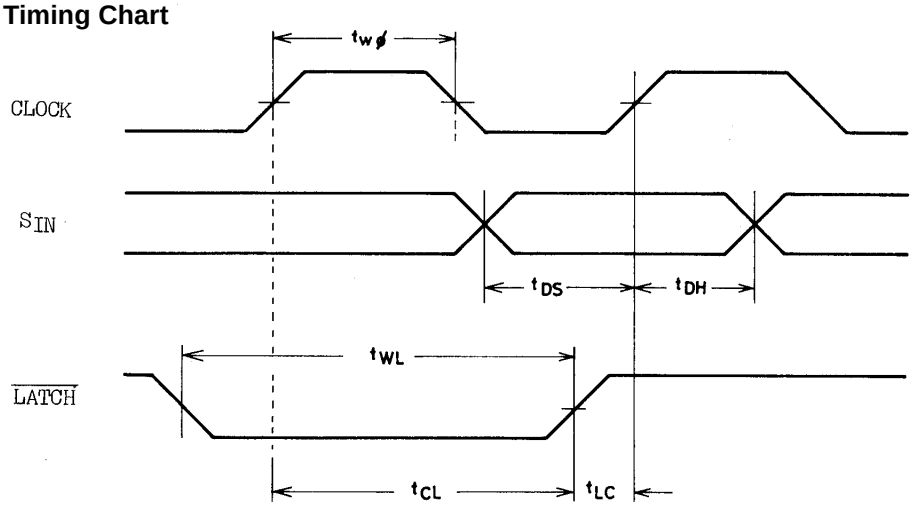
Pin Assignment



(Top View)

Note : SUB pin and NC pin must be kept open. [SUB pin is connected to the substrate (V_{DD}).]

Input Data Timing Chart



Output Data Timing Chart