Ordering number : EN*5236

CMOS LSI

LC78845Q

Sample Rate Converter for Digital Audio

Preliminary

Overview

The LC78845Q is a synchronous sample rate converter for digital audio signals.

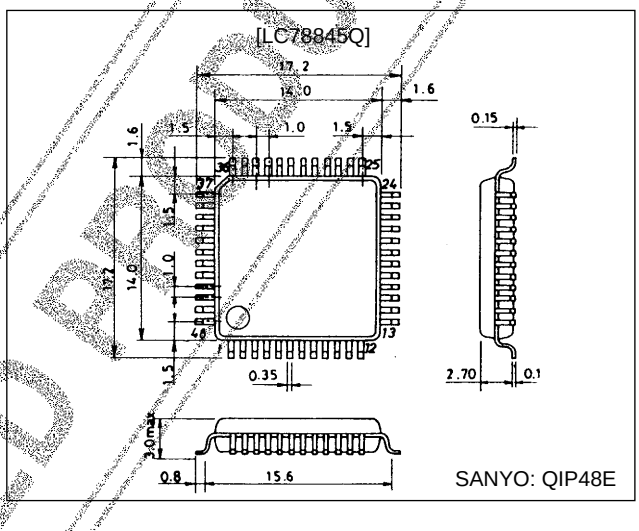
Features

- Converts data sampled at 32 or 48 kHz to 44.1-kHz sampled data.
- Passes 44.1-kHz sampled data trough without change.
- Supports 384fs and 512fs system clock rates.
- 8× oversampling filters
- Soft muting function
- Built-in PLL circuit

Package Dimensions

unit: mm

3156-QFP48E



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
I/O voltages	V_I, V_O		–0.3 to V_{DD} + 0.3	V
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

DC Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
Input voltage range	V_{IN}	Ta = –30 to +70°C	0		V_{DD}	V
Input high-level voltage	V_{IH}		0.7 V_{DD}			V
Input low-level voltage	V_{IL}				0.3 V_{DD}	V
Output high-level voltage	V_{OH}	I_{OH} = –1 µA	V_{DD} – 0.05			V
Output low-level voltage	V_{OL}	I_{OL} = 1 µA			V_{SS} + 0.05	V

This LSI can easily use CCB that is SANYO's original bus format.

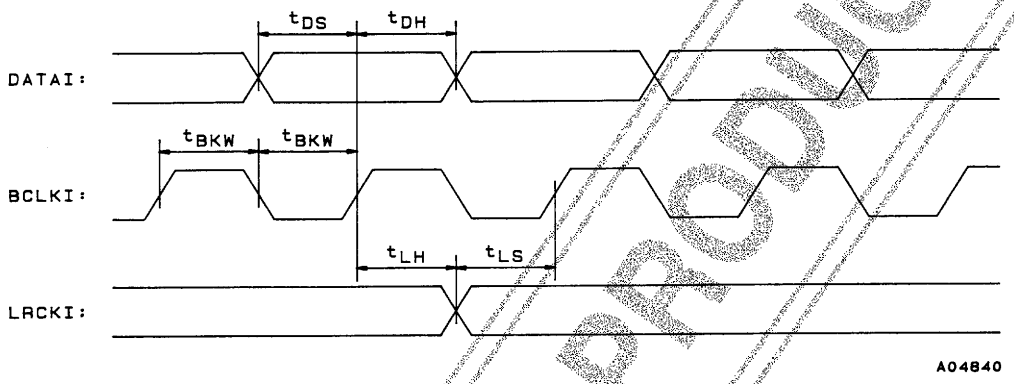
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-0005 JAPAN

AC Characteristics

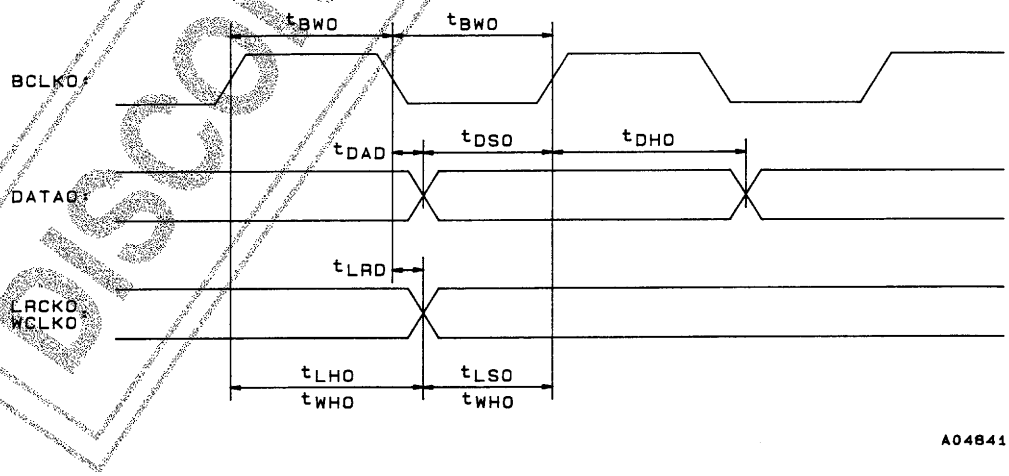
1. Audio data input

Parameter	Symbol	Conditions	min	typ	max	Unit
BCLKI pulse width	t_{BKW}		50			ns
DATAI setup time	t_{DS}		20			ns
DATAI hold time	t_{DH}		20			ns
LRCKI hold time	t_{LH}		25			ns
LRCKI setup time	t_{LS}		25			ns



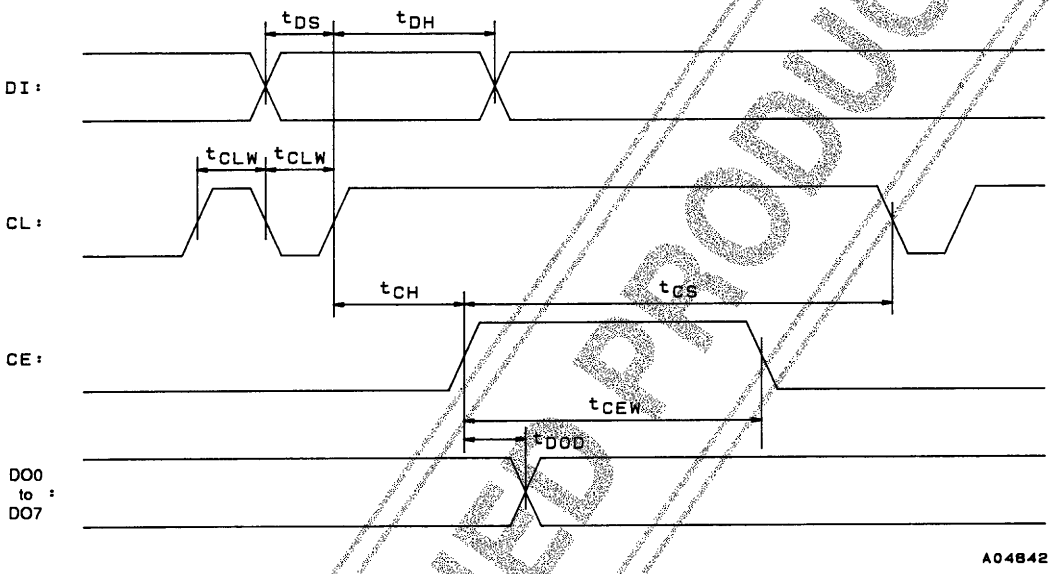
2. Audio data output

Parameter	Symbol	Conditions	min	typ	max	Unit
BCLKO pulse width	t_{BWO}		100			ns
DATAO output delay time	t_{DAD}				25	ns
DATAO setup time	t_{DSO}		50			ns
DATAO hold time	t_{DHO}		50			ns
LRCKO output delay time	t_{LRD}				25	ns
LRCKO setup time	t_{LSO}		50			ns
LRCKO hold time	t_{LHO}		50			ns
WCLKO setup time	t_{WSO}		50			ns
WCLKO hold time	t_{WHO}		50			ns



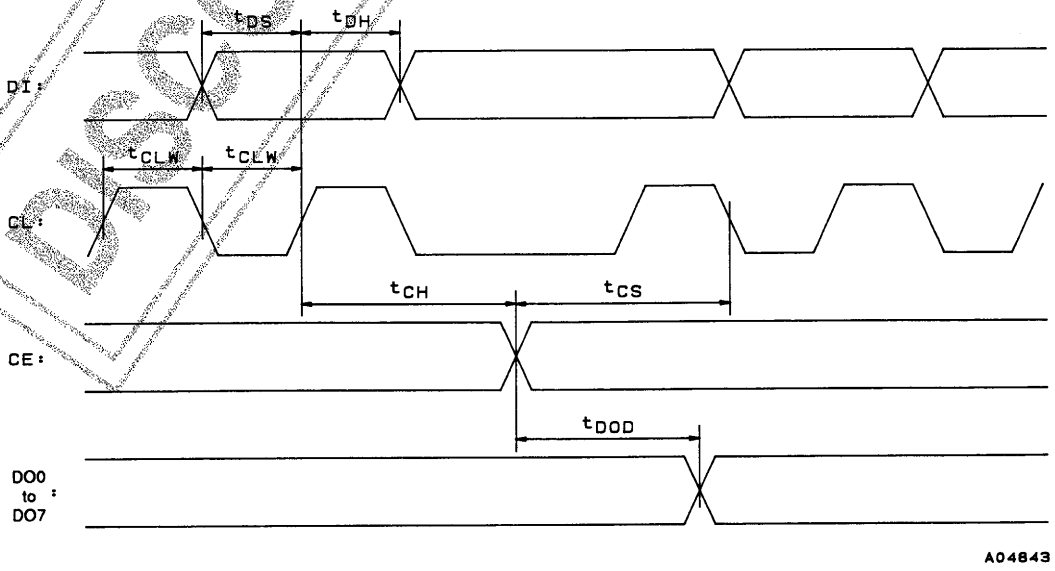
3. Serial input (CCB = low)

Parameter	Symbol	Conditions	min	typ	max	Unit
CL pulse width	t_{CLW}		50			ns
DI setup time	t_{DS}		20			ns
DI hold time	t_{DH}		20			ns
CE pulse width	t_{CEW}		50			ns
CE setup time	t_{CS}		20			ns
CE hold time	t_{CH}		20			ns
DO0 to DO7 output delay time	t_{DOD}				25	ns

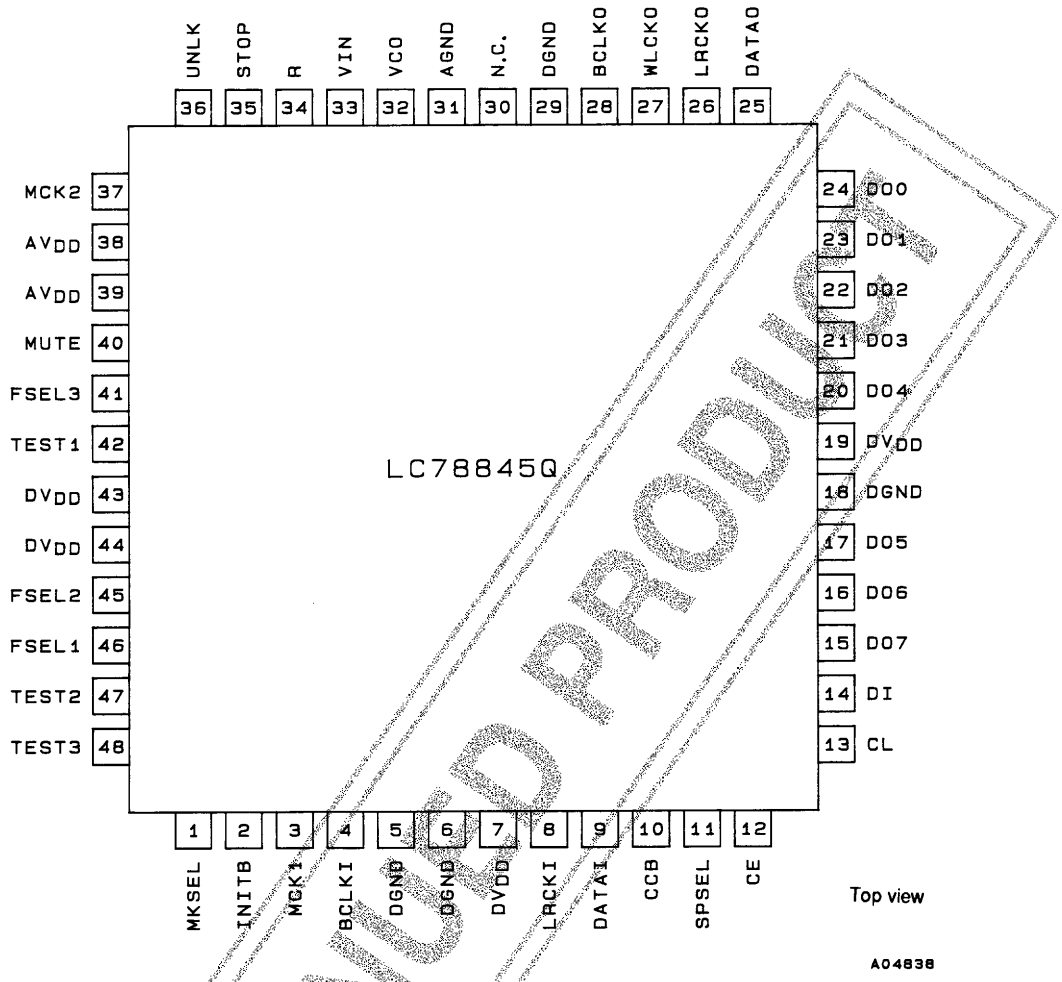


4. Serial input (CCB = high)

Parameter	Symbol	Conditions	min	typ	max	Unit
CL pulse width	t_{CLW}		50			ns
DI setup time	t_{DS}		20			ns
DI hold time	t_{DH}		20			ns
CE setup time	t_{CS}		20			ns
CE hold time	t_{CH}		20			ns
DO0 to DO7 output delay time with respect to the rise of CE	t_{DOD}				25	ns



Pin Assignment



Although the DV_{DD} and AV_{DD} pins in this IC are given different names to correspond to the internal circuit structure, they are connected internally through the circuit substrate. As a result, if different voltages are applied to these pins, abnormal currents will flow in the chip. Since this can cause latchup, power supplies with identical voltages and identical power-on timings must be used.

Pin Functions

Pin No.	Symbol	Overview	Function
1	MKSEL	DF master clock selection	Low: 384fs, high: 512fs
2	INITB	Reset input	Low: initialization operation
3	MCK1	DF master clock input	
4	BCLKI	Audio signal input	Audio signal bit clock input pin
5	DGND	Digital system ground	
6	DGND	Digital system ground	
7	DV_{DD}	Digital system power supply	
8 9	LRCKI DATAI	Audio signal input	Audio signal left/right clock and data input pins
10	CCB	Serial input format specification	Selects the input format for data from the microprocessor input pins.
11	SPSEL	Serial/parallel control	Allows certain of the setting pins to be set from serial data over the microprocessor interface. Low: serial, high: parallel (states set by input pins)

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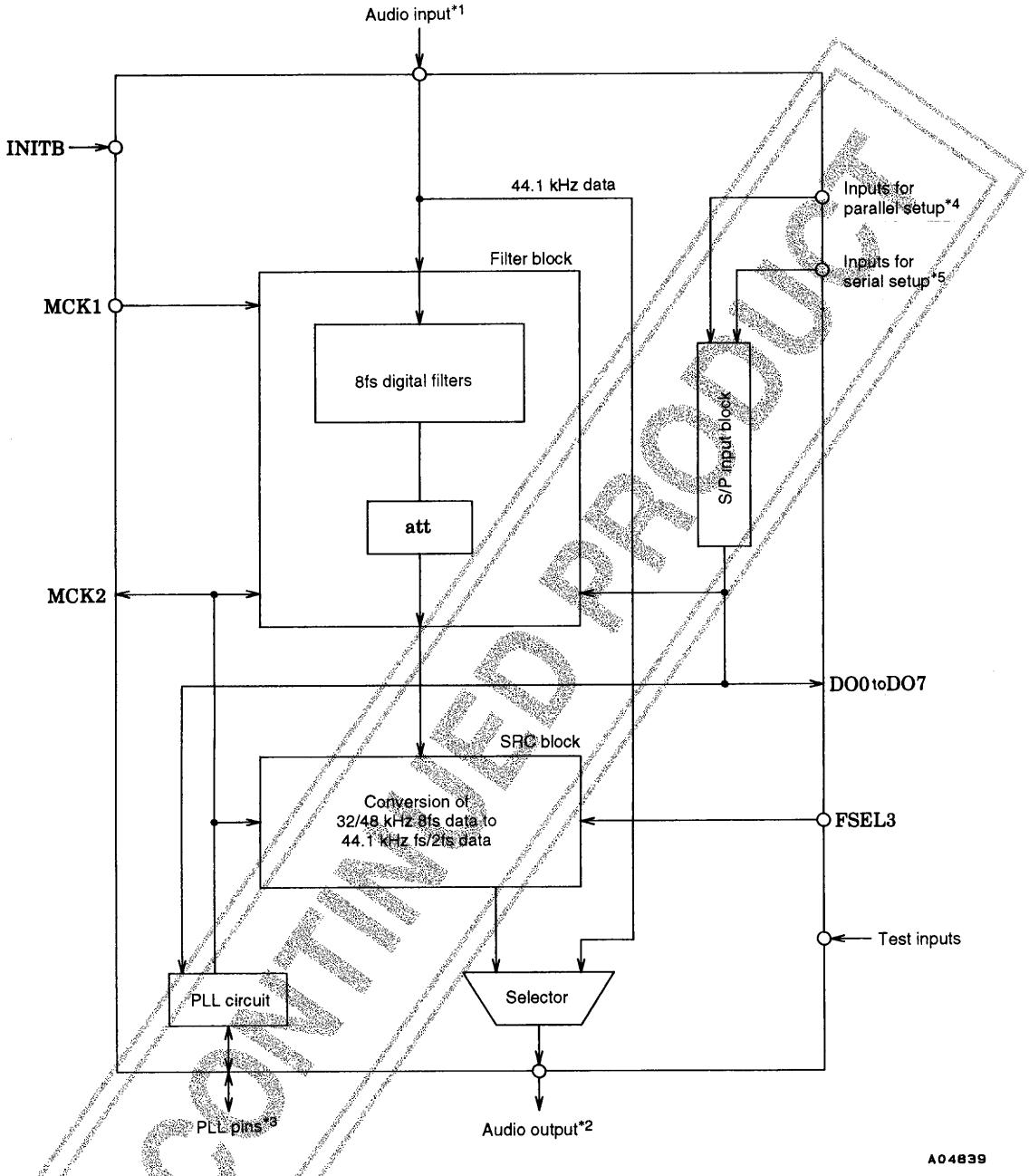
Pin No.	Symbol	Overview	Function
12	CE	Microprocessor input pins	Data enable signal input
13	CL		Shift clock input
14	DI		Address/data input
15	DO7	Parallel data output	Output of 8-bit parallel data according to microprocessor input
16	DO6		
17	DO5		
18	DGND	Digital system ground	
19	DV_{DD}	Digital system power supply	
20	DO4	Parallel data output	Output of 8-bit parallel data according to microprocessor input
21	DO3		
22	DO2		
23	DO1		
24	DO0		
25	DATAO	Audio signal output	Audio signal outputs (data, left/right clock, word clock, and bit clock)
26	LRCKO		
27	WCLKO		
28	BCLKO		
29	DGND	Digital system ground	
30	N.C	—	
31	AGND	Analog system ground	
32	VCO	PLL control	Low-pass filter connection
33	VIN	PLL control	Free-running setting
34	R	PLL control	VCO band adjustment
35	STOP	Oscillator stop signal input	Low: oscillator stopped, high: PLL running
36	UNLK	Unlock detection output	Outputs a high level when the PLL circuit is unlocked.
37	MCK2	Synchronization clock output	Outputs the clock generated by the VCO.
38	AV_{DD}	Analog system power supply	
39	AV_{DD}	Analog system power supply	
40	MUTE	Muting	Low: muting off, high: muting on
41	FSEL3	Output data fs selection	Low: fs data, high: 2fs data
42	TEST1	Test pin	Must be held low during normal operation.
43	DV_{DD}	Digital system power supply	
44	DV_{DD}	Digital system power supply	
45	FSEL2	Input signal fs selection	Selects the fs for the input signal.
46	FSEL1		
47	TEST2	Test pins	Must be held low during normal operation.
48	TEST3		

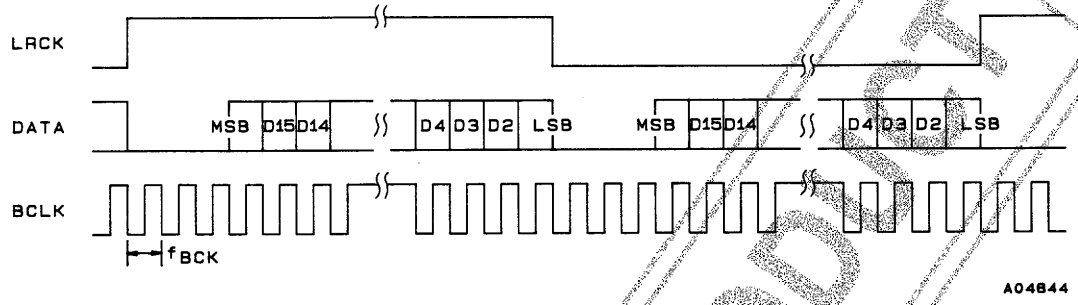
Block Diagram



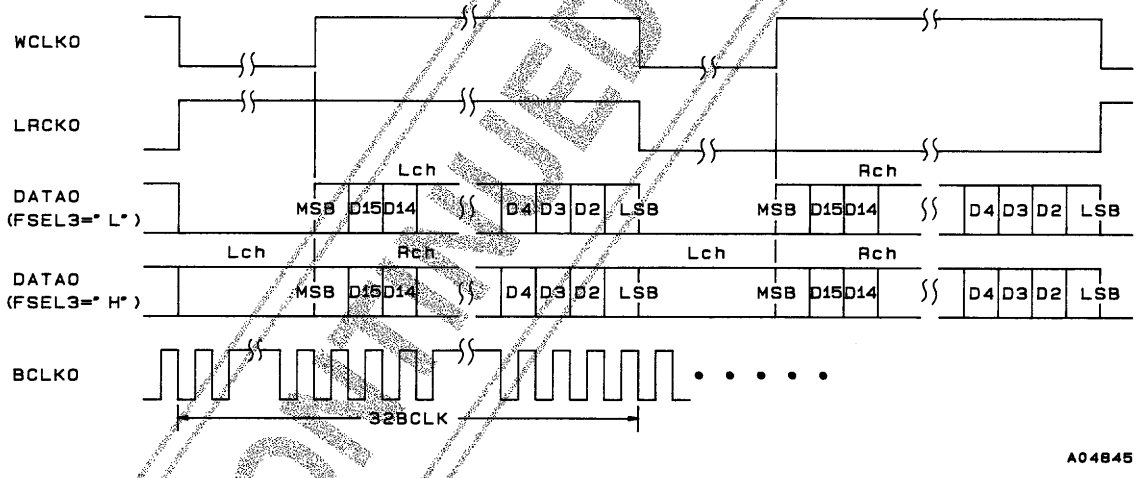
Note: 1. BCLKI, LRCKI, DATAI
2. BCLKO, LRCKO, DATAO, WCLKO
3. R, VIN, VCO, UNLK
4. MKSEL, FSEL1, FSEL2, MUTE, STOP
5. CCB, SPSEL, CE, CL, DI

Input and Output Formats

1. Input format
   Audio data is input through the audio data input pins (BCLKI, LRCKI, and DATAI) in the following format.
   MKSEL = L: f_{BCK} = 48fs
   MKSEL = H: f_{BCK} = 64fs



2. Output format 1
   Audio data is output through the audio data output pins (BCLKO, WCLKO, LRCKO, and DATAO) in the following format.
   BCLKO = 64fs (fixed)
   LRCKO = fs (fixed)
   WCLKO = 2fs (fixed)



3. Output format 2 (When the input fs is 44.1 kHz)
   When data sampled at 44.1 kHz is input, that data is output directly without change. The WCLKO output is held low in this case.

Pin Settings

1. Input master clock setup (when SPSEL is high)
   Input the master clock for the internal digital filters to MCK1 (pin 3). Also, set whether that clock is 384fs or 512fs with MKSEL (pin 1).

Pin	L	H
MKSEL	384fs	512fs

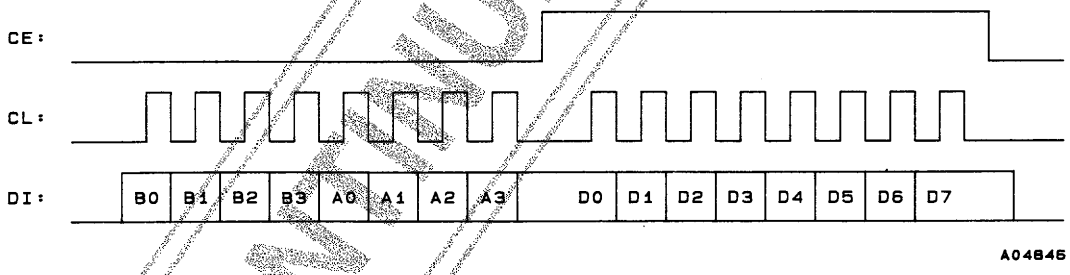
2. Input data fs setting (when SPSEL is high)
   The input data sampling frequency must be set. FSEL1 and FSEL2 (pins 46 and 45) are used for this setting. Data sampled at a 32 or 48 kHz sampling frequency is converted to data with a 44.1 kHz sampling frequency. If data sampled at 44.1 kHz is input, it is passed through unchanged.

Sampling frequency	FSEL1	FSEL2
44.1 kHz	0	×
48 kHz	1	0
32 kHz	1	1

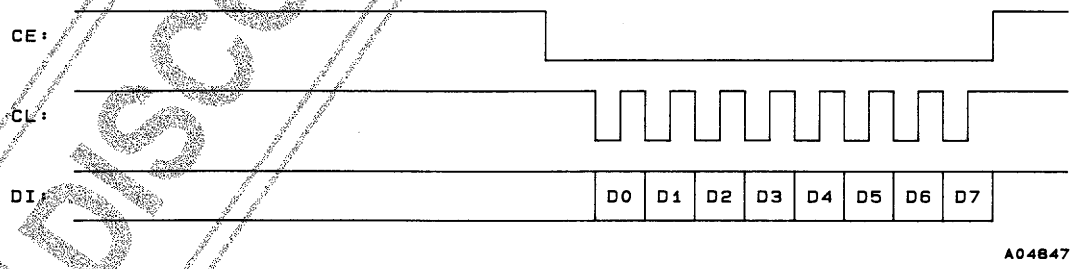
3. Output data setup
   The output data can be switched between fs and 2fs. FSEL3 (pin 41) is used to change this setting.

Pin	L	H
FSEL3	fs	2fs

4. Setup from serial input
   The MKSEL, FSEL1, FSEL2, MUTE, and STOP settings can be set using the serial bus by setting SPSEL (pin 11) low. The 8 bits of input data is output in parallel regardless of the SPSEL setting.



Serial input format 1 (CCB = high)



Serial input format 2 (CCB = low)

Data	INITB = H SPSEL = L	INITB = L
B0 to B3 A0 to A3	LSI selection Address	— —
D0 D1 D2 D3 D4 D5 to D7	MKSEL FSEL1 FSEL2 MUTE STOP —	L L L H L H

Address

LSB MSB

B0	B1	B2	B3	A0	A1	A2	A3
0	0	1	0	0	1	1	1

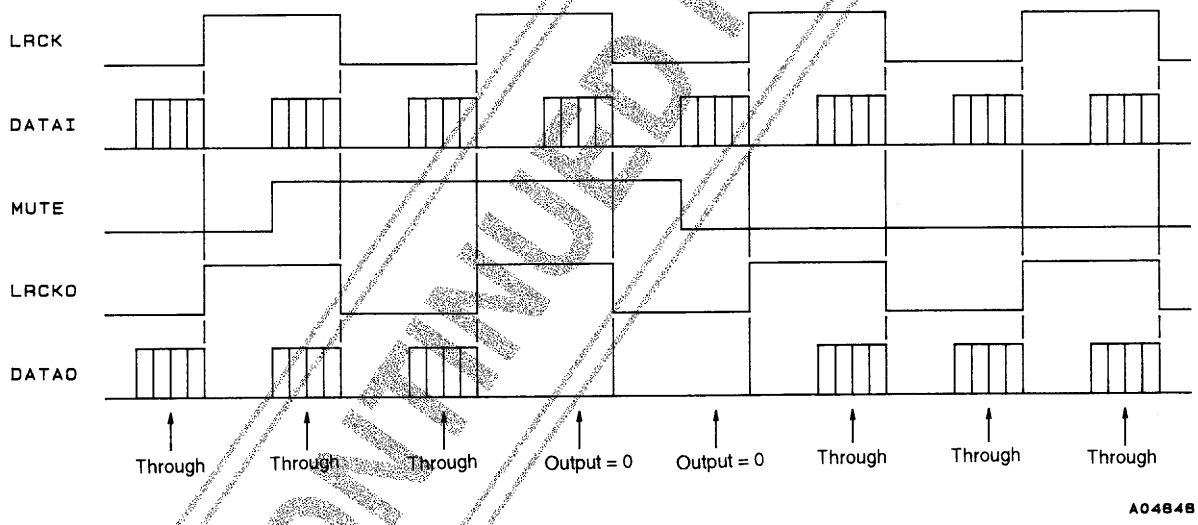
HEX : E4

The data and the signals correspond as listed in the tables. Since the external pins (MKSEL etc.) set by the serial input are unused, applications must assure that these pins do not become floating. If initialization is performed, set the initial values listed in the table.

5. Muting

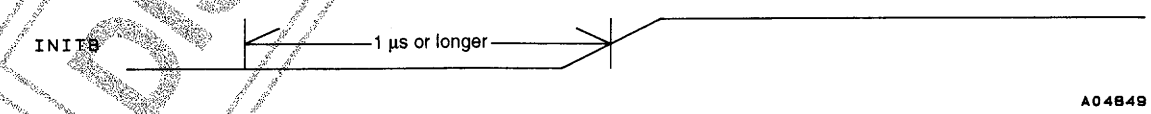
A soft muting function is applied to the data if the MUTE pin (pin 40) is set high when data with a 32 or 48 kHz sampling frequency is input. The input signal values are gradually attenuated so that the data reaches –∞ 1024/fs (seconds) later. When the soft muting function is turned off, the amplitude becomes the same as that of the input 1024/fs (seconds) later.

For input data with a 44.1 sampling frequency, the data is forcibly set to 0 on the next rising edge of the LRCK signal after the MUTE signal goes from low to high. Similarly, data is output on the next rising edge of the LRCK signal after the MUTE signal goes from high to low.



6. Initialization

When power is first applied, the LSI must be initialized when the pin settings are changed. Initialization is performed by holding INITB (pin 2) low for at least 1 µs in the state where the MCK1 signal is input after the power supply voltage has stabilized.



7. PLL block

The PLL block generates a 14.112 MHz master clock (MCK2) that is used for all three frequencies; 32, 44.1, and 48 kHz, when either 32 or 48 kHz is specified as the input data sampling frequency.

• STOP pin setting

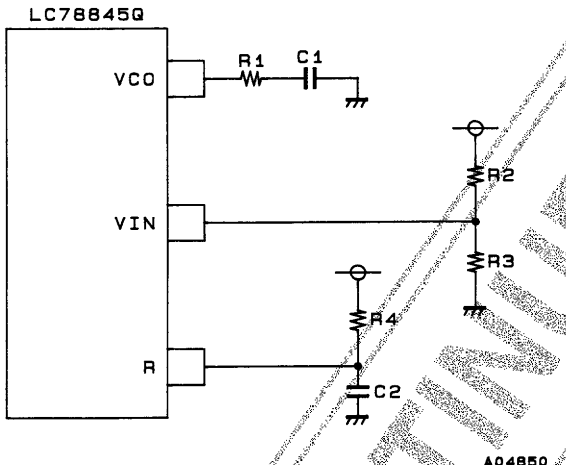
STOP	Function
L	The VCO is stopped.
H	The VCO operates.

• UNLK pin

UNLK	Function
L	Indicates that the PLL circuit is locked.
H	Indicates that the PLL circuit is in the unlocked state.

The UNLK pin is high during unlocked periods and during the 1024/fs (seconds) required for the unlocked to locked transition. The LSI performs the same processing during the locked to unlocked transition as it does when MUTE is high.

• External circuits



Symbol	Value	Unit
R1	150	Ω
R2	5.1 k	
R3	5.1 k	
R4	24 k	
C1	0.02	µF
C2	0.1	