



## LC75382E

### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

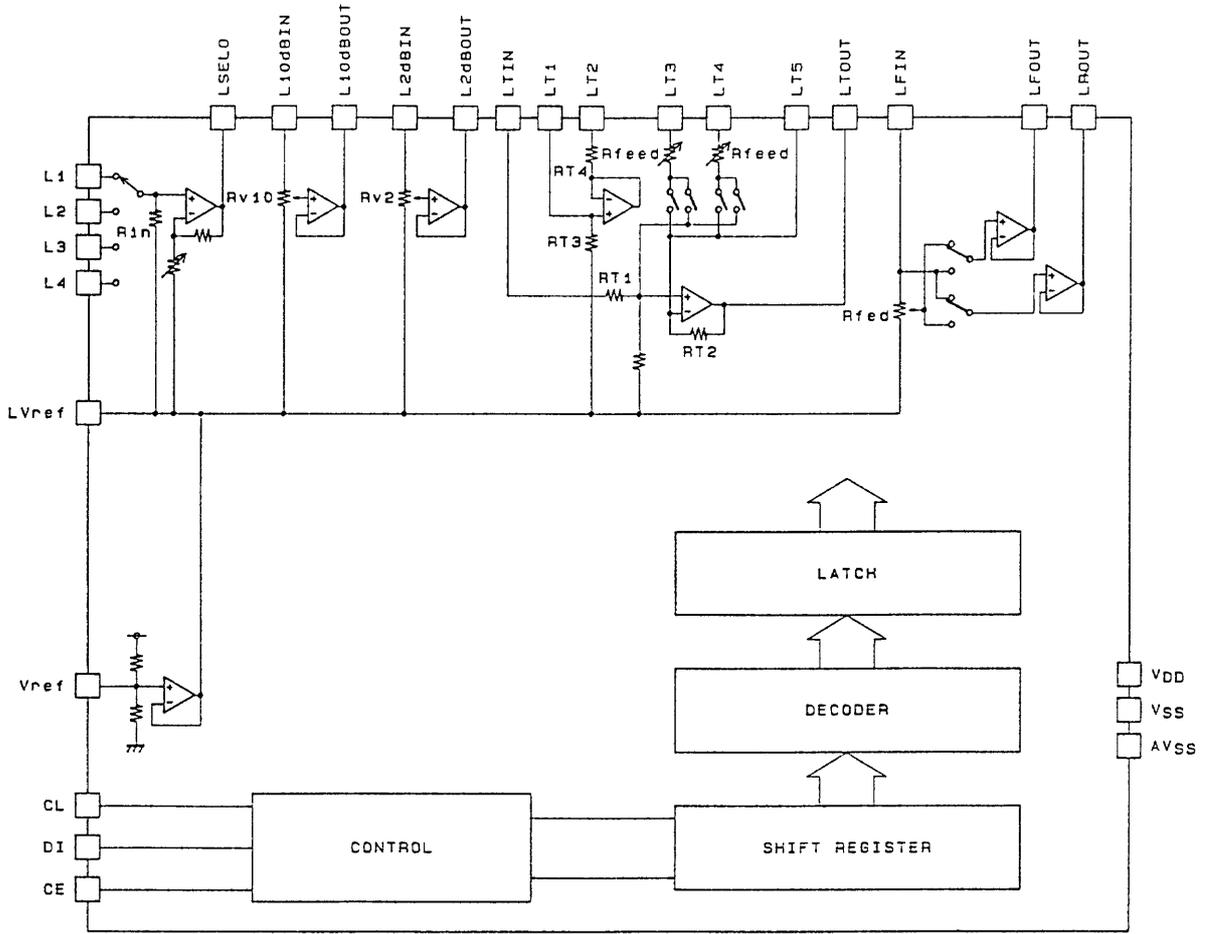
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}$	$V_{DD}$	6.0		11.0	V
Input high level voltage	$V_{IH}$	CL, DI, CE	4.0		$V_{DD}$	V
Input low level voltage	$V_{IL}$	CL, DI, CE	$V_{SS}$		1.0	V
Input voltage amplitude	$V_{IN}$	LTIN, RTIN, L10dBIN, R10dBIN, L2dBIN, R2dBIN, LFIN, RFIN, L1 to L4, R1 to R4	$V_{SS}$		$V_{DD}$	Vp-p
Input pulse width	$t_{\phi W}$	CL	1			$\mu\text{s}$
Setup time	$t_{\text{setup}}$	CL, DI, CE	1			$\mu\text{s}$
Hold time	$t_{\text{hold}}$	CL, DI, CE	1			$\mu\text{s}$
Operating frequency	fopg	CL			500	kHz

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 9\text{ V}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
[Input Block]						
Input resistance	$R_{in}$	L1 to L4, R1 to R4		1		$\text{M}\Omega$
Clipping level	$V_{cl}$	LSELO, RSELO: THD = 1.0%		2.35		Vrms
Output load resistance	$R_L$	LSELO, RSELO	10			$\text{k}\Omega$
Minimum input gain	$G_{in\ min}$		-2	0	+2	dB
Maximum input gain	$G_{in\ max}$		+16.0	+18.0	+20.0	dB
Step resolution	$G_{step}$			+6.0		dB
[Volume Block]						
Input resistance	$R_{v10}$	L10dBIN, R10dBIN: 10 dB steps	21	35	49	$\text{k}\Omega$
	$R_{v2}$	L2dBIN, R2dBIN: 2 dB steps	6	10	14	$\text{k}\Omega$
Step resolution	$\Delta T_{step}$			2		dB
Step error	$\Delta T_{err}$	step = 0 to -40 dB	-2	0	+2	dB
[Fader Volume Block]						
Input resistance	$R_{fed}$	LFIN, RFIN	12	20	28	$\text{k}\Omega$
Step resolution	$\Delta T_{step}$	step = 0 to -20 dB		2		dB
		step = -20 to -25 dB		5		dB
		step = -25 to -45 dB		10		dB
Step error	$\Delta T_{err}$	step = 0 to -40 dB, step = -40 to -60 dB	-2	0	+2	dB
Output load resistance	$R_L$	LFOUT, LROUT, RFOUT, RROUT	10			$\text{k}\Omega$
[Bass/Treble Control Block]						
Control range	$G_{bass}, G_{tre}$	Max. Boost/Cut	$\pm 15$	$\pm 17$	$\pm 19$	dB
Step resolution	$B_{step}$		0.7	1.7	2.7	dB
Internal feedback resistance	$R_{feed}$		46	76	107	$\text{k}\Omega$
[Overall Characteristics]						
Total harmonic distortion	THD (1)	$V_{IN} = 300\text{ mVrms}$ , $f = 1\text{ kHz}$ , all controls flat overall		0.005	0.01	%
	THD (2)	$V_{IN} = 300\text{ mVrms}$ , $f = 20\text{ kHz}$ , all controls flat overall		0.008	0.02	%
Crosstalk	CT	$V_{IN} = 1\text{ Vrms}$ , $f = 1\text{ kHz}$ , all controls flat overall, $R_g = 1\text{ k}\Omega$	60	84.5		dB
Output at maximum attenuation	$V_O\ min$	$V_{IN} = 1\text{ Vrms}$ , $f = 1\text{ kHz}$ , Main volume at $-\infty$	-65	-74.5		dB
Output noise voltage	$V_N$ (1)	All controls flat overall (IHF-A), $R_g = 1\text{ k}\Omega$		5.2	12	$\mu\text{V}$
	$V_N$ (2)	All controls flat overall (DIN-AUDIO), $R_g = 1\text{ k}\Omega$		7.2	16	$\mu\text{V}$
	$V_N$ (3)	All controls flat overall (NO-FILTER), $R_g = 1\text{ k}\Omega$		9.2	20	$\mu\text{V}$
	$V_N$ (4)	$G_v = +18\text{ dB}$ (IHF-A), $R_g = 1\text{ k}\Omega$		23	50	$\mu\text{V}$
	$V_N$ (5)	Bass at maximum boost, treble at maximum boost (IHF-A), $R_g = 1\text{ k}\Omega$		48	120	$\mu\text{V}$
Current drain	$I_{DD}$	$V_{DD} - V_{SS} = 11\text{ V}$		28	33	mA
Input high level current	$I_{IH}$	CL, DI, CE: $V_{IN} = 9\text{ V}$			10	$\mu\text{A}$
Input low level current	$I_{IL}$	CL, DI, CE: $V_{IN} = 0\text{ V}$	-10			$\mu\text{A}$

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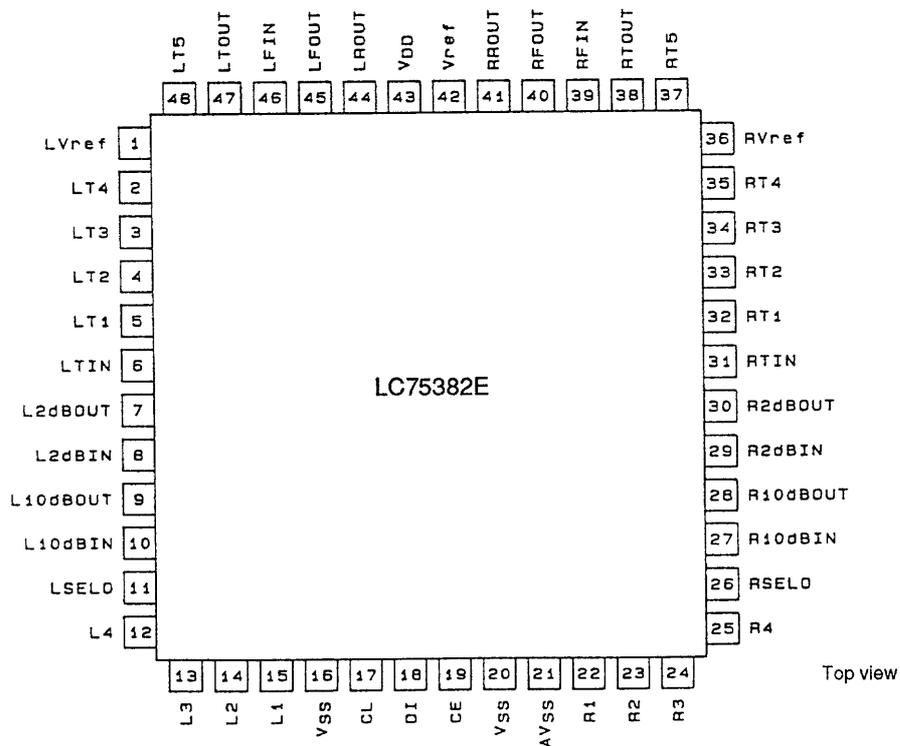
## Equivalent Circuit Block Diagram



Note: The right channel is identical.

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## Pin Assignment

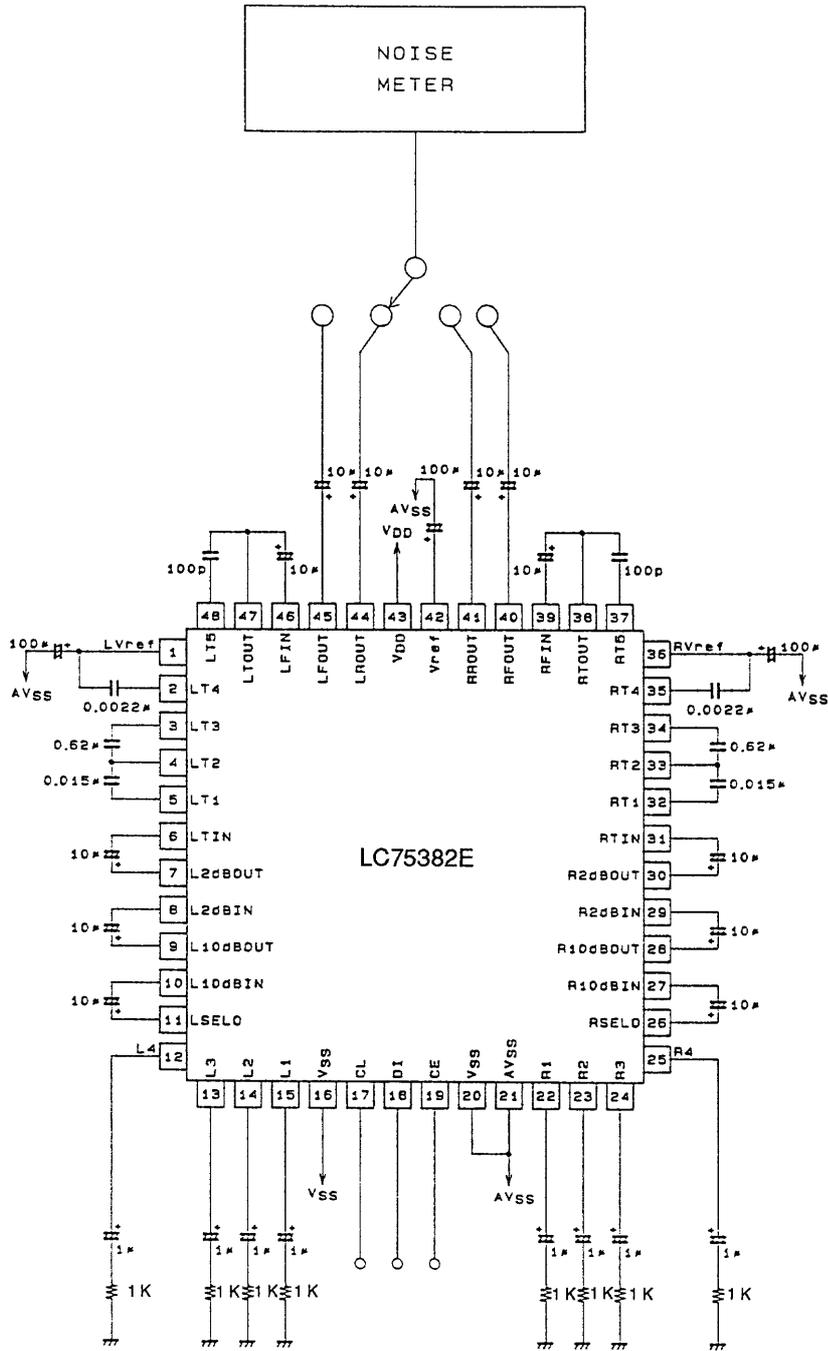


Top view



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## 2. Output noise voltage

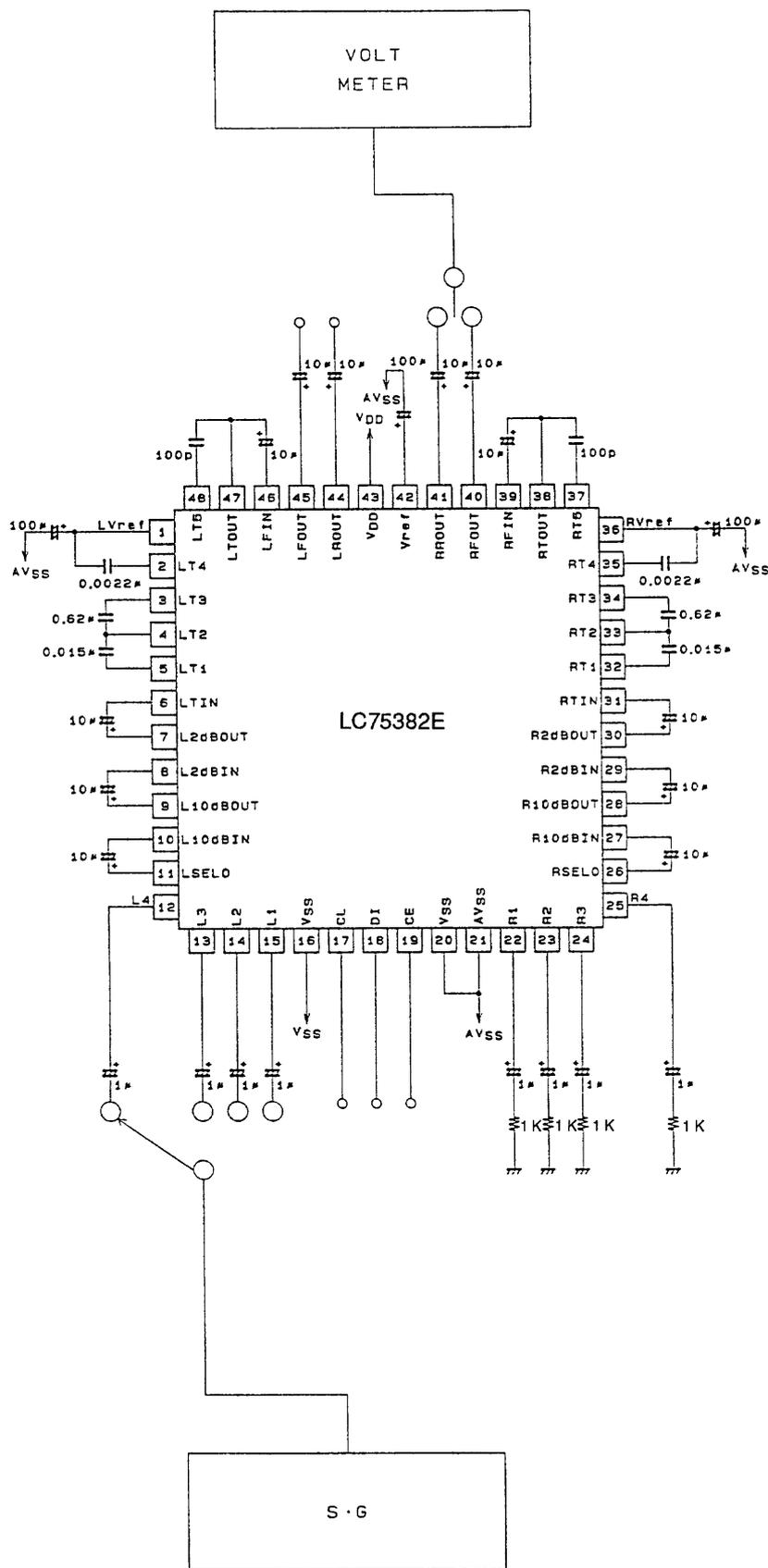


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Unit (resistance: Ω, capacitance: F)

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## 3. Crosstalk



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Unit (resistance: Ω, capacitance: F)

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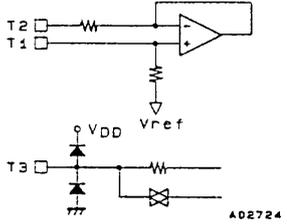
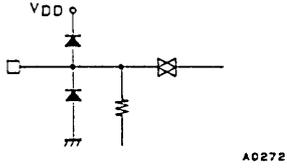
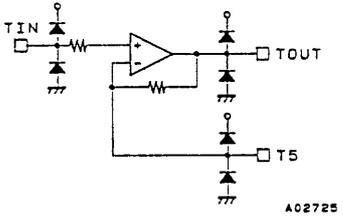
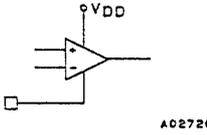
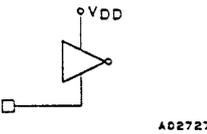
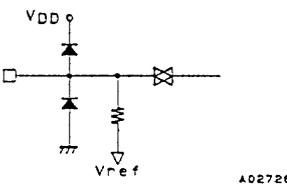
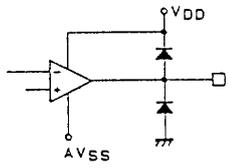
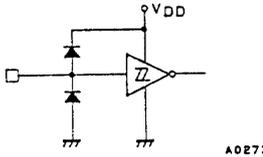
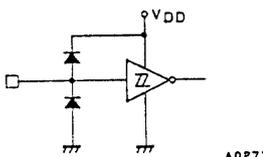
### Pin Functions

Pin No.	Symbol	Function	Note
44 45 41 40	LROUT LFOUT RROUT RFOUT	Fader block output. Attenuates only the front or rear outputs. The left/right attenuation is identical. These are op amp outputs and thus are low impedance.	
46 39	LFIN RFIN	Fader block input Must be driven by low impedance outputs.	
1 36	LVref RVref	Common pins for the main volume, fader, tone and gain control blocks.	
42	Vref	$V_{DD}/2$ voltage generation block. Connect a capacitor (about 100 $\mu$ F) between Vref and AV <sub>SS</sub> to suppress power supply ripple.	
7 30	L2dBOUT R2dBOUT	Main volume 2 dB step attenuator outputs	
8 29	L2dBIN R2dBIN	Main volume 2 dB step attenuator inputs Must be driven by low impedance outputs	
9 28	L10dBOUT R10dBOUT	Main volume 10 dB step attenuator outputs	
10 27	L10dBIN R10dBIN	Main volume 10 dB step attenuator inputs Must be driven by low impedance outputs.	
47 38	LTOUT RTOUT	Tone control outputs	

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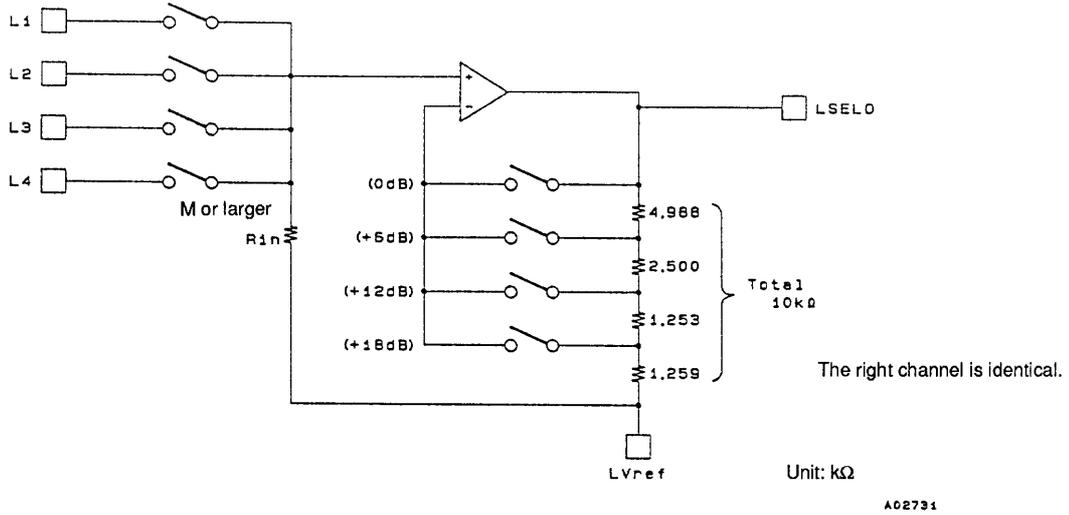
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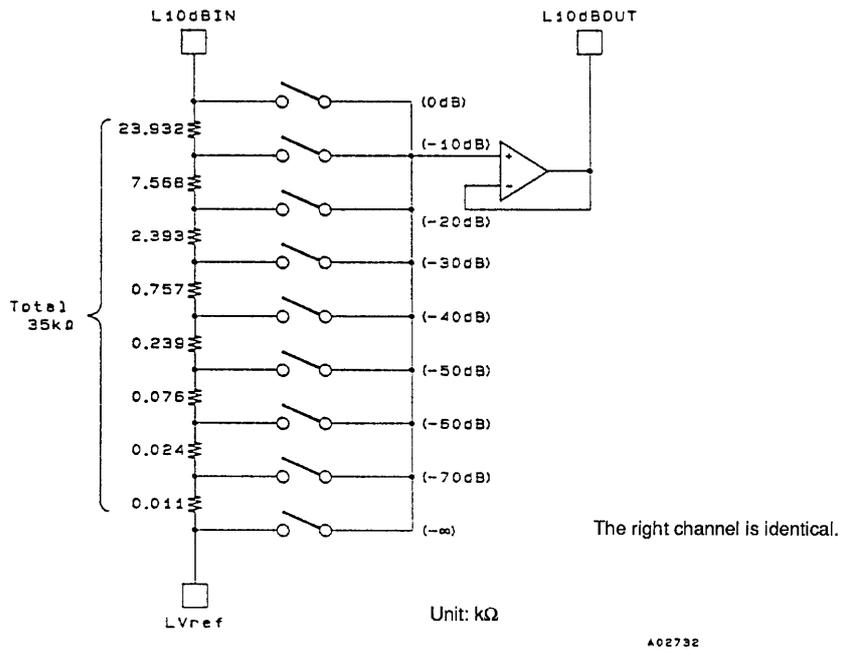
Pin No.	Symbol	Function	Note
5 4 3 32 33 34	LT1 LT2 LT3 RT1 RT2 RT3	Tone circuit low band filter capacitor connections. Connect capacitors between the T1 and T2 pairs and between the T2 and T3 pairs.	 A02724
2 35	LT4 RT4	Tone circuit high band filter capacitor connections. Connect high band compensating capacitors between the T4 pins and Vref.	 A02721
48 37	LT5 RT5	Tone circuit filter op amp inverting inputs Out of band signals can be excluded by connecting capacitors with appropriate values between the T5 and TOUT pairs.	 A02725
6 31	LTIN RTIN	Tone control circuit inputs Must be driven by low impedance outputs.	
43	V <sub>DD</sub>	Power supply	
21	A. V <sub>SS</sub>	Internal op amp ground	 A02726
16, 20	V <sub>SS</sub>	Internal logic system ground	 A02727
15 14 13 12 22 23 24 25	L1 L2 L3 L4 R1 R2 R3 R4	Audio signal inputs	 A02728
11 26	LSELO RSELO	Input selector outputs	 A02729
19	CE	Chip enable. Data is written to the internal latch on the high to low transition of this signal. The analog switches operate at that point. Data transfer is enabled when this signal is high.	 A02730
18 17	DI CL	Serial data and clock connections for IC control.	 A02730

Internal Equivalent Circuit Details

Input Block Equivalent Circuit

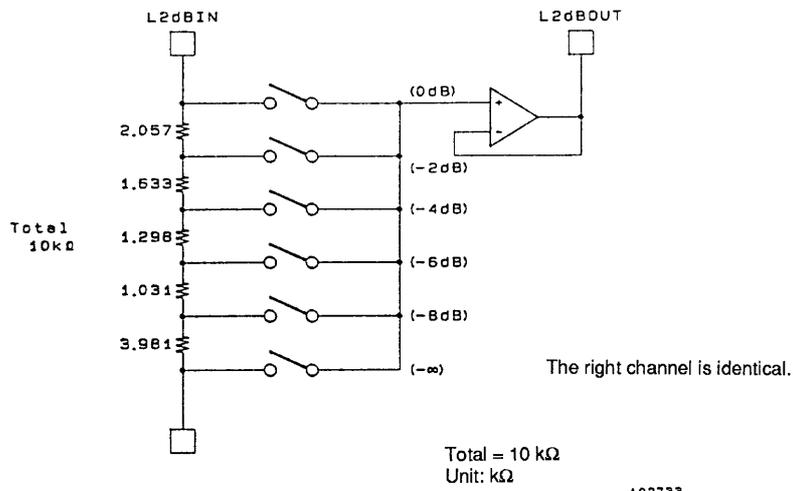


10 dB Step Volume Equivalent Circuit

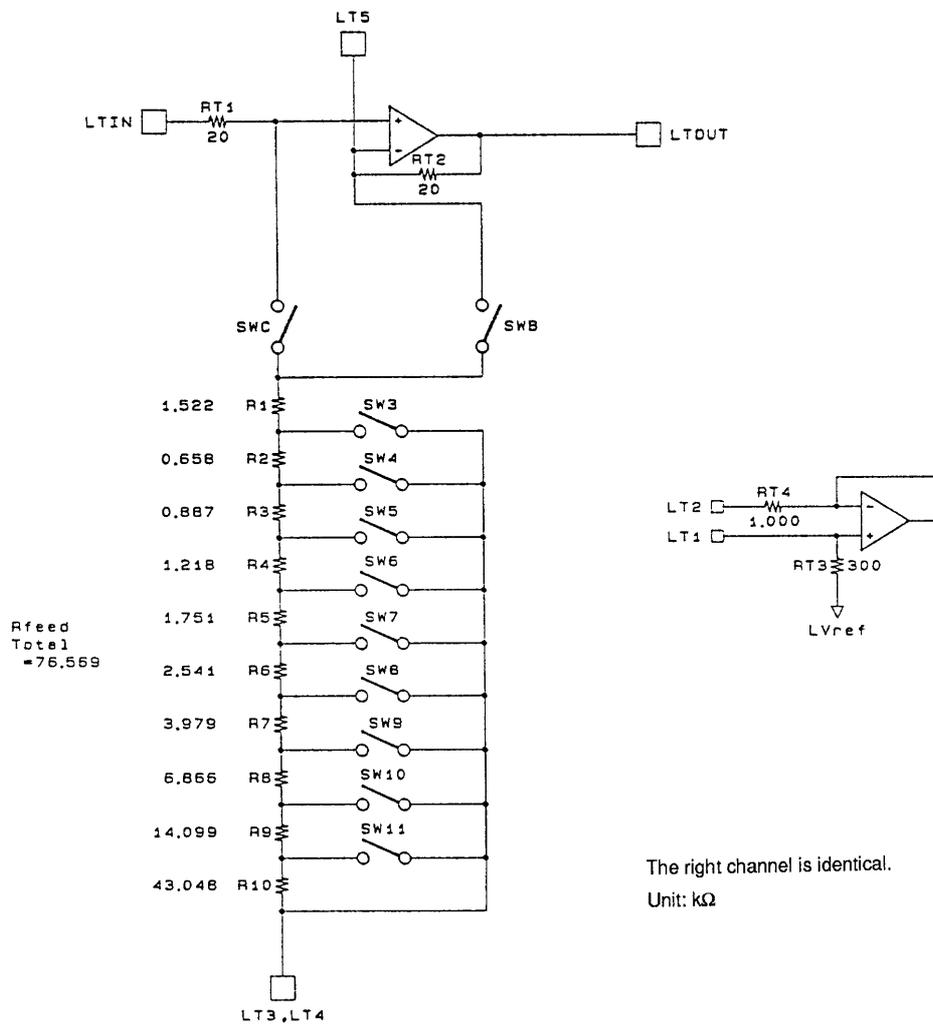


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## 2 dB Step Equivalent Circuit



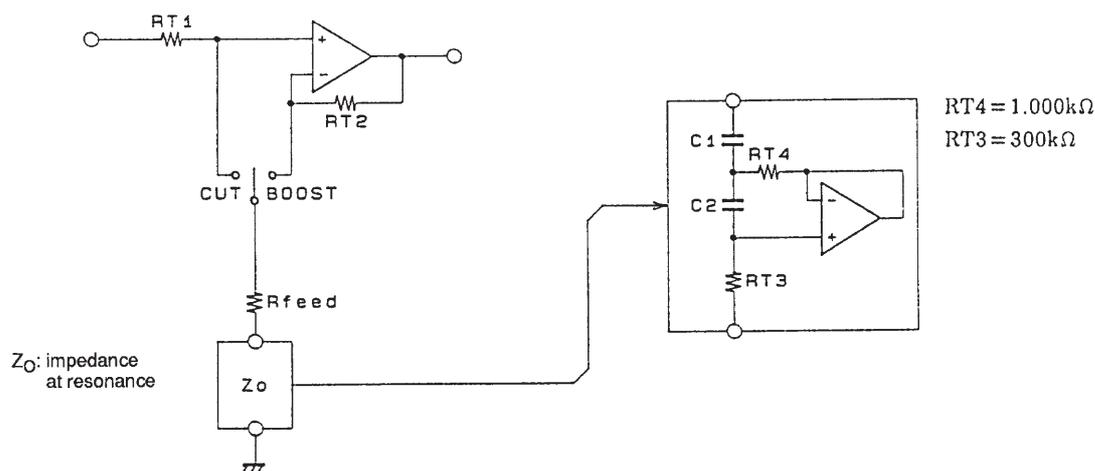
## Tone Block Equivalent Circuit



### Tone Control Circuit External Capacitor Value Calculation Example

The external capacitors used with the LC75382E are structural components of semiconductor inductors (simulated inductors). This section presents the equivalent circuits and formulas for acquiring the desired center frequencies.

#### 1. Semiconductor inductor equivalent circuit



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#### 2. Sample calculation

- Specifications:
1. Center frequency  $F_O = 100$  Hz
  2. Q at maximum boost:  $Q_{max} = 1.05$

① Derive the sharpness of the semiconductor inductor itself,  $Q_O$ .

$$Q_O = \frac{(RT4 + R_{feed})}{RT4} \times Q_{max} = 2.6481$$

② Derive  $C1$ .

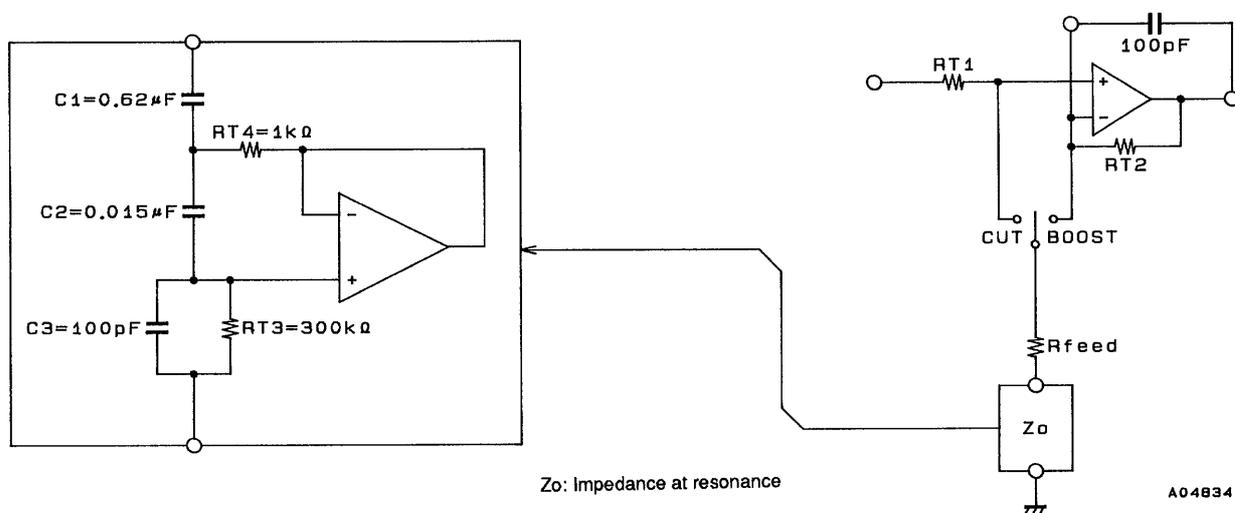
$$C1 = 1/2\pi F_O RT4 Q_O \approx 0.60 (\mu F)$$

③ Derive  $C2$ .

$$C2 = Q_O / 2\pi F_O RT3 \approx 0.014 (\mu F)$$

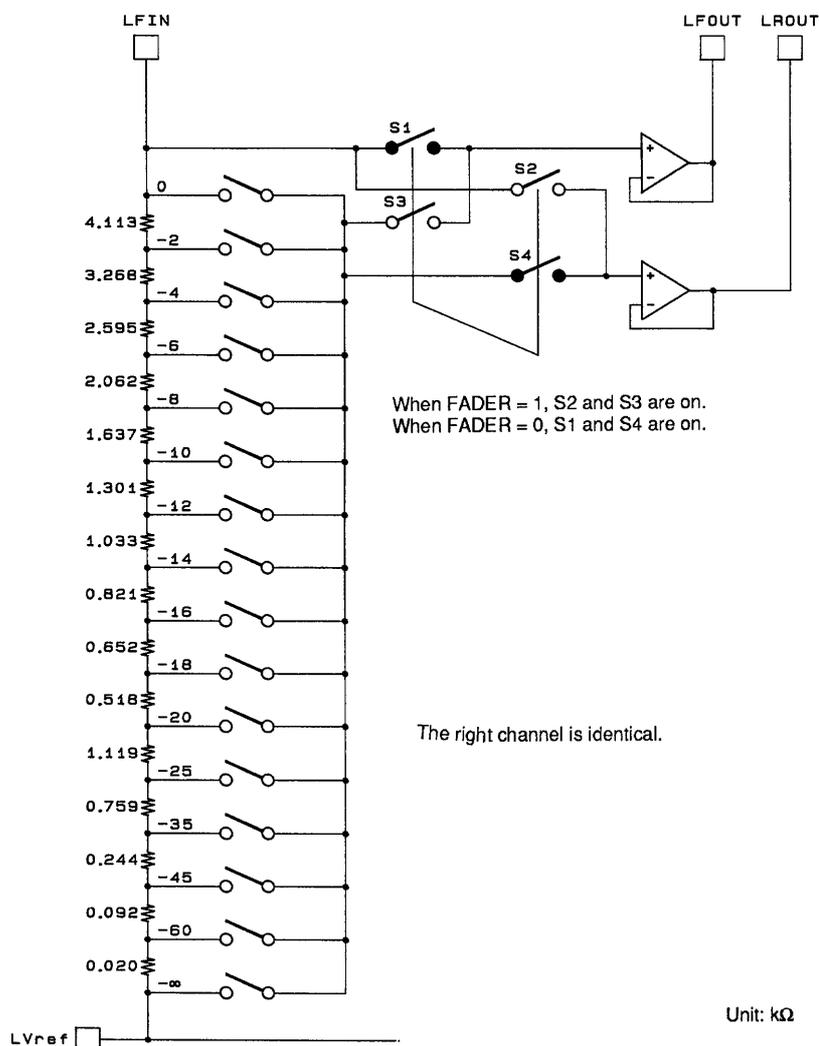
Note: See the tone block equivalent circuit diagram (page 10) for the internal resistance.

Technique for Reducing Noise in the Tone Circuit Output



The output noise can be improved by about 6 dB by providing an external impedance at resonance of  $Z_o$  and adding the capacitor  $C_3$  with a value of about 100 pF. An even larger noise reduction effect can be acquired by using a low noise operational amplifier in the external circuit.

Fader Block Equivalent Circuit

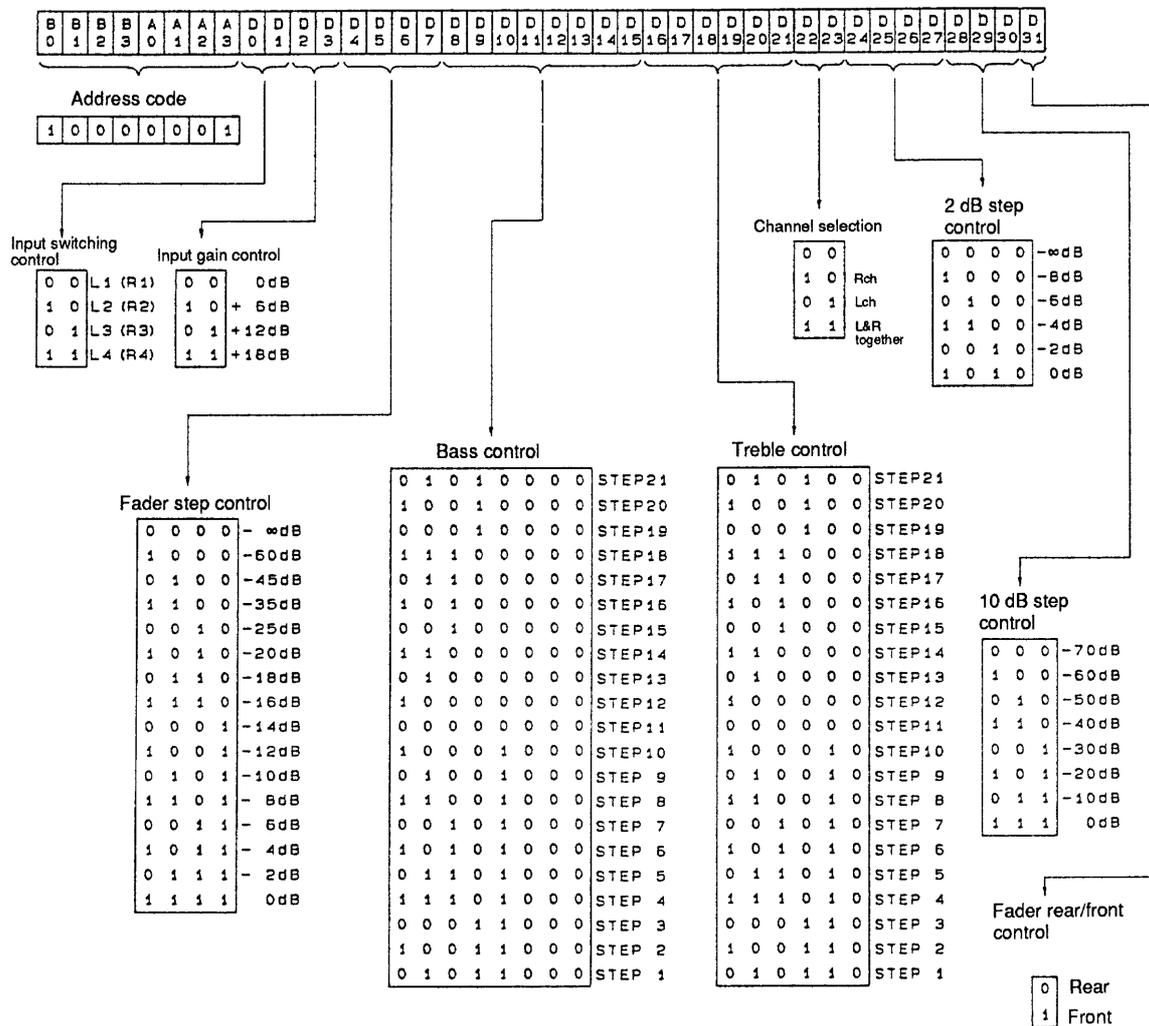
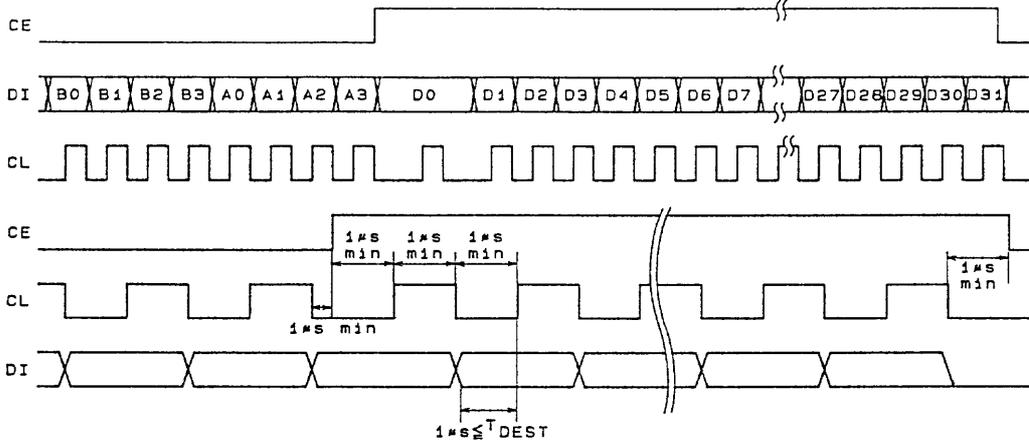


When data specifying a  $-\infty$  attenuation in the 2 dB step main volume is issued, S1 and S2 will open and at the same time, S3 and S4 will turn on.

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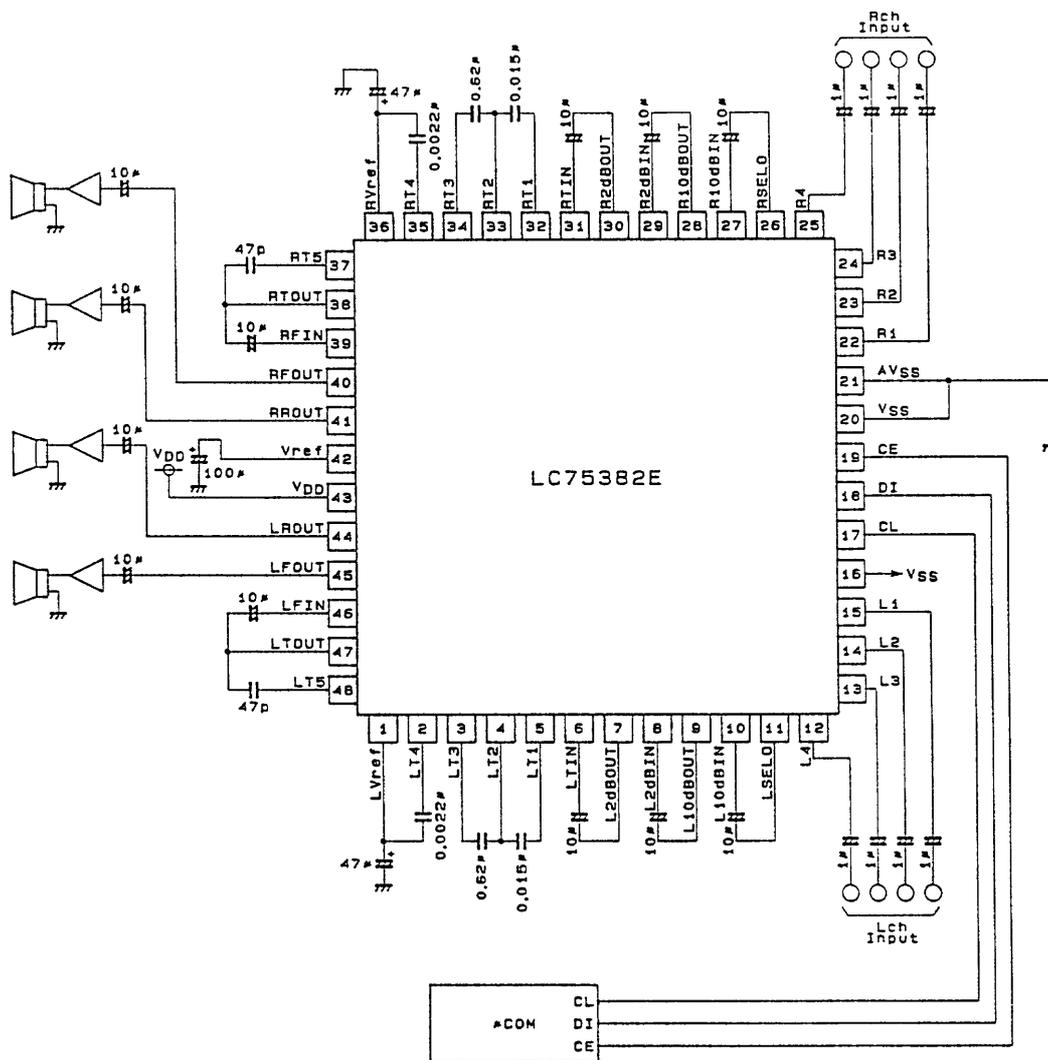
## Control System Timing and Data Format

The prescribed data (signals) must be applied to the CE, CL and DI pins to control the LC75382. The data consists of a total of 40 bits, of which 8 bits are address and 32 bits are the actual control data.



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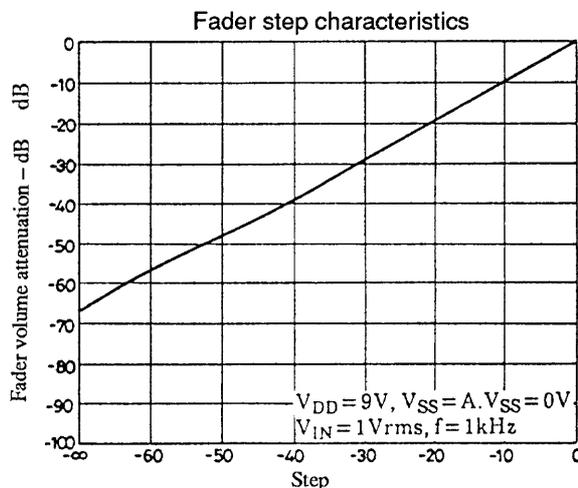
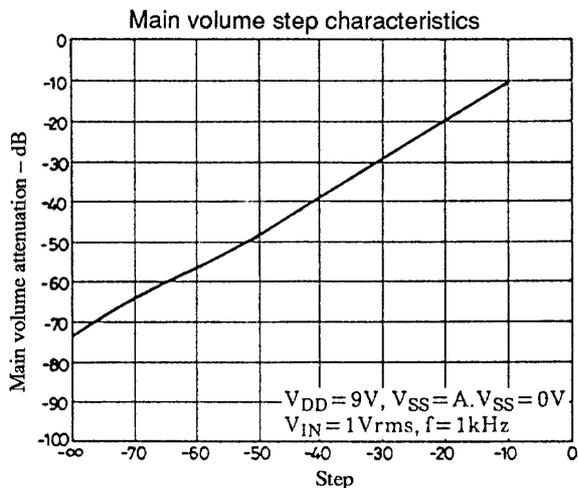
Sample Application Circuit



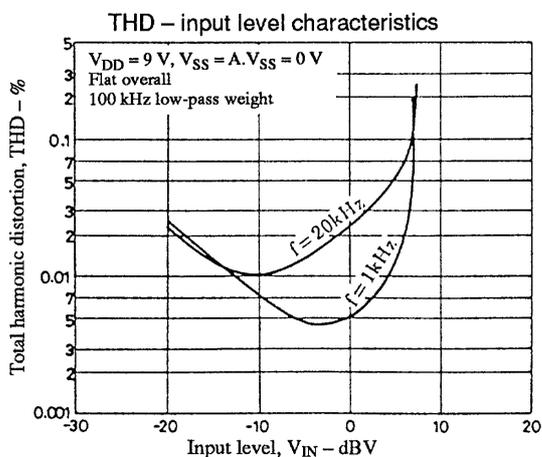
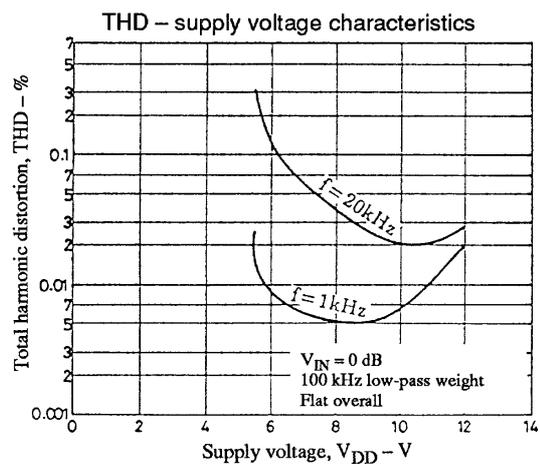
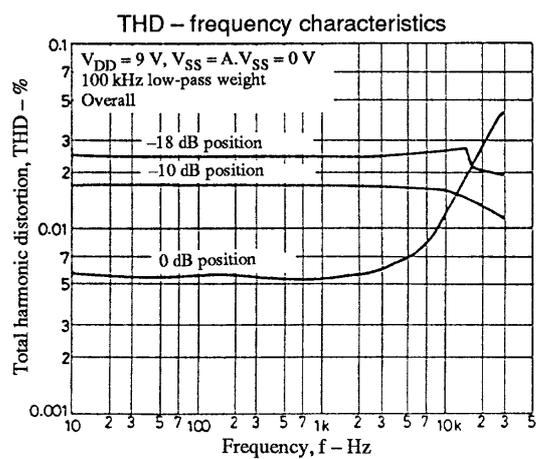
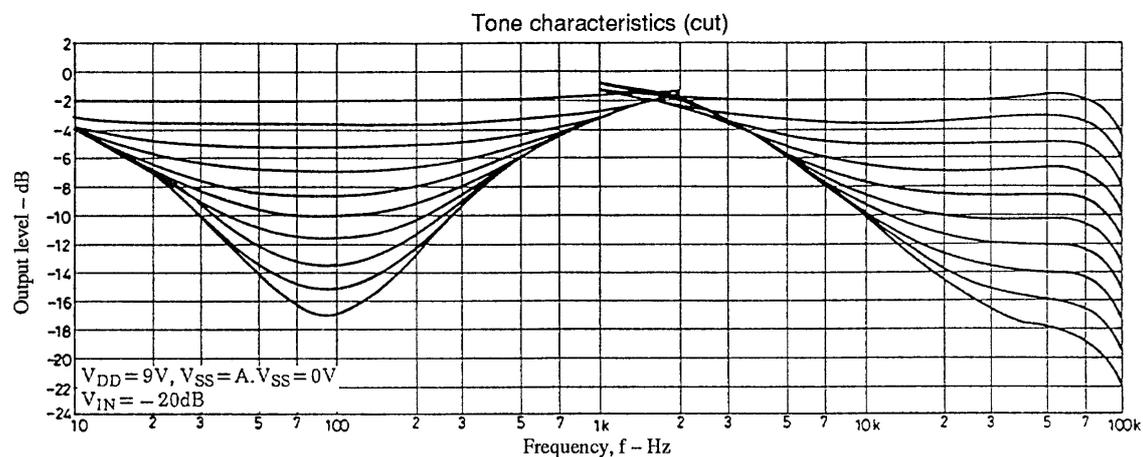
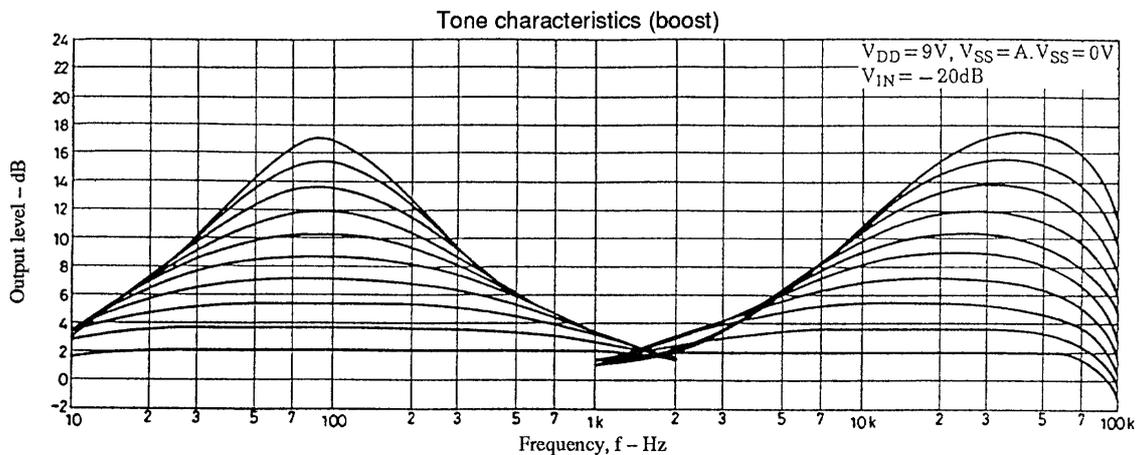
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Usage Notes

1. The states of the internal analog switches are undefined when power is first applied. Muting should be applied externally until data has been transferred.
2. To prevent the high frequency digital signals on the CL, DI and CE pin lines from entering the analog signal system, those lines must be guarded by the ground pattern. Alternatively, shielded cable can be used for those lines.



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