Ordering number : EN4863

CMOS LSI

LC7536R

High Breakdown Voltage Serial Control Electronic Volume Control

Overview

The LC7536R is an electronic volume control IC that implements volume and balance functions with a minimum number of external components.

Features

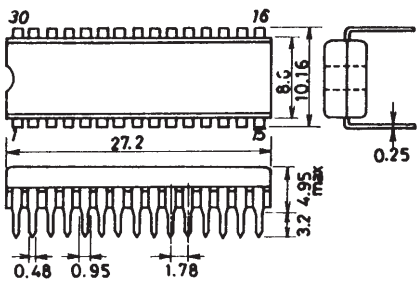
- The LC7536R is controlled by a 3-wire (DI, CL and CE) serial data control scheme that can be shared with other ICs. Up to two LC7536Rs can be used on the same bus by using the S (select) pin.
- Eighty positions in 1 dB steps plus mute (–∞), maximum attenuation is over 80 dB
- Input impedance (5 dB inputs): 47 kΩ (typical)
- High breakdown voltage: ±16 V

Package Dimensions

unit: mm

3047A-DIP30S

[LC7536R]



SANYO: DIP30S

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 18	V
	V_{EE} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} – 18 to V_{SS}	V
	V_{CC} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} to V_{SS} + 7	V
Input voltage	V_I1	CL, DI, CE	0 to V_{DD} + 0.3	V
	V_I2	IN1, IN2	V_{EE} – 0.3 to V_{DD} + 0.3	V
	V_I3	S	V_{CC} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	250	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

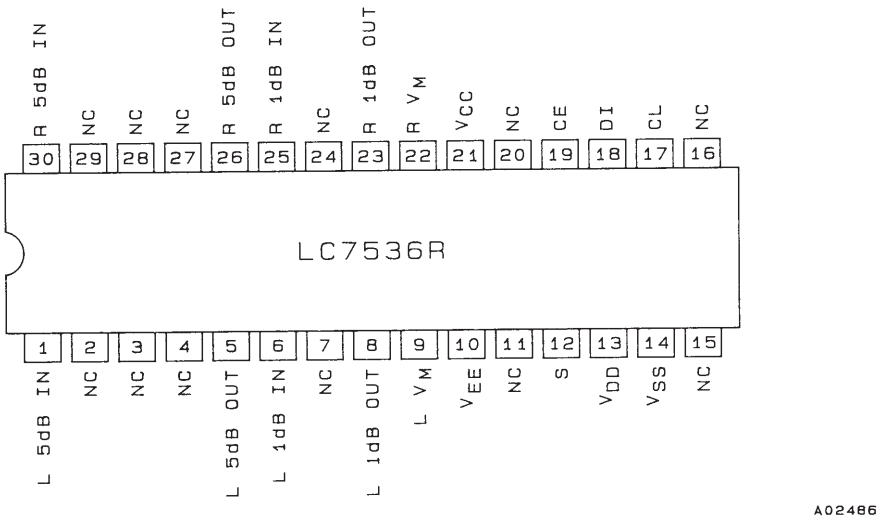
Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		V_{CC} + 4.5		16	V
	V_{EE}		–16		0	V
	V_{CC}		4.5	5	5.5	V
Input high level voltage	$V_{IH}1$	CL, DI, CE	0.8 V_{CC}		V_{CC}	V
Input low level voltage	$V_{IL}1$	CL, DI, CE	V_{SS}		0.2 V_{CC}	V
Input high level voltage	$V_{IH}2$	S	$0.8 \times (V_{DD} - V_{CC}) + V_{CC}$		V_{DD}	V
Input low level voltage	$V_{IL}2$	S	V_{CC}		$0.2 \times (V_{DD} - V_{CC}) + V_{CC}$	V
Input pulse width	tøw	CL	1			µs
Setup time	$t_{set\ up}$	CL, DI, CE	1			µs
Hold time	t_{hold}	CL, DI, CE	1			µs
Operating frequency	f_{opg}	CL			500	kHz
Input signal amplitude	V_{IN}	IN1, IN2	V_{EE}		V_{DD}	V
Input leakage current	I_{IN}	CL, DI, CE, S	–10		+10	µA

Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V

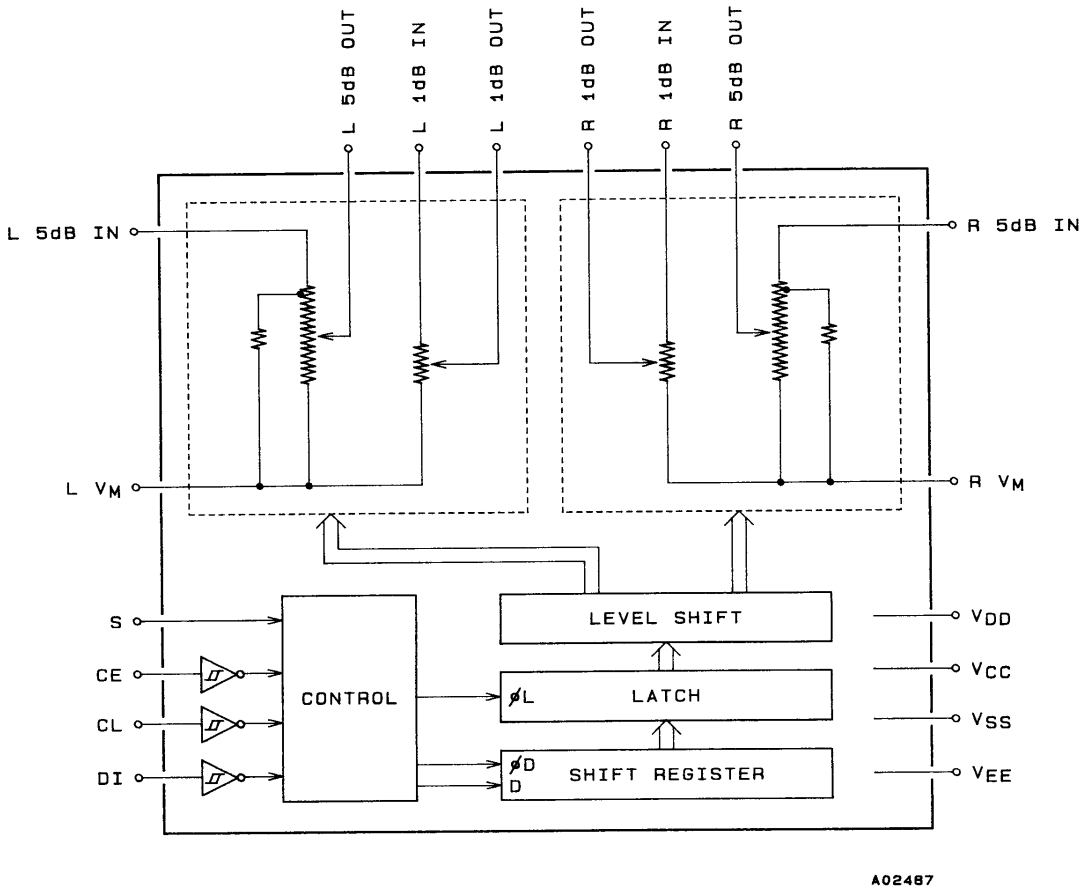
Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{DD}				1	mA
	I_{CC}				1	mA
Output off leakage current	I_{OFF}	IN1, IN2, V_M1, V_M2, CT1, CT2, OUT1, OUT2, analog switch off	–10		+10	µA
Total harmonic distortion	THD1	V_{IN} = 1 Vrms, f = 1 kHz, $V_{DD} - V_{EE}$ = 32 V, V_R = max		0.004		%
	THD2	V_{IN} = 0.1 Vrms, f = 1 kHz, $V_{DD} - V_{EE}$ = 32 V, V_R = max		0.02		%
Inter-channel crosstalk	C_T	OUT1 and OUT2, with a 20 kHz 1 Vrms input to one channel		–75	–60	dB
Output at maximum attenuation	V_O	f = 20 kHz, V_{IN} = 1 Vrms		–98		dB

Pin Assignment

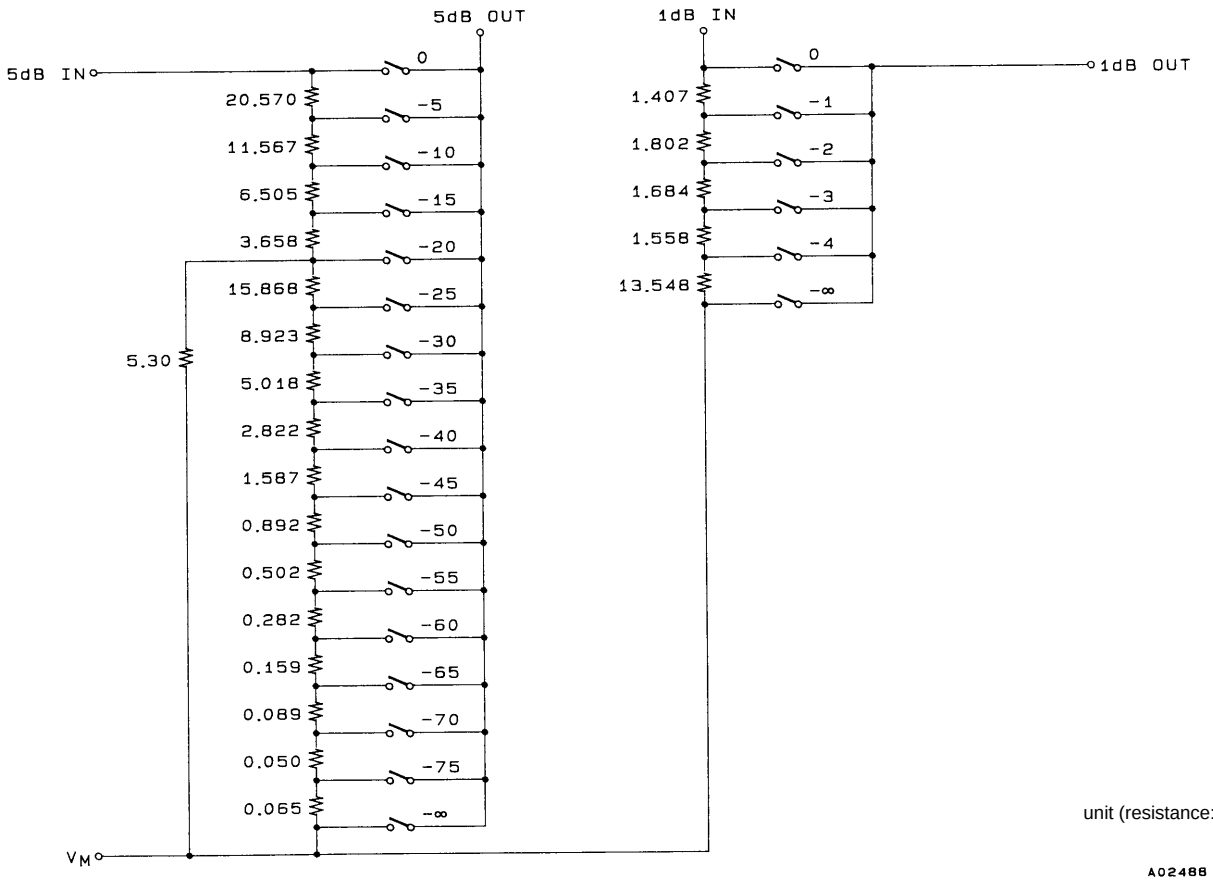


Top view

Equivalent Circuit Block Diagram

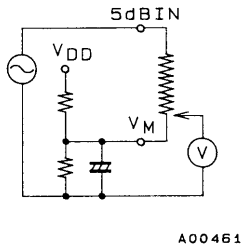


Internal Resistor Equivalent Circuit Diagram

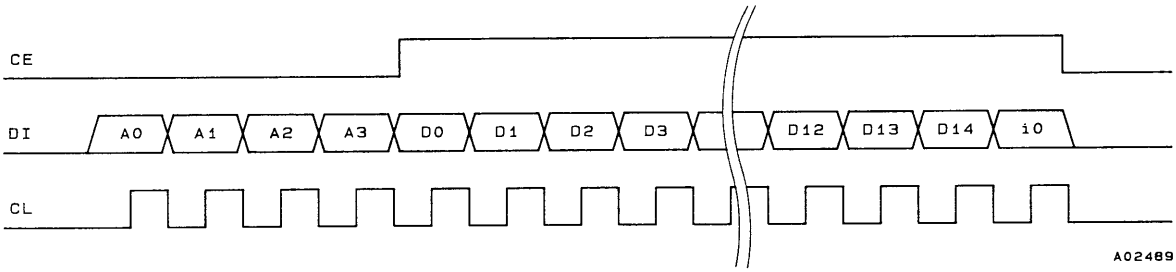


unit (resistance: KΩ)

Pin Functions

Pin No.	Symbol	Function	Note
1	L 5dBIN	Inputs to the 5 dB step attenuator. Must be driven by low impedance outputs.	
30	R 5dBIN		
3	NC	No connection	
4	NC		
28	NC		
27	NC		
5	L 5dBOUT	Outputs from the 5 dB step attenuator. Outputs should be received by a load of about 1 MΩ.	
26	R 5dBOUT		
6	L 1dBIN	Inputs to the 1 dB step attenuator. Must be driven by low impedance outputs.	
25	R 1dBIN		
8	L 1dBOUT	Outputs from the 1 dB step attenuator. Outputs should be received by a load in the range 47 kΩ to 1 MΩ.	
23	R 1dBOUT		
9	L V_M	Volume control common connections. The impedance of the pattern connected to these pins should be lowered as far as possible. Since LV_M, RV_M and V_{SS} are not connected internally, they should be connected externally according to their respective specifications. In particular, when a single-sided power supply is used, the capacitor connected between V_M and V_{SS} appears as the residual resistance when the volume is attenuated. Thus care is required when selecting the value for this capacitor.	
22	R V_M		
12	S	Selection pin for the address code in the data format. When this pin is connected to V_{DD}, the LC7536R will accept data when the address code is 9 and when connected to V_{CC}, the LC7536R will accept data when the address code is 8.	
17	CL	Inputs for controlling the LC7536R from serial data. Signals should have an amplitude of 0 to 5 V.	
18	DI		
19	CE		
10	V_{EE}	Power supply connections. Do not bring up the V_{CC} voltage before the V_{DD} voltage when powering up the LC7536R.	
13	V_{DD}		
14	V_{SS}		
21	V_{CC}		
2, 7, 11, 15, 16, 20, 24, 29	NC	No connection	

Data Format



Data consists of a total of 20 bits.

A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	i0

Address code

S pin	A0	A1	A2	A3
V_{DD}	1	0	0	1
V_{CC}	0	0	0	1

Right channel 5 dB step

	D0	D1	D2	D3
−75dB	0	0	0	0
−70dB	1	0	0	0
−65dB	0	1	0	0
−60dB	1	1	0	0
−55dB	0	0	1	0
−50dB	1	0	1	0
−45dB	0	1	1	0
−40dB	1	1	1	0
−35dB	0	0	0	1
−30dB	1	0	0	1
−25dB	0	1	0	1
−20dB	1	1	0	1
−15dB	0	0	1	1
−10dB	1	0	1	1
−5dB	0	1	1	1
0dB	1	1	1	1

Left channel 5 dB step
(Identical to the left channel)

Do not care

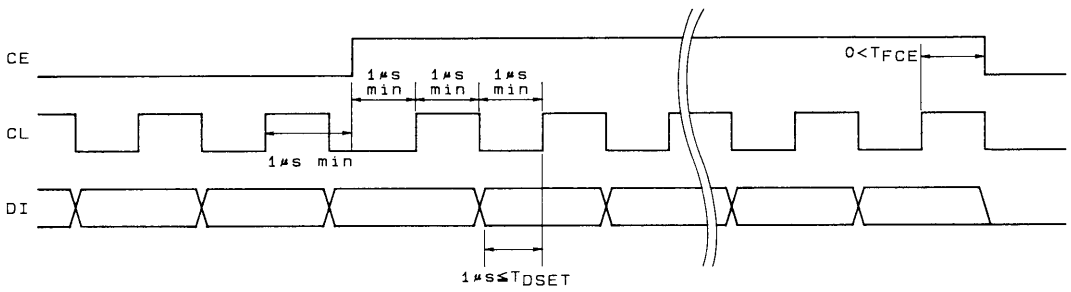
Right channel 1 dB step

Setting state	D4	D5	D6	D7
−∞	0	0	0	0
−4dB	0	1	0	0
−3dB	1	1	0	0
−2dB	0	0	1	0
−1dB	1	0	1	0
0dB	0	1	1	0

Left channel 1 dB step

Setting state	D12	D13	D14
−∞	0	0	0
−4dB	0	1	0
−3dB	1	1	0
−2dB	0	0	1
−1dB	1	0	1
0dB	0	1	1

A02490



Sample Application Circuit