Ordering number : ENN6450A

CMOS IC

LC74980W

LCD TV Scan Converter IC

Overview

The LC74980W is an LCD TV scan converter IC that converts an NTSC TV signal to an XGA personal computer video signal. This IC, in conjunction with a digital decoder, a microcontroller, and an LCD panel, can easily form an LCD TV video signal-processing circuit system. Since the LC74980W performs resolution conversion without an external frame memory, it can reduce system costs. Since this IC also provides PAL TV signal input and DTV inputs (480p and 480i formats), it provides the functions required in the next generation of LCD TV sets.

Features

- NTSC and PAL inputs: 8-bit digital YUV (CCIR 601) input
- DTV input: 8-bit digital YCbCr input
- Progressive-scan XGA RGB (6 bits per color, two-phase) signal output
- YUV to RGB conversion and YCbCr to RGB conversion
- Interlaced to progressive scan conversion
- Resolution conversion (enlargement)
- Variable display size and display position (independently settable in the horizontal and vertical directions)
- Image quality adjustments: brightness, contrast, color, sharpness, color phase, black balance, and white balance
- Built-in γ correction (programmable LUT technique)
- Dithering (8-bit to 6-bit conversion)
- Built-in OSD function (8 colors)
- I^2C bus interface
- Constant frame-rate processing (identical frame periods in the input and output signals) adopted so that no external memory is required.

Specifications

- Supply voltage: 3.3 V (input pins are 5 V tolerant)
- Maximum operating frequency: 65.0 MHz
- Package: SQFP208

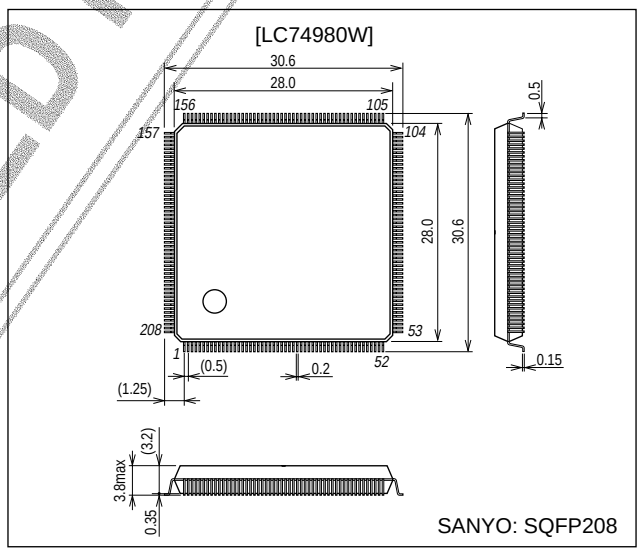
Applications

- LCD TVs, monitors, and projectors
- PDP displays
- Digital TV sets (both home and car products)

Package Dimensions

unit: mm

3210-SQFP208



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I/O Specifications

Input Specifications (Main input signals)

- Video signals
  TV: Two 8-bit digital YUV (CCIR 601) input systems. The Y data is 8 bits, and the UV signal is an 8-bit point sequential multiplexed signal.
  Note: NTSC and PAL signals are referred to simply as TV signals in this document.
  DTV: One 8-bit digital YCbCr (CCIR 601) input system. Supports the 480i and 480p formats.
  Note: This IC does not perform frame rate conversion. Thus only frame rates that fall within the operating range of the LCD panel module used are supported as input frame rates.
- Synchronizing signals:
  Both horizontal and vertical synchronizing signal are input as two independent systems. They are switched internally.
  Any input polarity may be used. The IC detects the polarity internally.
- Blanking signal:
  Provides as either a component signal or as a composite signal.
- Input processing clock:
  Two clock systems are input independently. They are switched internally.
- Output processing clock: A fixed-frequency oscillator provides 65.0 MHz clock.

Output Specifications (Main output signals)

- Video signal: Two-phase XGA digital RGB signal with 6 bits per color.
  A single-phase output mode is also support, and can be selected by settings using the I²C bus. (Output is from the ODD pin in this case.)
- Synchronizing signals:
  The period and polarity of both the horizontal and the vertical signals may be set. The synchronizing signal position is also variable.
  A composite synchronizing signal can also be output from the vertical output.
- Blanking signals:
  Horizontal and vertical blanking signals are provided. The periods and the polarities can be set.
  A composite blanking signal can also be output from the vertical output.
- Output processing clock:
  In XGA mode, 65.0 MHz (DCLK1) and 32.5 MHz (DCLK2) clocks are output.

Control Specifications

- I²C bus: Used for setting internal registers and for reading out status values. (SDA, SCL)
- Three-wire bus: Control bus used for OSD control and γ correction settings. (AIDA, AICK, AICS)
- External control output: EXCTR pin can be used for general-purpose control of circuits external to the IC over the I²C bus.

Electrical Characteristics

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}		–0.3 to +4.6	V
Input voltage	V_I		–0.5 to V_{IN} + 0.5	V
I/O voltages	V_I, V_O		–0.3 to V_{DD} + 0.3	V
Storage temperature	Tstg		–55 to +125	°C
Operating temperature	Topr		–30 to +70	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0	—	5.5	V

I/O Pin Capacitances at V_{DD} = $-V_I$ = 0 V, Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input pins	C_{IN}	f = 1 MHz	—	—	10	pF
Output pins	C_{OUT}	f = 1 MHz	—	—	10	pF
Bidirectional pins	$C_{I/O}$	f = 1 MHz	—	—	10	pF

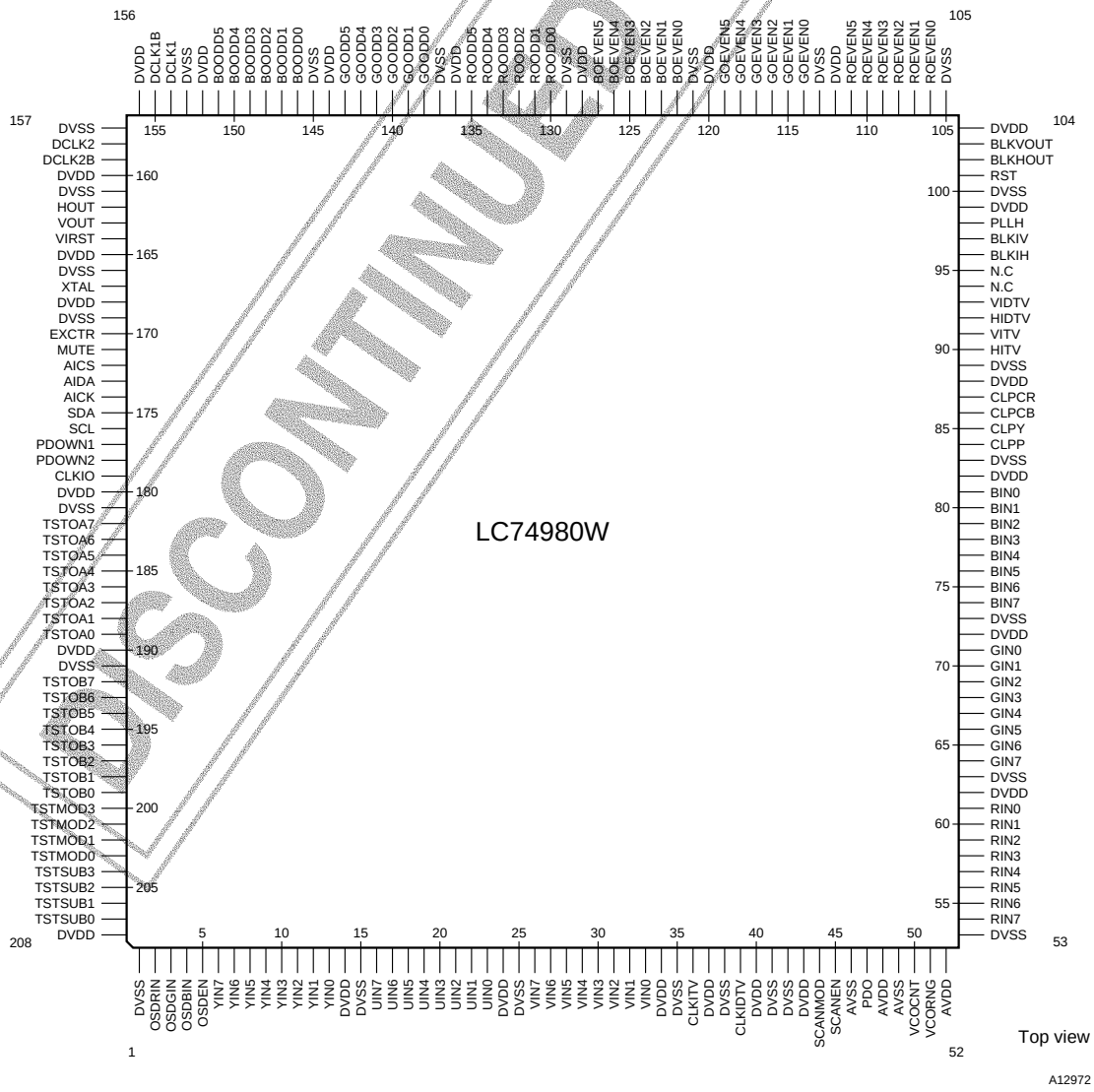
DC Characteristics at Ta = –30 to +70°C, V_{DD} = 3.0 to 3.6 V, V_{IDD} = 3.0 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	CMOS level	0.7 V_{DD}	—	—	V
		CMOS level Schmitt	0.75 V_{DD}	—	—	V
Input low-level voltage	V_{IL}	CMOS level	—	—	0.2 V_{IDD}	V
		CMOS level Schmitt	—	—	0.15 V_{IDD}	V
Input high-level current	I_{IH}	$V_I = V_{DD}$	–10	—	+10	µA
		$V_I = V_{DD}$, with pull-down resistors attached.	+10	—	+100	µA
Input low-level current	I_{IL}	$V_I = V_{SS}$	–10	—	+10	µA
Output high-level voltage	V_{OH}	Type B4, I_{OH} = –2 mA	V_{DD} – 0.8	—	—	V
		Type B8, I_{OH} = –4 mA	V_{DD} – 0.8	—	—	V
		Type B12, I_{OH} = –6 mA	V_{DD} – 0.8	—	—	V
Output low-level voltage	V_{OL}	Type B4, I_{OL} = 2 mA	—	—	0.4	V
		Type B8, I_{OL} = 4 mA	—	—	0.4	V
		Type B12, I_{OL} = 6 mA	—	—	0.4	V
Output leakage current	I_{OZ}	In the high-impedance output state	–10	—	+10	µA
Pull-down resistance	R_{DN}		34.3	68.5	137	kΩ
Quiescent current*	I_{DD}	Outputs open, $V_I = V_{SS}$ or V_{DD}	—	—	100	µA

*: Note that the rating cannot be always guaranteed due to the circuit structure such as a case where the circuit includes a pull-down resistor.

Pins

Pin Assignment



Pin Functions

Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
1	DVSS	P		GND	Digital system ground
2	OSDRIN	I	g74980m03	Caption OSD microcontroller	OSD red input
3	OSDGIN	I	g74980m03	Caption OSD microcontroller	OSD green input
4	OSDBIN	I	g74980m03	Caption OSD microcontroller	OSD blue input
5	OSDEN	I	g74980m03	Caption OSD microcontroller	OSD data enable
6	YIN7	I	g74980m03	Digital decoder	MSB
7	YIN6	I	g74980m03	or	TV Y signal input
8	YIN5	I	g74980m03	ADC	or
9	YIN4	I	g74980m03		DTV Y signal input
10	YIN3	I	g74980m03		
11	YIN2	I	g74980m03		
12	YIN1	I	g74980m03		
13	YIN0	I	g74980m03		LSB
14	DVDD	P		Power supply	Digital system power supply: 3.3 V
15	DVSS	P		GND	Digital system ground
16	UIN7	I	g74980m03	Digital decoder	MSB
17	UIN6	I	g74980m03	or	TV UV multiplexed signal input
18	UIN5	I	g74980m03	ADC	or
19	UIN4	I	g74980m03		DTV Cb signal input
20	UIN3	I	g74980m03		
21	UIN2	I	g74980m03		
22	UIN1	I	g74980m03		
23	UIN0	I	g74980m03		LSB
24	DVDD	P		Power supply	Digital system power supply: 3.3 V
25	DVSS	P		GND	Digital system ground
26	VIN7	I	g74980m03	Digital decoder	MSB
27	VIN6	I	g74980m03	or	DTV Cr signal input
28	VIN5	I	g74980m03	ADC	
29	VIN4	I	g74980m03		
30	VIN3	I	g74980m03		
31	VIN2	I	g74980m03		
32	VIN1	I	g74980m03		
33	VIN0	I	g74980m03		LSB
34	DVDD	P		Power supply	Digital system power supply: 3.3 V
35	DVSS	P		GND	Digital system ground
36	CLKITV	I	g74980m05	Digital decoder	TV clock input (data rate)
37	DVDD	P		Power supply	Digital system power supply: 3.3 V
38	DVSS	P		GND	Digital system ground
39	CLKIDTV	I	g74980m05	PLL	DTV clock input
40	DVDD	P		Power supply	Digital system power supply: 3.3 V
41	DVSS	P		GND	Digital system ground
42	DVSS	P		GND	Digital system ground
43	DVDD	P		Power supply	Digital system power supply: 3.3 V
44	SCANMOD	I	g74980m03	Open	Scan test mode
45	SCANEN	I	g74980m03	Open	Scan test enable
46	AVSS	P		Power supply	Analog system ground
47	PDO	O	zwp3vp113	Loop filter	Charge pump output (Leave open when unused.)
48	AVDD	P		Power supply	Analog system power supply: 3.3 V
49	AVSS	P		Power supply	Analog system ground
50	VCOCNT	I	g74100m06	Loop filter	VCO control input (Connect to AVSS when unused.)
51	VCORNG	I	g74100m06	Resistor	VCO bias resistor input (Connect to AVSS when unused.)
52	AVDD	P		Power supply	Analog system power supply: 3.3 V

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Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
53	DVSS	P		GND	Digital system ground
54	RIN7	I	g74980m03	ADC	MSB
55	RIN6	I	g74980m03		Y signal input
56	RIN5	I	g74980m03		
57	RIN4	I	g74980m03		
58	RIN3	I	g74980m03		
59	RIN2	I	g74980m03		
60	RIN1	I	g74980m03		
61	RIN0	I	g74980m03		LSB
62	DVDD	P		Power supply	Digital system power supply: 3.3 V
63	DVSS	P		GND	Digital system ground
64	GIN7	I	g74980m03	ADC	MSB
65	GIN6	I	g74980m03		U signal input
66	GIN5	I	g74980m03		
67	GIN4	I	g74980m03		
68	GIN3	I	g74980m03		
69	GIN2	I	g74980m03		
70	GIN1	I	g74980m03		
71	GIN0	I	g74980m03		LSB
72	DVDD	P		Power supply	Digital system power supply: 3.3 V
73	DVSS	P		GND	Digital system ground
74	BIN7	I	g74980m03	ADC	MSB
75	BIN6	I	g74980m03		V signal input
76	BIN5	I	g74980m03		
77	BIN4	I	g74980m03		
78	BIN3	I	g74980m03		
79	BIN2	I	g74980m03		
80	BIN1	I	g74980m03		
81	BIN0	I	g74980m03		LSB
82	DVDD	P		Power supply	Digital system power supply: 3.3 V
83	DVSS	P		GND	Digital system ground
84	CLPP	O	POB4	ADC	Clamp pulse
85	CLPY	O	POT4	ADC	Y clamp level
86	CLPCB	O	POT4	ADC	Cb clamp level
87	CLPCR	O	POT4	ADC	Cr clamp level
88	DVDD	P		Power supply	Digital system power supply: 3.3 V
89	DVSS	P		GND	Digital system ground
90	HITV	I	g74980m04	TV decoder	TV horizontal synchronizing signal input
91	VITV	I	g74980m04	TV decoder	TV vertical synchronizing signal input
92	HIDTV	I	g74980m04	Digital interface	DTV horizontal synchronizing signal input
93	VIDTV	I	g74980m04	Digital interface	DTV vertical synchronizing signal input
94	N.C	—	—	—	—
95	N.C	—	—	—	—
96	BLKIH	I	g74980m02	Digital interface	Horizontal blanking signal input or composite blanking signal
97	BLKIV	I	g74980m02	Digital interface	Vertical blanking signal input (Held high in composite mode)
98	PLLH	O	POB4	PLL	PLL internal divider output
99	DVSS	P		GND	Digital system ground
100	DVDD	P		Power supply	Digital system power supply: 3.3 V
101	RST	I	g74980m01	Initialization circuit	System reset (reset to low)
102	BLKHOUT	O	POB8	Initialization circuit	Horizontal data enable
103	BLKVOUT	O	POB8	Initialization circuit	Vertical data enable or composite data enable
104	DVDD	P		Power supply	Digital system power supply: 3.3 V

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Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
105	DVSS	P		GND	Digital system ground
106	ROEVEN0	O	POB4	LCD module	LSB
107	ROEVEN1	O	POB4		Red signal output (even)
108	ROEVEN2	O	POB4		
109	ROEVEN3	O	POB4		
110	ROEVEN4	O	POB4		
111	ROEVEN5	O	POB4		MSB
112	DVDD	P		Power supply	Digital system power supply: 3.3 V
113	DVSS	P		GND	Digital system ground
114	GOEVEN0	O	POB4	LCD module	LSB
115	GOEVEN1	O	POB4		Green signal output (even)
116	GOEVEN2	O	POB4		
117	GOEVEN3	O	POB4		
118	GOEVEN4	O	POB4		
119	GOEVEN5	O	POB4		MSB
120	DVDD	P		Power supply	Digital system power supply: 3.3 V
121	DVSS	P		GND	Digital system ground
122	BOEVEN0	O	POB4	LCD module	LSB
123	BOEVEN1	O	POB4		Blue signal output (even)
124	BOEVEN2	O	POB4		
125	BOEVEN3	O	POB4		
126	BOEVEN4	O	POB4		
127	BOEVEN5	O	POB4		MSB
128	DVDD	P		Power supply	Digital system power supply: 3.3 V
129	DVSS	P		GND	Digital system ground
130	ROODD0	O	POB4	LCD module	LSB
131	ROODD1	O	POB4		Red signal output (odd)
132	ROODD2	O	POB4		or
133	ROODD3	O	POB4		Red signal single-phase output
134	ROODD4	O	POB4		
135	ROODD5	O	POB4		MSB
136	DVDD	P		Power supply	Digital system power supply: 3.3 V
137	DVSS	P		GND	Digital system ground
138	GOODD0	O	POB4	LCD module	LSB
139	GOODD1	O	POB4		Green signal output (odd)
140	GOODD2	O	POB4		or
141	GOODD3	O	POB4		Green signal single-phase output
142	GOODD4	O	POB4		
143	GOODD5	O	POB4		MSB
144	DVDD	P		Power supply	Digital system power supply: 3.3 V
145	DVSS	P		GND	Digital system ground
146	BOODD0	O	POB4	LCD module	LSB
147	BOODD1	O	POB4		Blue signal output (odd)
148	BOODD2	O	POB4		or
149	BOODD3	O	POB4		Blue signal single-phase output
150	BOODD4	O	POB4		
151	BOODD5	O	POB4		MSB
152	DVDD	P		Power supply	Digital system power supply: 3.3 V
153	DVSS	P		GND	Digital system ground
154	DCLK1	O	POB12	LCD module	Data clock 1 (for single-phase data output)
155	DCLK1B	O	POB12	LCD module	Inverted data clock 1 (for single-phase data output)
156	DVDD	P		Power supply	Digital system power supply: 3.3 V

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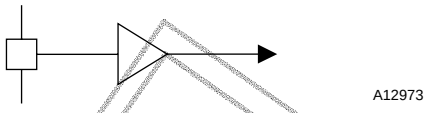
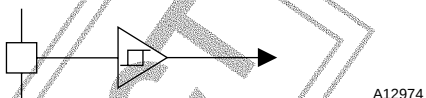
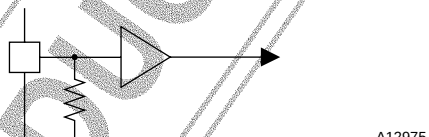
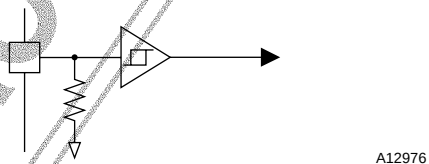
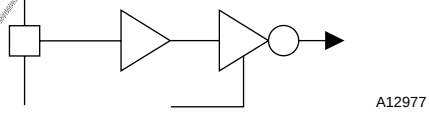
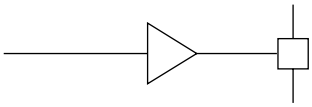
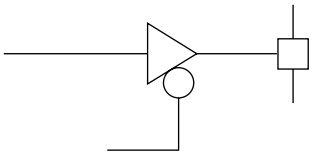
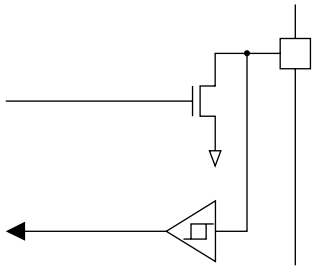
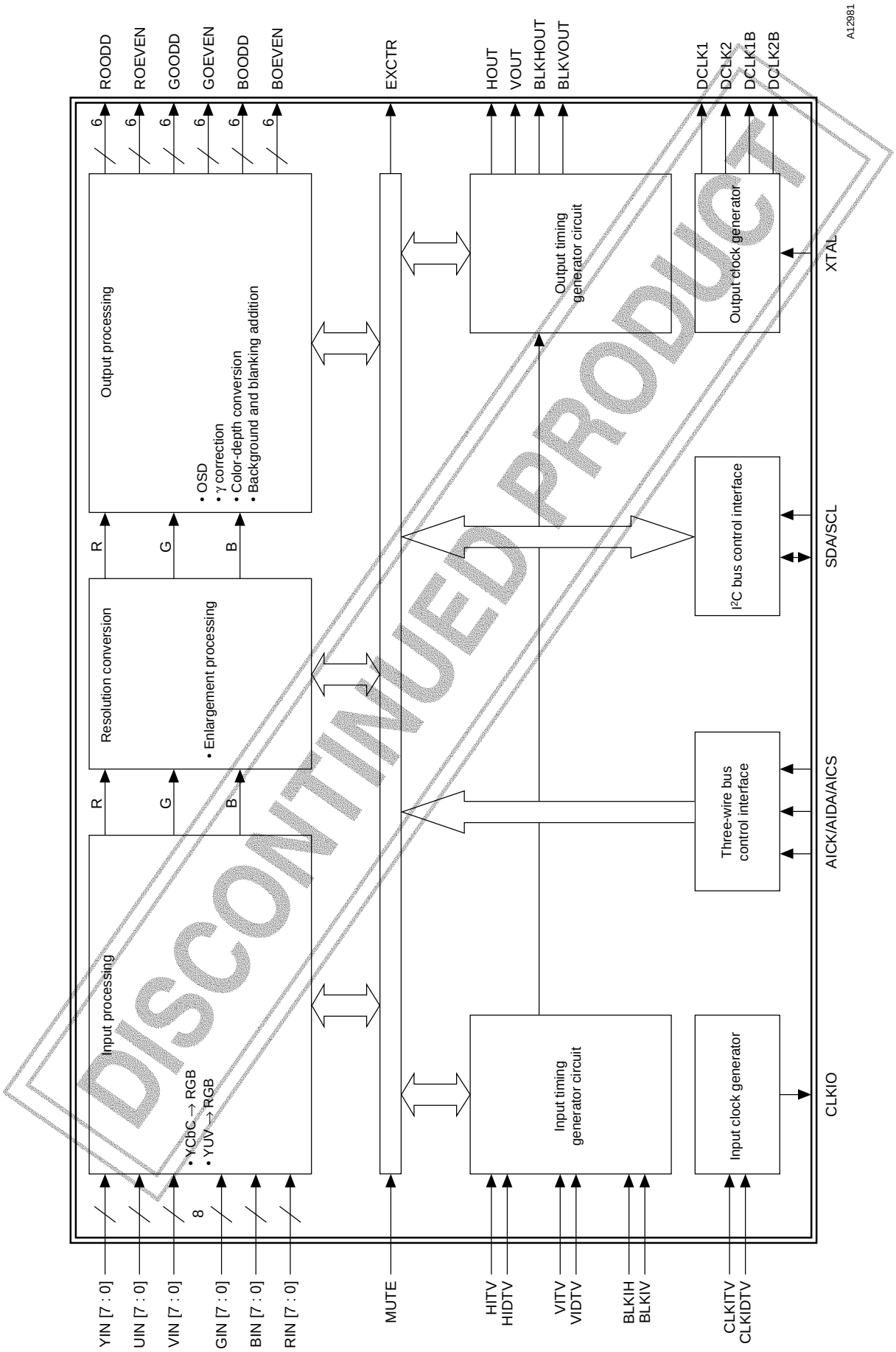
Pin No.	Pin	I/O type		Connection	Notes
		I/O	Type		
157	DVSS	P		GND	Digital system ground
158	DCLK2	O	POB12	—	Data clock 2 (for two-phase data output)
159	DCLK2B	O	POB12	—	Inverted data clock 2 (for two-phase data output)
160	DVDD	P		Power supply	Digital system power supply: 3.3 V
161	DVSS	P		GND	Digital system ground
162	HOUT	O	POB8	LCD module	Horizontal sync output
163	VOUT	O	POB8	LCD module	Vertical synchronizing signal output or composite synchronizing signal output
164	VIRST	O	POB4	XTAL	Crystal oscillator reset
165	DVDD	P		Power supply	Digital system power supply: 3.3 V
166	DVSS	P		GND	Digital system ground
167	XTAL	I	g74980m01	VCO	Crystal oscillator circuit output
168	DVDD	P		Power supply	Digital system power supply: 3.3 V
169	DVSS	P		GND	Digital system ground
170	EXCTR	O	POB4	—	External control output (output controlled over the I^2C bus)
171	MUTE	I	g74980m02	Microcontroller	Mute control input (mute to low)
172	AICS	I	g74980m02	Microcontroller	3-wire bus control chip select
173	AIDA	I	g74980m02	Microcontroller	3-wire bus control bus data
174	AICK	I	g74980m02	Microcontroller	3-wire bus control bus clock
175	SDA	B	g74980m06	Microcontroller	I^2C control data
176	SCL	I	g74980m02	Microcontroller	I^2C control clock
177	PDOWN1	I	g74980m01	Microcontroller	Power down 1 (low in normal mode)
178	PDOWN2	I	g74980m01	Microcontroller	Power down 2 (high in normal mode)
179	CLKI0	O	POB12	—	Input system clock output
180	DVDD	P		Power supply	Digital system power supply: 3.3 V
181	DVSS	P		GND	Digital system ground
182	TSTOA7	O	POB4	OPEN	MSB
183	TSTOA6	O	POB4		Test outputs
184	TSTOA5	O	POB4		
185	TSTOA4	O	POB4		
186	TSTOA3	O	POB4		
187	TSTOA2	O	POB4		
188	TSTOA1	O	POB4		
189	TSTOA0	O	POB4		LSB
190	DVDD	P		Power supply	Digital system power supply: 3.3 V
191	DVSS	P		GND	Digital system ground
192	TSTOB7	O	POB4	OPEN	MSB
193	TSTOB6	O	POB4		Test outputs
194	TSTOB5	O	POB4		
195	TSTOB4	O	POB4		
196	TSTOB3	O	POB4		
197	TSTOB2	O	POB4		
198	TSTOB1	O	POB4		
199	TSTOB0	O	POB4		LSB
200	TSTMOD3	I	g74980m03	OPEN	Test mode
201	TSTMOD2	I	g74980m03		
202	TSTMOD1	I	g74980m03		
203	TSTMOD0	I	g74980m03		
204	TSTSUB3	I	g74980m03	OPEN	Test sub-mode
205	TSTSUB2	I	g74980m03		
206	TSTSUB1	I	g74980m03		
207	TSTSUB0	I	g74980m03		
208	DVDD	P		Power supply	Digital system power supply: 3.3 V

Pin Type

I/O type	Applicable pins	Function	Equivalent circuit
g74980m01	RST PDOWN1 to 2 XTAL	3 to 5 V voltage handling input	 A12973
g74980m02	AICS, AIDA, AICK SCL BLKIH, BLKIV MUTE	3 to 5 V voltage handling Schmitt input	 A12974
g74980m03	OSDRIN, OSDGIN, OSDBIN, OSDEN YIN0 to 7, UIN0 to 7, VIN0 to 7 SCANMOD, SCANEN RIN0 to 7, GIN0 to 7, BIN0 to 7 TSTMOD0 to 3, TSTSUB0 to 3 Leave open when unused.	3 to 5 V voltage handling pull-down input	 A12975
g74980m04	HITV, VITV HIDTV, VIDTV	3 to 5 V voltage handling pull-down Schmitt input	 A12976
g74980m05	CLKITV CLKIDTV	3 to 5 V voltage handling OE input	 A12977
POB4	CLPP, PLLH, ROEVEN0 to 5, GOEVEN0 to 5, BOEVEN0 to 5 ROODD0 to 5, GOODD0 to 5, BOODD0 to 5 VIRST, EXCTR, TST0A0 to 7, TST0B0 to 7	4 mA drive output	 A12978
POB8	BLKHOUT, BLKVOUT HOUT, VOUT	8 mA drive output	
POB12	DCLK1, DBLK1B, DCLK2, DCLK2B CLKI0	12 mA drive output	
POT4	CLPY, CLPCB, CLPCR	4 mA 3-state drive output	 A12979
g74980m06	SDA	Open-drain I/O	 A12980

IC Internal Block Diagram



Supplementary Documentation: Sample Application (LCD TV)