Ordering number : *EN5039

CMOS IC

LC74763, 74763M

On-Screen Display LSI

Preliminary

Overview

The LC74763 and LC74763M are on-screen display CMOS LSIs that superimpose text and low-level graphics onto a TV screen (video signal) under the control of a microcontroller. The display characters have a 12 by 18 dots structure, and 128 characters are provided.

Features

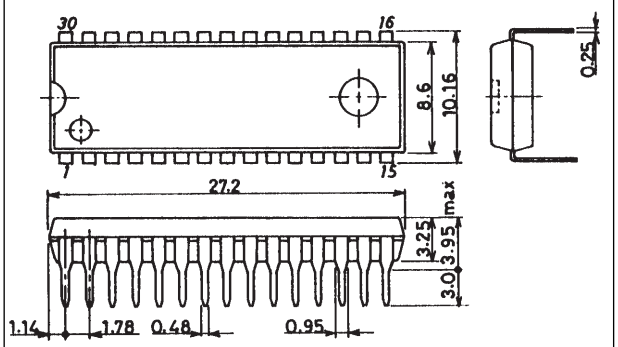
- Display structure: 12 lines by 24 characters (up to 288 characters)
- Maximum character display: Up to 288 characters
- Character configuration: 12 (W) by 18 (H) dots structure
- Number of characters: 128 characters (128 plus space 2 fonts)
- Character sizes: Three sizes (normal, double, and triple sizes)
- Display starting positions: 64 horizontal and 64 vertical locations
- Reverse video function: Characters can be inverted on a per character basis.
- Flashing types: Two types with periods of 0.5 and 1.0 second on a per character basis (duty fixed at 50%)
- Background color: One of eight colors (when internal synchronization used)
- External control input: Serial data input in 8-bit units
- Built-in horizontal/vertical sync separation circuit, AFC circuit, and synchronization detector
- Video output: Composite video signal output in NTSC, PAL, PAL-M, PAL-N, PAL60, NTSC4.43, or SECAM format

Package Dimensions

unit: mm

3196-DIP30SD

[LC74763]

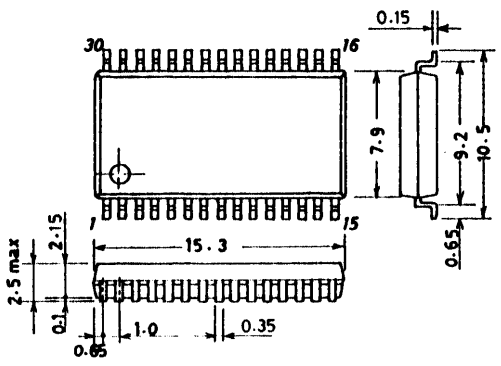


SANYO: DIP30SD

unit: mm

3216A-MFP30S

[LC74763M]



SANYO: MFP30S

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD1}, V_{DD2} pins	V_{SS} – 0.3 to V_{SS} + 7.0	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max	$HSYNC_{OUT}$, $VSYNC_{OUT}$, $SYNC_{DET}$ pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Supply voltage	V_{DD1}	V_{DD1} pin		4.5	5.0	5.5	V
	V_{DD2}	V_{DD2} pin		4.5	5.0	1.27 V_{DD1}	V
Input high level voltage	V_{IH1}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK pins		0.8 V_{DD1}		V_{DD1} + 0.3	V
	V_{IH2}	SECAM, $\overline{525}$/625, $\overline{NTSC}$/PAL, $\overline{3.58}$/4.43 pins		0.7 V_{DD1}		V_{DD1} + 0.3	V
Input low level voltage	V_{IL1}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK		V_{SS} – 0.3		0.2 V_{DD1}	V
	V_{IL2}	SECAM, $\overline{525}$/625, $\overline{NTSC}$/PAL, $\overline{3.58}$/4.43 pins		V_{SS} – 0.3		0.3 V_{DD1}	V
Input voltage	V_{IN}	FC, AMP_{IN} pins		V_{SS} – 0.3		V_{DD1} + 0.3	V
Composite video signal input voltage	V_{IN1}	CVIN pins			2 V_{PP}		V
	V_{IN2}	CV_{CR} pins			2 V_{PP}		V
	V_{IN3}	$SYNC_{IN}$ pins			2 V_{PP}	2.5 V_{PP}	V
Oscillator frequency	F_{OSC1}	$Xtal_{IN1}$, $Xtal_{OUT1}$, $Xtal_{IN2}$, $Xtal_{OUT2}$ pins; 4fsc	NTSC		14.318		MHz
			PAL		17.734		MHz
			PAL-M		14.302		MHz
			PAL-N		14.328		MHz

Electrical Characteristics at Ta = –30 to +70°C, with V_{DD1} = V_{DD2} = 5 V unless otherwise specified

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Output off leakage current	I_{leak1}	CV_{OUT} pin			10	µA
Input off leakage current	I_{leak2}	CV_{IN}, CV_{CR} pins			10	µA
Output high level voltage	V_{OH}	$HSYNC_{OUT}$, $VSYNC_{OUT}$, $SYNC_{DET}$, SECAM, $\overline{525}$/625, NTSC/PAL, $\overline{3.58}$/4.43, AMP_{OUT}, PD_{OUT} pins; V_{DD1} = 4.5 V, I_{OH} = –1.0 mA	3.5			V
Output low level voltage	V_{OL}	$HSYNC_{OUT}$, $VSYNC_{OUT}$, $SYNC_{DET}$, SECAM, $\overline{525}$/625, $\overline{NTSC}$/PAL, $\overline{3.58}$/4.43, AMP_{OUT}, PD_{OUT} pins; V_{DD1} = 4.5 V, I_{OL} = 1.0 mA			1.0	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SECAM, $\overline{525}$/625, $\overline{NTSC}$/PAL, $\overline{3.58}$/4.43 pins; V_{IN} = V_{DD1}			1	µA
	I_{IL}	SECAM, $\overline{525}$/625, $\overline{NTSC}$/PAL, $\overline{3.58}$/4.43 pin; V_{IN} = V_{SS1}	–1			µA
Oscillator frequency	F_{OSC3}	VCO_{IN}, VCO_{OUT} pins; FC = 1/2 V_{DD1}		14.12		MHz
Operating current dissipation	I_{DD1}	V_{DD1} pin; All outputs open, Xtal: 4fsc			15	mA
	I_{DD2}	V_{DD2} pin; V_{DD2} = 5.0 V			20	mA

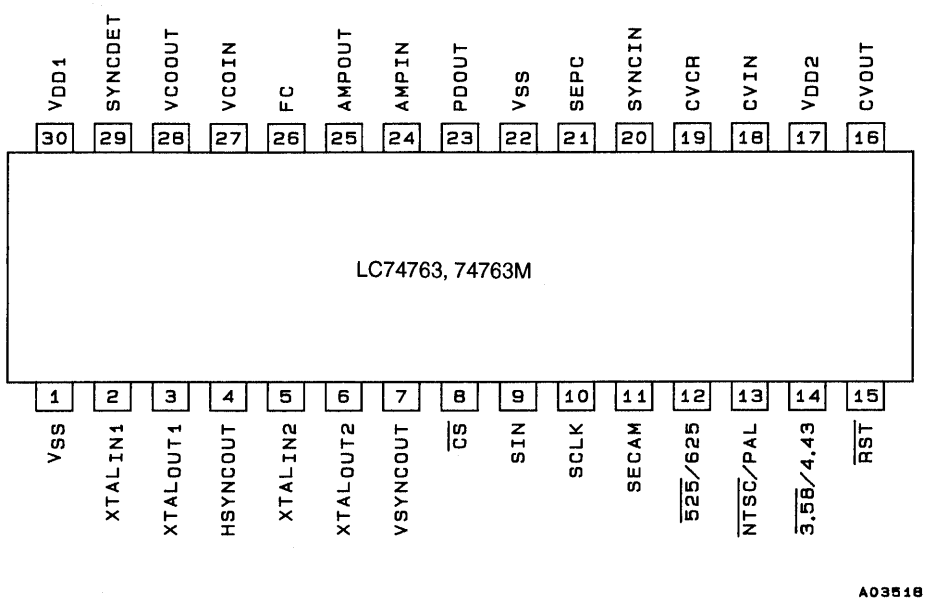
Timing Characteristics at Ta = –30 to +70°C, V_{DD} = 5 ±0.5 V

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Minimum input pulse width	$t_{W(SCLK)}$	SCLK pin	200			ns
	$t_{W(CS)}$	$\overline{CS}$ pin (during periods when $\overline{CS}$ is high)	1			µs
Data setup time	$t_{SU(CS)}$	$\overline{CS}$ pin	200			ns
	$t_{SU(SIN)}$	SIN pin	200			ns
Data hold time	$t_{h(CS)}$	$\overline{CS}$ pin	2			µs
	$t_{h(SIN)}$	SIN pin	200			ns
One word write time	t_{word}	Write time for 8 bits of data	4.2			µs
	t_{wt}	RAM data write time	1			µs

Pin Functions

Pin No.	Symbol	Function	Description
1	V_{SS}	Ground	Ground connection
2	$Xtal_{IN1}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. The oscillator can be selected with a command switch.
3	$Xtal_{OUT1}$		
4	$HSYNC_{OUT}$	Horizontal synchronization output	Outputs the horizontal synchronization signal (AFC). The output polarity can be selected (metal option). Also functions as general output port (command switch).
5	$Xtal_{IN2}$	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal.
6	$Xtal_{OUT2}$		
7	$VSYNC_{OUT}$	Vertical synchronization output	Outputs the vertical synchronization signal. The output polarity can be selected (metal option). Also functions as general output port (command switch).
8	$\overline{CS}$	Enable input	Enables/disables serial data input. Serial data is enabled when this pin is low (hysteresis input). Pull-up resistor built in (metal option).
9	SIN	Data input	Serial data input (hysteresis input). Pull-up resistor built in (metal option).
10	SCLK	Clock input	Clock input for serial data input (hysteresis input). Pull-up resistor built in (metal option).
11	SECAM	SECAM mode switch input/ output (command switch)	During input, switches between SECAM and other modes. During output, functions as general output port or internal V output (command switch). Low = other modes, high = SECAM mode
12	$\overline{525}$/625	525/625 switch input/output (command switch)	During input, switches between 525 scan lines and 625 scan lines. During output, functions as general output port or character data output (command switch). Low = 525 lines, high = 625 lines
13	$\overline{NTSC}$/PAL	NTSC/PAL switch input/output (command switch)	Switches the color mode between NTSC and PAL. During output, functions as general output port or frame data output (command switch). Low = NTSC, high = PAL
14	$\overline{3.58}$/4.43	3.58/4.43 switch input/output (command switch)	Switch FSC between 3.58 MHz and 4.43 MHz. During output, functions as general output port or halftone output (command switch). Low = 3.58, high = 4.43
15	$\overline{RST}$	Reset input	System reset input pin, low is active (hysteresis input). Pull-up resistor built in (metal option).
16	CV_{OUT}	Video signal output	Composite video output
17	V_{DD2}	Power supply connection	Power supply connection for composite video signal level generation
18	CV_{IN}	Video signal input	Composite video input
19	CV_{CR}	Video signal input	SECAM chroma signal input
20	$SYNC_{IN}$	Sync separator circuit input	Built-in sync separator circuit video signal input
21	SEP_{C}	Sync separator circuit	Built-in sync separator circuit
22	V_{SS}	Ground	Ground connection
23	PD_{OUT}	Control voltage output	AFC control voltage output
24	AMP_{IN}	AFC filter connection	Filter connection
25	AMP_{OUT}		
26	FC	Control voltage input	AFC control voltage input
27	VCO_{IN}	LC oscillator connection	VCO LC oscillator circuit coil and capacitor connection
28	VCO_{OUT}		
29	$SYNC_{DET}$	External synchronization signal detection output	Outputs the exclusive NOR of the horizontal synchronization signal (AFC) and CSYNC (sync separator). The output polarity can be selected (metal option). Also functions as general output port (command switch).
30	V_{DD1}	Power supply connection	Power supply connection (+5 V: digital system power supply)

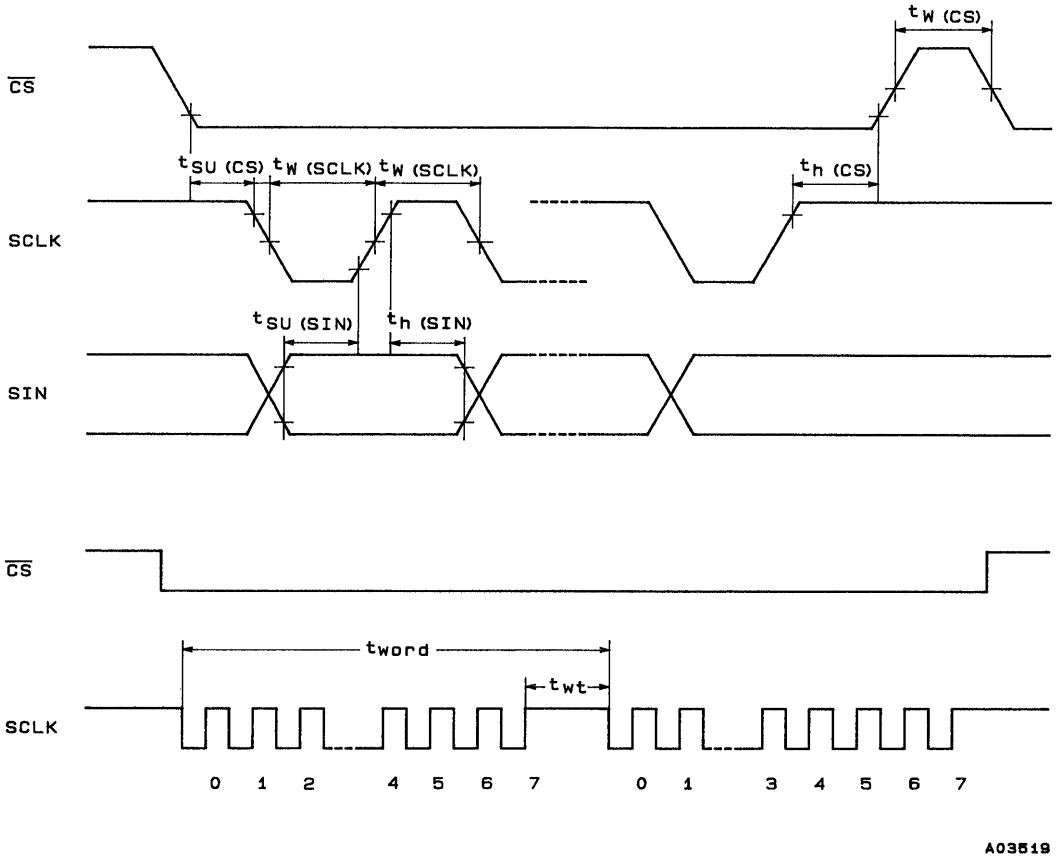
Pin Assignment



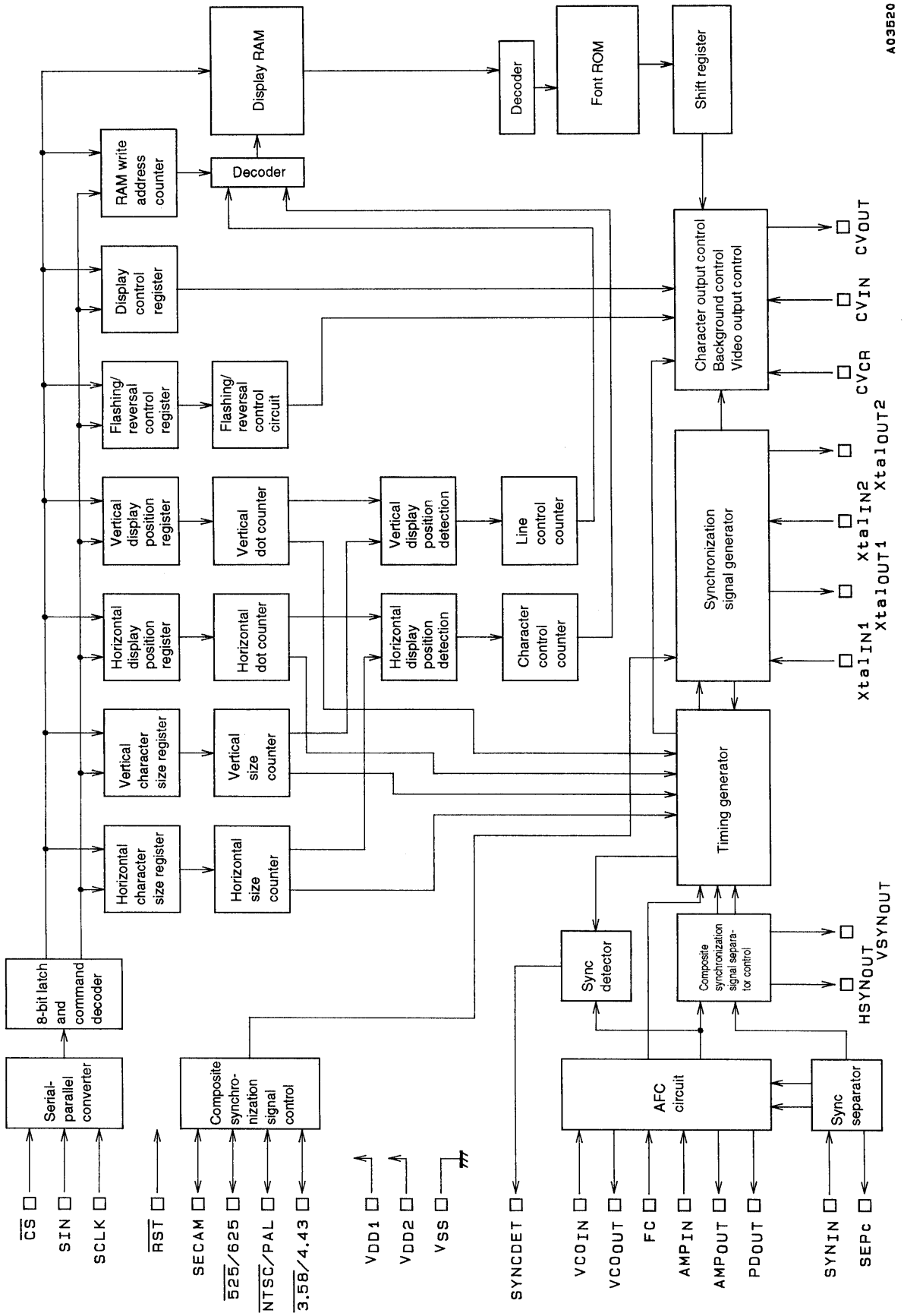
Top View

Top view

Serial Data Input Timing



System Block Diagram



Display Control Commands

Display control commands are input in an 8-bit serial format. Commands consist of a command identification code in the first byte and data in the second and following bytes. The following commands are supported.

① COMMAND0: Display memory (VRAM) write address setting command
② COMMAND1: Display character data write command
③ COMMAND2: Vertical display start position and character size (lines 1 and 2) setting command
④ COMMAND3: Horizontal display start position and character size (lines 9 and 11) setting command
⑤ COMMAND4: Display control setting command 1
⑥ COMMAND5: Display control setting command 2
⑦ COMMAND6: Display control setting command 3
⑧ COMMAND7: Display control setting command 4

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	at2	at1	c7	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical display start position	1	0	1	0	SZ 21	SZ 20	SZ 11	SZ 10	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal display start position	1	0	1	1	SZ B1	SZ B0	SZ 91	SZ 90	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control 1	1	1	0	0	RST	RAM	OSC	RND	0	I/N	BLK 1	BLK 0	BK 1	ATS	0	DSP
COMMAND5 Display control 2	1	1	0	1	PH 2	PH 1	PH 0	I/E	0	TST	CHAL	BKL	RSL 1	RSL 0	CVM	XTS
COMMAND6 Display control 3	1	1	1	0	MOD 3	MOD 2	MOD 1	MOD 0	0	HFI	M30S	SMS	IOS	BCL 1	BCL 0	CB
COMMAND70 Display control 4	1	1	1	1	0	0	0	LINS	0	VCOS 1	LIN 5	LIN 4	LIN 3	LIN 2	LIN 1	LIN 0
COMMAND71 Display control 5	1	1	1	1	0	1	0	LINS	0	EG 2	PS 2	PS 1	VMN	SVIS	VNS	VSS
COMMAND72 Display control 6	1	1	1	1	1	0	0	LINS	0	0	0	0	MOD 3	MOD 2	MOD 1	MOD 0
COMMAND73 Display control 7	1	1	1	1	1	1	0	LINS	0	0	0	0	VCOS 2	SOUT	VOUT	HOUT

Once the command identification code in the first bite is written, it is stored internally until the first byte of the following command is written. However, when the display character data write command (COMMAND1) is written, the system becomes locked in display character data write mode, and the first byte cannot be overwritten.

When the $\overline{CS}$ pin is set high the command state is set to COMMAND0, i.e., display memory write address setting mode.

① COMMAND0: Display Memory Write Address Setting Command

First data byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 0 identification code: sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (from 0 to B (hexadecimal))	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory character address (from 0 to 17 (hexadecimal))	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: When the chip is reset by the $\overline{\text{RST}}$ pin, the register states (bits) are all cleared to 0.

② COMMAND1: Display Character Data Write Setting Command

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 1 identification code: sets the display memory write address.	When this command is entered, the chip locks in display character write mode until the ~~CS~~ pin is set high.
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	at2	0	Turns character attribute 2 off.	Specifies highlight or flashing.
		1	Turns character attribute 2 on.	
0	at1	0	Turns character attribute 1 off.	Specifies reverse video.
		1	Turns character attribute 1 on.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	c7	0	Character code (from 00 to 7F, FE, FF)	
		1		
6	c6	0		
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

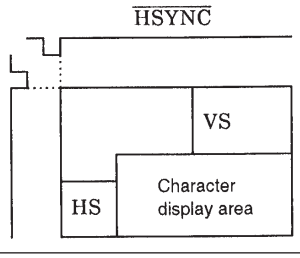
Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

③ COMMAND2: Vertical Display Position Setting Command

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 2 identification code: sets the vertical display position.	
6	—	0		
5	—	1		
4	—	0		
3	SZ21	0	SZ21 \ SZ20: 0 = Normal size, 1 = Double size; 1 = Triple size, 1 = Normal size	Character size for the second line
		1		
2	SZ20	0		
		1		
1	SZ11	0	SZ11 \ SZ10: 0 = Normal size, 1 = Double size; 1 = Triple size, 1 = Normal size	Character size for the first line
		1		
0	SZ10	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	—	0		
5	VP5 (MSB)	0	The vertical display start position is given by $VS = H \times (\sum_{n=0}^{5} 2^n VPn)$ where H is the horizontal synchronization pulse period. 	The six bits VP0 to VP5 specify the vertical display start position. The weight of the lsb is 1 × H.
		1		
4	VP4	0		
		1		
3	VP3	0		
		1		
2	VP2	0		
		1		
1	VP1	0		
		1		
0	VP0 (LSB)	0		
		1		

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

④ COMMAND3: Horizontal Display Position Setting Command

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">The command 3 identification code:
sets the horizontal display position.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>0</td></tr>
<tr><td>5</td><td>—</td><td>1</td></tr>
<tr><td>4</td><td>—</td><td>1</td></tr>
<tr><td>3</td><td>SZB1</td><td>0
1</td><td rowspan="3"><table><tr><th>SZB1 \ SZB0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Normal size</td><td>Double size</td></tr><tr><td>1</td><td>Triple size</td><td>Normal size</td></tr></table></td><td rowspan="3">The character size for the eleventh line.</td></tr>
<tr><td>2</td><td>SZB0</td><td>0
1</td></tr>
<tr><td>1</td><td>SZ91</td><td>0
1</td></tr>
<tr><td>0</td><td>SZ90</td><td>0
1</td><td><table><tr><th>SZ91 \ SZ90</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Normal size</td><td>Double size</td></tr><tr><td>1</td><td>Triple size</td><td>Normal size</td></tr></table></td><td>The character size for the ninth line.</td></tr>
</table>

Second byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td>Second byte identification code</td><td></td></tr>
<tr><td>6</td><td>—</td><td>0</td><td></td><td></td></tr>
<tr><td>5</td><td>HP5
(MSB)</td><td>0
1</td><td rowspan="6">The horizontal display start position is given by
$HS = Tc \times (\sum_{n=0}^{5} 2^{n}HPn)$
where Tc is the period of the OSCIN and OSCOUT oscillator in operating mode.</td><td rowspan="6">The six bits HP0 to HP5 specify the vertical display start position.
The weight of the lsb is 1 x Tc.</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>0</td><td>HP0
(LSB)</td><td>0
1</td></tr>
</table>

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

⑤ COMMAND4: Display Control Setting Command 1

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">The command 4 identification code:
sets display control parameters.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>1</td></tr>
<tr><td>5</td><td>—</td><td>0</td></tr>
<tr><td>4</td><td>—</td><td>0</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">RST_{SYS}</td><td>0</td><td></td><td rowspan="2">This reset occurs when the $\overline{CS}$ pin goes low, and the reset state cleared when the $\overline{CS}$ pin goes high.</td></tr>
<tr><td>1</td><td>Resets all registers. (Clears all registers to 0.)</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">RAM_{ERS}</td><td>0</td><td></td><td rowspan="2">The RAM erase function requires at least 500 µs.
It is executed on DSPOFF.</td></tr>
<tr><td>1</td><td>Erases display RAM. (Sets display RAM to FF (hexadecimal).)</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">OSC_{STP}</td><td>0</td><td>Continues crystal oscillator operation.</td><td rowspan="2">Only valid with character display off if external synchronization is used.</td></tr>
<tr><td>1</td><td>Stops the crystal oscillator.</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">RND_{SEL}</td><td>0</td><td>Turns off rounding.</td><td rowspan="2">Only valid for double and triple size characters.</td></tr>
<tr><td>1</td><td>Turns on rounding.</td></tr>
</table>

Second byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td colspan="2">Second byte identification code</td><td></td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">INT/NON</td><td>0</td><td colspan="2">Interlaced</td><td rowspan="2">Switches between interlaced and non-interlaced display.</td></tr>
<tr><td>1</td><td colspan="2">Non-interlaced</td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">BLK1</td><td>0</td><td colspan="2" rowspan="4"><table><tr><th>BLK1 \ BLK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blanking off</td><td>Character size blanking</td></tr><tr><td>1</td><td>Frame size blanking</td><td>Total area blanking</td></tr></table></td><td rowspan="4">Changes the blanking size.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BLK0</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">BK1</td><td>0</td><td colspan="2">Flashing period about 0.5 s</td><td rowspan="2">Sets the flashing period.</td></tr>
<tr><td>1</td><td colspan="2">Flashing period about 1 s</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">ATS</td><td>0</td><td colspan="2">Highlight function</td><td rowspan="2">Selects at2.</td></tr>
<tr><td>1</td><td colspan="2">Flashing function</td></tr>
<tr><td>1</td><td>—</td><td>0</td><td colspan="2"></td><td></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">DSPON</td><td>0</td><td colspan="2">Character display off</td><td rowspan="2">Turns character output on and off.</td></tr>
<tr><td>1</td><td colspan="2">Character display on</td></tr>
</table>

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

⑥ COMMAND5: Display Control Setting Command 2

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td colspan="2" rowspan="4">The command 5 identification code:
sets display control parameters.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>1</td></tr>
<tr><td>5</td><td>—</td><td>0</td></tr>
<tr><td>4</td><td>—</td><td>1</td></tr>
<tr><td rowspan="6">3</td><td rowspan="6">PH2</td><td rowspan="2">0</td><td colspan="2" rowspan="10"><table><tr><th rowspan="2">PHASE 2</th><th rowspan="2">PHASE 1</th><th rowspan="2">PHASE 0</th><th colspan="2">Background color (phase)</th></tr><tr><th>NTSC</th><th>PAL</th></tr><tr><td>0</td><td>0</td><td>0</td><td>π/2</td><td>±π/2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>In phase</td><td>In phase</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3 π/2</td><td>∓π/2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>π</td><td>±π</td></tr><tr><td>1</td><td>0</td><td>0</td><td>3 π/4</td><td>±3 π/4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>π/4</td><td>±π/4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>7 π/4</td><td>∓π/4</td></tr><tr><td>1</td><td>1</td><td>1</td><td>5 π/4</td><td>∓3 π/4</td></tr></table></td><td rowspan="10">Sets the phase of the background color for color burst.sz</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">PH1</td><td rowspan="2">0</td></tr>
<tr><td rowspan="2">1</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">PH0</td></tr>
<tr><td rowspan="2">0</td></tr>
<tr><td rowspan="2">1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">INT/EXT</td><td>0</td><td colspan="2">External synchronization mode</td><td rowspan="2">Switches between internal and external synchronization.</td></tr>
<tr><td>1</td><td colspan="2">Internal synchronization mode</td></tr>
</table>

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	TST	0	Normal operation	Test mode should not be used. This bit should always be zero.
		1	Test mode	
5	CHAL	0	Sets the character intensity level to about 85 IRE (bright white).	Switches the character intensity level.
		1	Sets the character intensity level to about 72 IRE (white with a touch of grey).	
4	BKL	0	Sets the blanking intensity level to about 3 IRE (a deep black as a frame level).	Switches the blanking intensity level.
		1	Sets the blanking intensity level to about 13 IRE (a dark grey as a frame level).	
3	RSL1	0	RSL1 = 0, RSL0 = 0: About 15 IRE, Amplitude About 60 IRE RSL1 = 0, RSL0 = 1: About 30 IRE, Amplitude About 60 IRE RSL1 = 1, RSL0 = 0: About 45 IRE, Amplitude About 60 IRE RSL1 = 1, RSL0 = 1: About 55 IRE, Amplitude About 65 IRE	Switches the background intensity level.
		1		
2	RSL0	0		
		1		
1	CV_{outmt}	0	Normal CV_{out} output	
		1	CV_{out} pedestal level output	
0	$XTAL_{sel}$	0	Selects XTAL1	Switches the oscillator circuit
		1	Selects XTAL2	

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

⑦ COMMAND6: Display Control Setting Command 3

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 6 identification code: sets display control parameters.	
6	—	1		
5	—	1		
4	—	0		
3	MOD3	0	Sets Fsc to 3.58 MHz.	The logical or of this bit and the Fsc switching input pin (pin 14) is used.
		1	Sets Fsc to 4.43 MHz.	
2	MOD2	0	Sets the color mode to NTSC.	The logical or of this bit and the color mode switching input pin (pin 13) is used.
		1	Sets the color mode to PAL.	
1	MOD1	0	Sets the number of scan lines to 525 lines.	The logical or of this bit and the scan line count switching input pin (pin 12) is used.
		1	Sets the number of scan lines to 625 lines.	
0	MOD0	0	Sets the mode to a mode other than SECAM.	The logical or of this bit and the mode switching input pin (pin 11) is used.
		1	Sets the mode to SECAM mode.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	HALF INT	0	Normal mode	
		1	Half internal synchronous mode	
5	P14OUT SEL	0	Halftone output	Selects P14 (3.58/4.43) output.
		1	High output in internal synchronous mode	
4	SECAM SEL	0	In SECAM mode, only the character frame area is on.	Selects the CVCR “on” period.
		1	In SECAM mode, the entire character display area is on.	
3	IOS	0	Sets the mode setting pin to be an input pin.	Switches the input/output direction of the mode setting pins.
		1	Sets the mode setting pin to be an output pin.	
2	BCOL1	0	See BCOL1/BCOL0 table below	Determines whether a background color is displayed. (Only valid in internal synchronization mode.)
		1		
1	BCOL0	0		
		1		
0	CBOFF	0	Outputs a color burst signal.	Only valid when either BCOL0 is 1 or BCOL1 is 1.
		1	Stops the output of color burst signals.	

BCOL1	BCOL0	Background color
0	0	Background color displayed
0	1	No background color (about 13 IRE)
1	0	No background color (about 23 IRE)
1	1	CV_{outmt2} (CSYNC)

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

⑧ COMMAND70: Display Control Setting Command 4

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 7 identification code: sets display control parameters.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Expansion command 0 identification code	
2	—	0		
1	—	0		
0	LINS	0	Selects the lower 6 bits (bits 0 to 5)	Selects the upper or lower six bits when halftone output line mode is specified.
		1	Selects the upper 6 bits (bits 6 to B)	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification code	
6	VCO SELECT1	0	VCO frequency is 14.12 MHz	Selects VCO oscillation frequency.
		1	VCO frequency is 7.07 MHz	
5	LIN5	0	Turns off (low) sixth line halftone output.	Used for the line 12 setting when LINS is high.
		1	Turns on (high) sixth line halftone output.	
4	LIN4	0	Turns off (low) fifth line halftone output.	Used for the line 11 setting when LINS is high.
		1	Turns on (high) fifth line halftone output.	
3	LIN3	0	Turns off (low) fourth line halftone output.	Used for the line 10 setting when LINS is high.
		1	Turns on (high) fourth line halftone output.	
2	LIN2	0	Turns off (low) third line halftone output.	Used for the line 9 setting when LINS is high.
		1	Turns on (high) third line halftone output.	
1	LIN1	0	Turns off (low) second line halftone output.	Used for the line 8 setting when LINS is high.
		1	Turns on (high) second line halftone output.	
0	LIN0	0	Turns off (low) first line halftone output.	Used for the line 7 setting when LINS is high.
		1	Turns on (high) first line halftone output.	

Note: When the chip is reset by the $\overline{RST}$ pin, the register states (bits) are all cleared to 0.

⑨ COMMAND71: Display Control Setting Command 5

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 7 identification code: sets display control parameters	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Expansion command 1 identification code	
2	—	1		
1	—	0		
0	LINS	0	Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half-tone output line setting.
		1	Selects upper 6 bits (6 to B).	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	EGMODE 2SELECT	0	Normal display	
		1	Applies frame to inverted characters also.	
5	PORTSET SELECT2	0	Sets port output data	
		1	Sets port (output switching)	
4	PORTSET SELECT1	0	Sets port output data	
		1	Sets port (output switching)	
3	VMN SEL	0	Normal V signal	
		1	VMASK signal	
2	VINPsel	0	Normal I/O	
		1	V is input from P11.	
1	VNPsel	0	V rise detection	Selects V detection polarity.
		1	V fall detection	
0	VSEPsel	0	VSEP is about 9.3 µs.	Selects V separation time.
		1	VSEP is about 18.6 µs.	

Note: When the chip is reset by the $\overline{\text{RST}}$ pin, the register states (bits) are all cleared to 0.

⑩ COMMAND72: Display Control Setting Command 6

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 7 identification code: sets display control parameters	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Expansion command 2 identification code	
2	—	0		
1	—	0		
0	LINS	0	Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half-tone output line setting.
		1	Selects upper 6 bits (6 to B).	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	—	0		
3	MOD3 SEL	0	Normal MOD3 (P14) output (PS1 = 1)	Specifies port output data when PS1 = 0.
		1	Specifies MOD3 general port output	
2	MOD2 SEL	0	Normal MOD2 (P13) output (PS1 = 1)	Specifies port output data when PS1 = 0.
		1	Specifies MOD2 general port output	
1	MOD1 SEL	0	Normal MOD1 (P12) output (PS1 =1)	Specifies port output data when PS1 = 0.
		1	Specifies MOD1 general port output	
0	MOD0 SEL	0	Normal MOD0 (P11) output (PS1 = 1)	Specifies port output data when PS1 = 0.
		1	Specifies MOD0 general port output	

Note: When the chip is reset by the $\overline{\text{RST}}$ pin, the register states (bits) are all cleared to 0.

⑪ COMMAND73: Display Control Setting Command 7

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	The command 7 identification code: sets display control parameters	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Expansion command 3 identification code	
2	—	1		
1	—	0		
0	LINS	0	Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half tone output line setting.
		1	Selects upper 6 bits (6 to B).	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	—	0		
3	VCP SELECT2	0	No feedback resistance	Specifies VCO oscillator feedback resistance connection
		1	Feedback resistance	
2	SDETOUT SEL	0	Normal SOUT (P29) output (PS2 = 1)	Specifies port output data when PS2 = 0.
		1	Specifies SOUT general port output	
1	VOUT SEL	0	Normal VOUT (P7) output (PS2 =1)	Specifies port output data when PS2 = 0.
		1	Specifies VOUT general port output	
0	HOUT SEL	0	Normal HOUT (P4) output (PS2 = 1)	Specifies port output data when PS2 = 0.
		1	Specifies HOUT general port output	

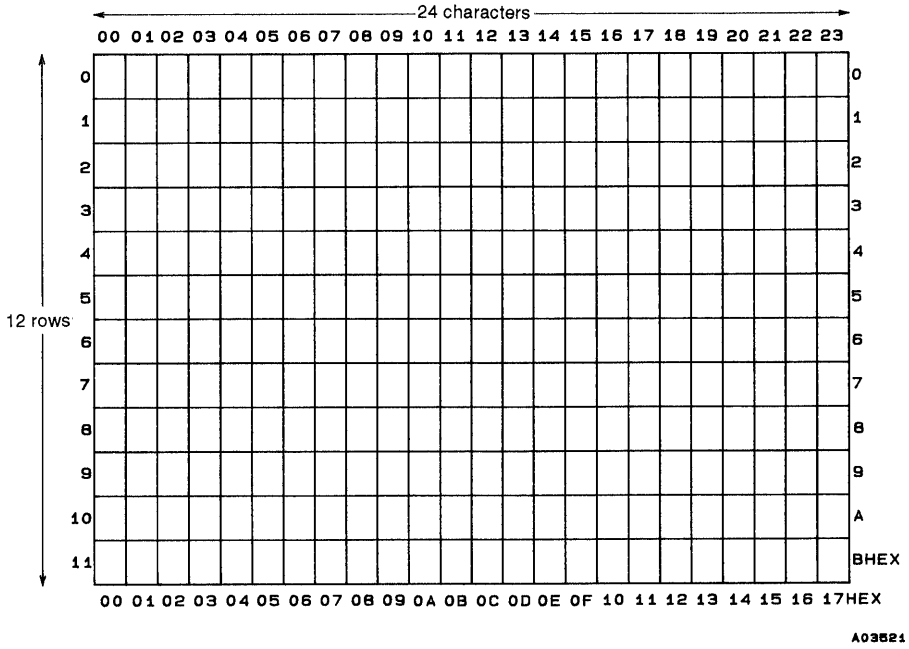
Note: When the chip is reset by the $\overline{\text{RST}}$ pin, the register states (bits) are all cleared to 0.

Display Configuration

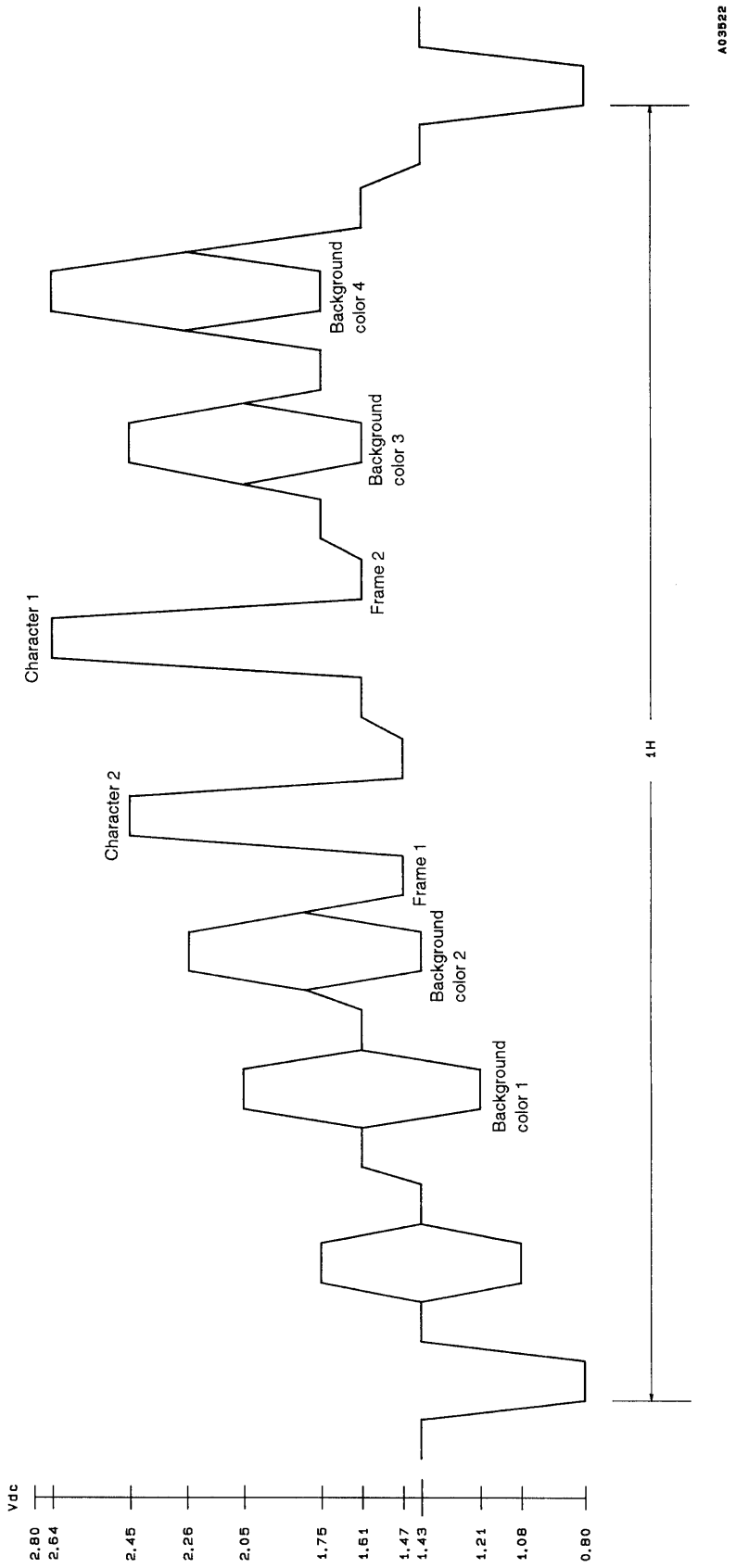
The display consists of 12 rows of 24 characters each. Up to 288 characters can be displayed unless enlarged characters are displayed. Display memory addresses are expressed as a row address in the range 0 to B (hexadecimal) and a column address in the range 0 to 17 (hexadecimal).

Display Configuration and Display Memory Addresses

24 characters by 12 rows



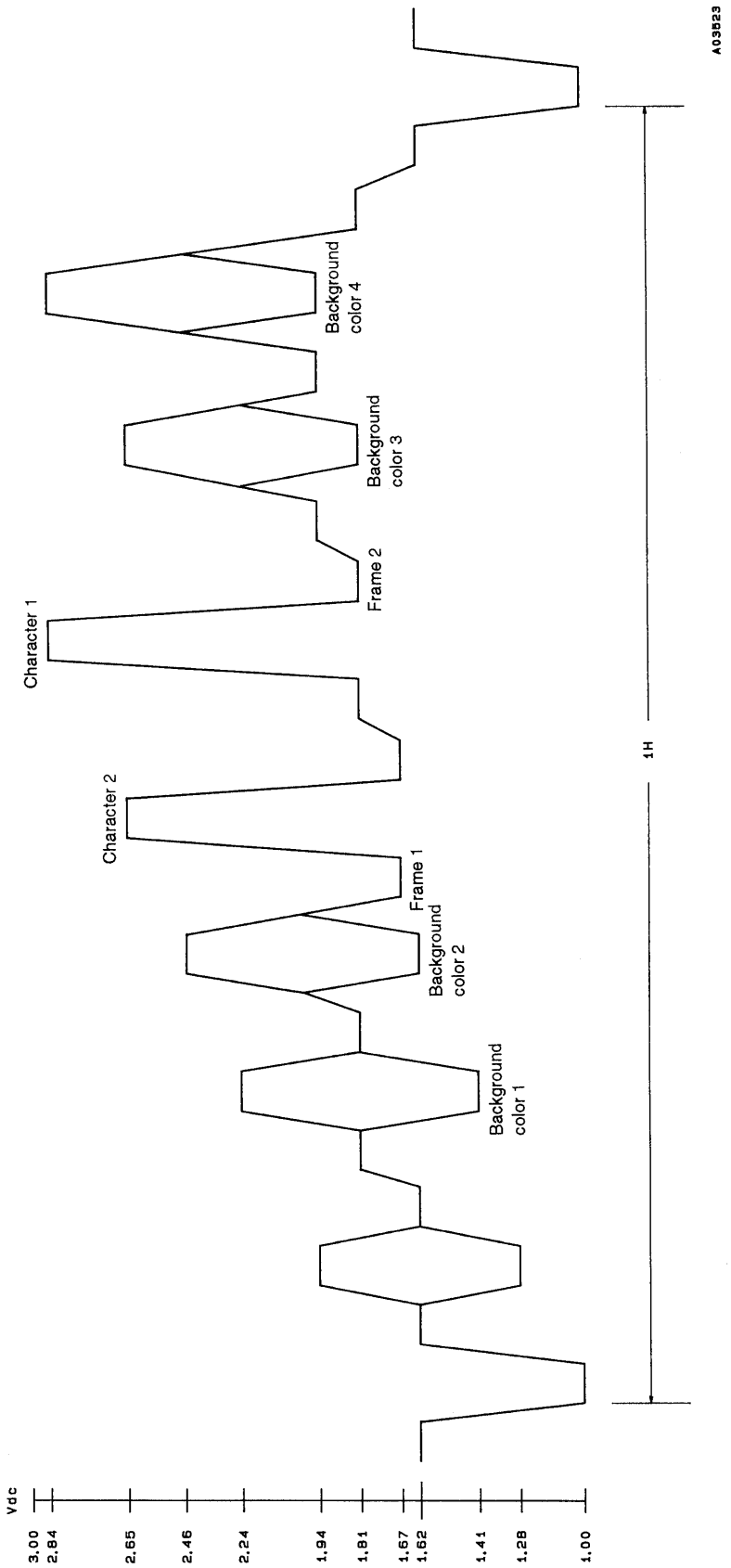
Composite Video Signal Output Levels (internally generated levels) Metal Option



Output level	Output voltage (VDC)
Character level 1	2.638
Character level 2	2.449
Background high level 2	2.262
Background high level 1	2.047
Burst high level	1.747
Frame level 2	1.610

Output level	Output voltage (VDC)
Frame level 1	1.465
Pedestal level	1.429
Background low level 1	1.212
Burst low level	1.080
Sync level	0.800

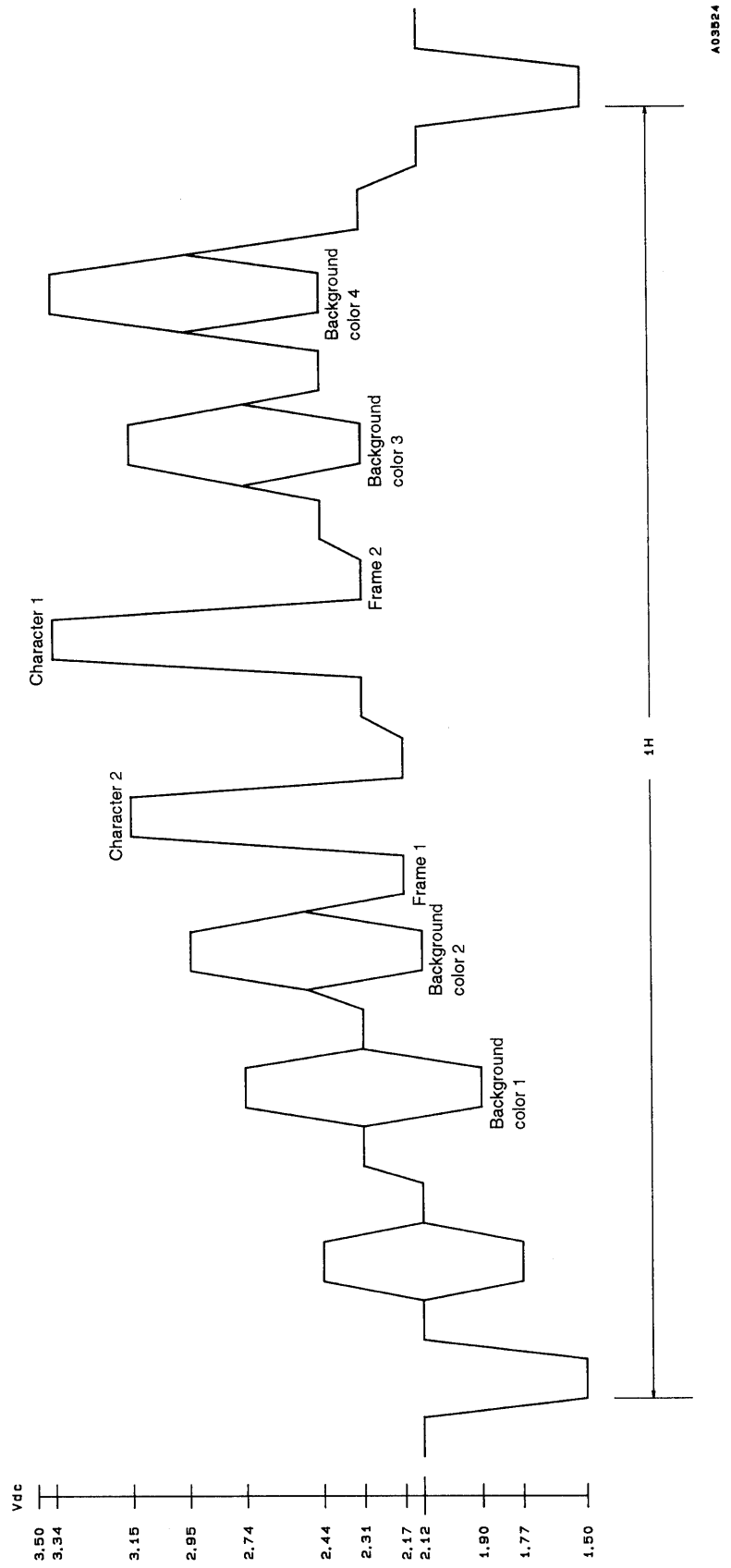
Composite Video Signal Output Levels (internally generated levels) Metal Option



Output level	Output voltage (VDC)
Character level 1	2.841
Character level 2	2.652
Background high level 2	2.456
Background high level 1	2.242
Burst high level	1.943
Frame level 2	1.811

Output level	Output voltage (VDC)
Frame level 1	1.665
Pedestal level	1.624
Background low level 1	1.407
Burst low level	1.275
Sync level	1.000

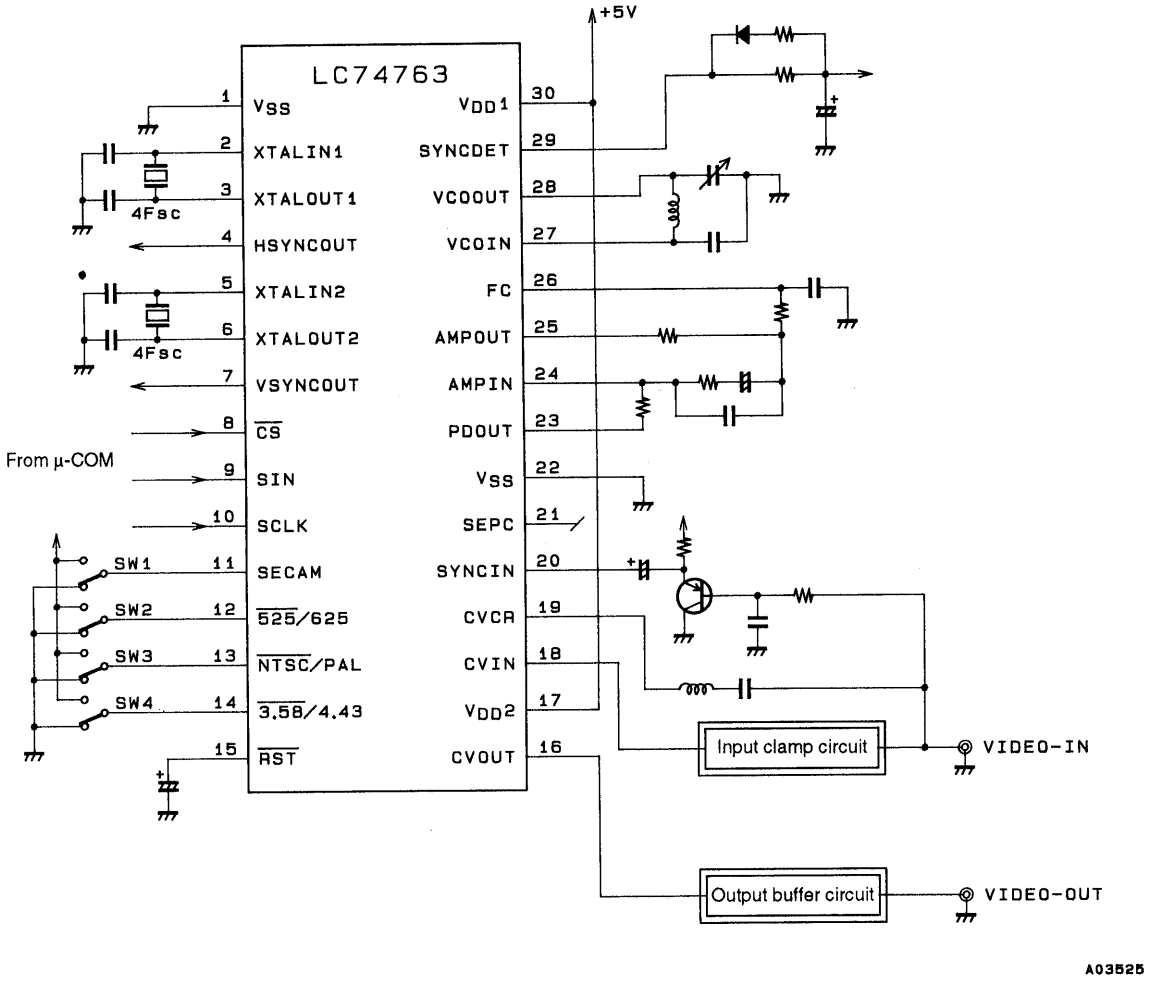
Composite Video Signal Output Levels (internally generated levels) Metal Option



Output level	Output voltage (VDC)
Character level 1	3.342
Character level 2	3.153
Background high level 2	2.950
Background high level 1	2.735
Burst high level	2.436
Frame level 2	2.312

Output level	Output voltage (VDC)
Frame level 1	2.166
Pedestal level	2.118
Background low level 1	1.902
Burst low level	1.770
Sync level	1.500

Application Circuit Diagram



Signal format	4 Fsc (MHz)
NTSC	3.579545 × 4
PAL	4.433618 × 4
SECAM	4.433618 × 4
PAL-M	3.575611 × 4
PAL-N	3.582056 × 4
NTSC4.43	4.433618 × 4
PAL60	4.433618 × 4

Signal format	SW1	SW2	SW3	SW4
NTSC	0	0	0	0
PAL	0	1	1	1
SECAM	1	(1)	(1)	(1)
PAL-M	0	0	1	0
PAL-N	0	1	1	0
NTSC4.43	0	0	0	1
PAL60	0	0	1	1

Note: Fix SW1 to SW4 to 0 when setting a mode by command.