Ordering number:ENN3885A

CMOS IC

LC7475

On-Screen Display Controller for PAL-Format Video

Overview

The LC7475 is a video display controller for superimposing text and low-level graphics onto a PAL-format television receiver. The LC7475 has 128 characters in internal ROM. Up to 288 characters can be displayed on a 12-line by 24-character display under microprocessor control.

The LC7475 features four vertical and four horizontal character dimensions and 64 vertical and 64 horizontal screen start positions. It also features a flashing enable bit for each character position.

The LC7475 operates from a 5 V supply and is available in 22-pin shrink DIPs.

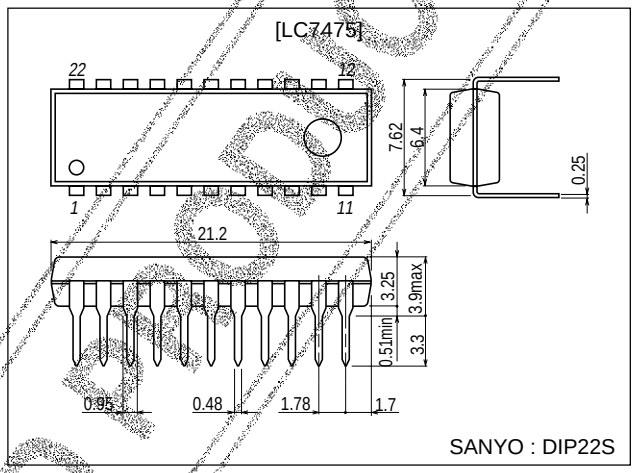
Features

- Complete text and graphics video overlay circuitry.
- 128 characters in internal ROM.
- 288 character display capability.
- 12 × 18 dot-matrix character resolution.
- Approximately 0.5 or 1 s period character flashing option.
- Selectable flashing duty cycles of 25, 50 or 75%.
- Internal or external synchronization.
- Serial data control.
- 5 V supply.
- 22-pin shrink DIP.

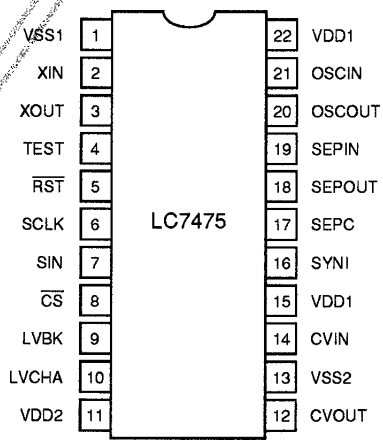
Package Dimensions

unit:mm

3059-DIP22S



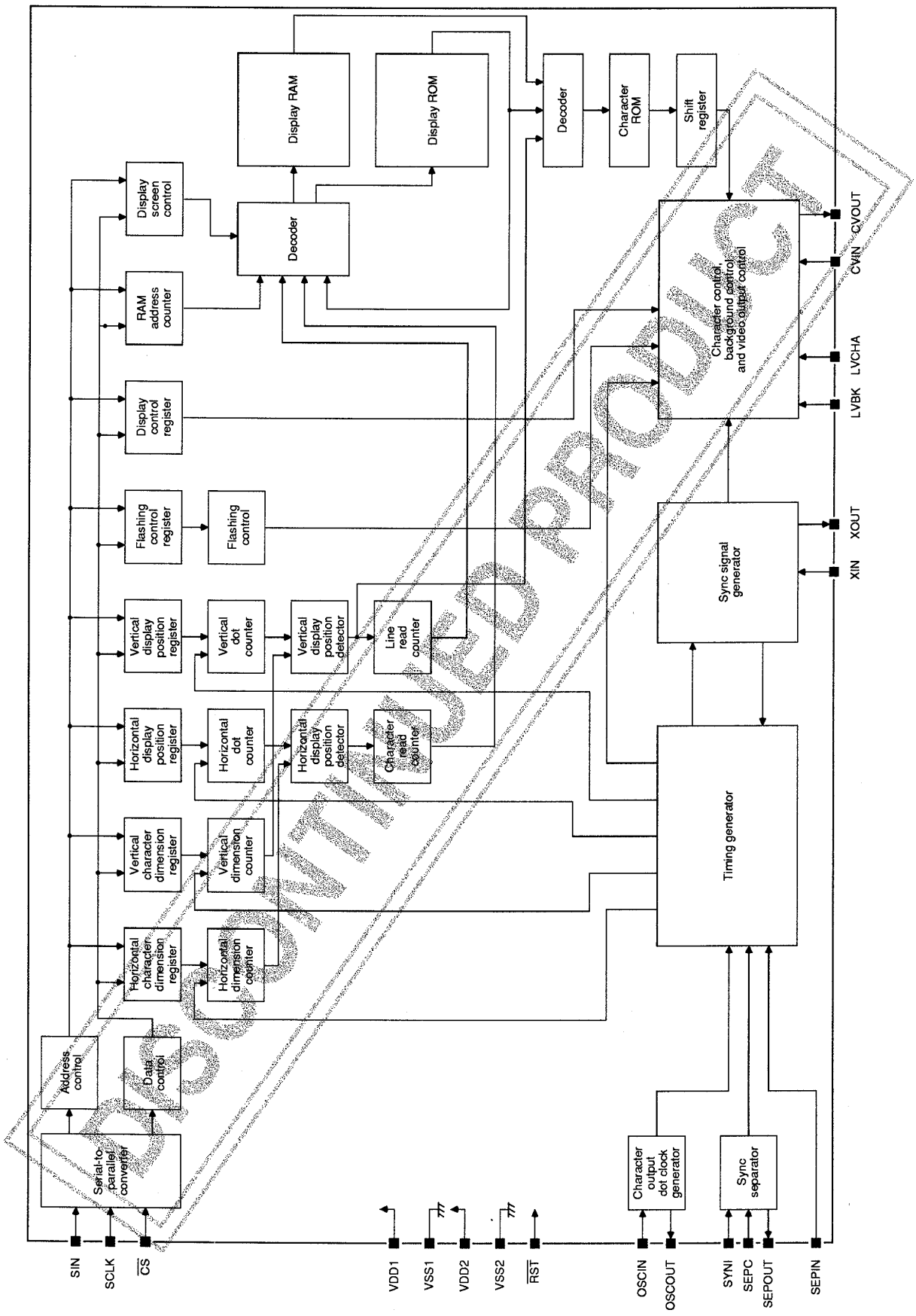
Pin Assignment



Top view

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Block Diagram



Pin Description

Number	Name	Description
1	V_{SS1}	Digital circuit ground
2	XIN	Crystal oscillator input
3	XOUT	Crystal oscillator output
4	TEST	Test output
5	$\overline{RST}$	Reset input
6	SCLK	Serial data clock input
7	SIN	Serial data input
8	$\overline{CS}$	Chip select input
9	LVBK	Blanking-level adjustment input
10	LVCHA	Cgaracter-level adjustment input
11	V_{DD2}	Analog circuit supply
12	CVOUT	Composite video output
13	V_{SS2}	Analog circuit ground
14	CVIN	Composite video input
15	V_{DD1}	Logic supply
16	SYNI	Sync separator input
17	SEPC	Sync separator adjustment input
18	SEPOUT	Sync separator output
19	SEPIN	Vertical sync input
20	OSCOUT	Dot clock oscillator output
21	OSCIN	Dot clock oscillator input
22	V_{DD1}	Logic supply

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{DD}		V_{SS}–0.3 to V_{SS}+7.0	V
Input voltage range	V_I		V_{SS}–0.3 to V_{DD}+0.3	V
Output voltage range	V_O		V_{SS}–0.3 to V_{DD}+0.3	V
Allowable power dissipation	Pd max		300(Ta=25˚C)	mW
Operating temperature	Topr		–30 to +70	˚C
Storage temperature	Tstg		–40 to +125	˚C

Recommended Operating Conditions at Ta = 25˚C

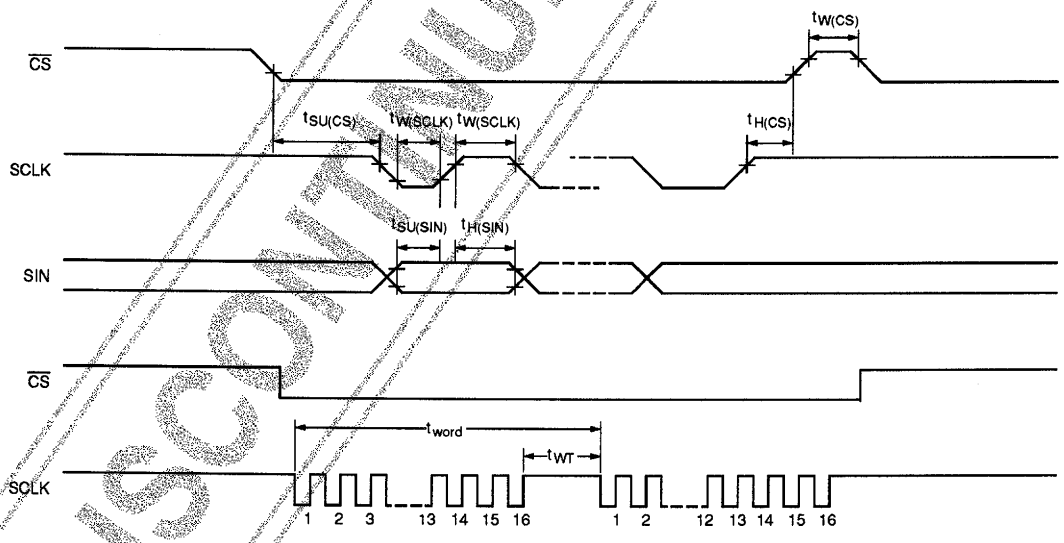
Parameter	Symbol	Conditions	Ratings	Unit
Logic supply voltage	V_{DD1}		5	V
Analog supply voltage	V_{DD2}		5	V
Logic supply voltage range	V_{DD1}		4.5 to 5.5	V
Analog supply voltage range	V_{DD2}		4.5 to 1.27V_{DD1}	V

Electrical Characteristics at Ta = –30 to +70˚C, V_{DD1} = 5V, V_{DD2} = 5V, unless otherwise noted

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{DD}				20	mA
SEPOUT low-level intput voltage	V_{IL1}	V_{DD1}=4.5V, I_{OL}=1mA			1.0	V
$\overline{CS}$, SIN, $\overline{RST}$ and SCLK low-level input voltage	V_{IL2}		V_{SS}–0.3		0.2V_{DD1}	V
SEPOUT high-level input voltage	V_{IH1}	V_{DD1}=4.5V, I_{OH}=1mA	3.5			V
$\overline{CS}$, SIN, $\overline{RST}$ and SCLK high-level input voltage	V_{IH2}		0.8V_{DD1}		V_{DD1}+0.3	V
SYNI composite video input voltage	V_{IN1}			2.0	2.5	V_{P-P}
CVIN composite video input voltage	V_{IN2}			2		V_{P-P}
$\overline{CS}$, SIN, $\overline{RST}$, SCLK and SEPIN high-level input current	I_{IH1}				1	µA
OSCIN high-level input current	I_{IH2}		1			µA
Sync generator input frequency	f_{OSC1}			17.73		MHz
Dot clock input frequency	f_{OSC2}		5	7	10	MHz
CVOUT leakage current	I_L				10	µA

Timing Characteristics at Ta = –30 to +75˚C, V_{DD1} = 5±0.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCLK input pulsewidth	$t_{W(SCLK)}$		200			ns
$\overline{CS}$ high-level input pulsewidth	$t_{W(CS)}$		1			µs
$\overline{CS}$ data enable input setup time	$t_{SU(CS)}$		200			ns
SIN data input setup time	$t_{SU(SIN)}$		200			ns
$\overline{CS}$ data enable input hold time	$t_{H(CS)}$		2			µs
SIN data input hold time	$t_{H(SIN)}$		200			ns
16-bit word write time	t_{word}		10			µs
RAM data write time	t_{WT}		1			µs



Input Timing

Data and address words are input in serial format on SIN. A 16-bit address word is input after the falling edge of $\overline{CS}$ followed by 16-bit data words. The address is incremented automatically after each data word. The data input timing is shown in figure 1.

Only the lower eight bits of the address word are significant. Only the lower eight bits of data words at addresses 000H to 0AFH, the lower 11 bits of data words at addresses 0B0H to 0BBH, and the lower 12 bits of data words at addresses 0BCH to 0BFH are significant. All non-significant bits should be set to 0.

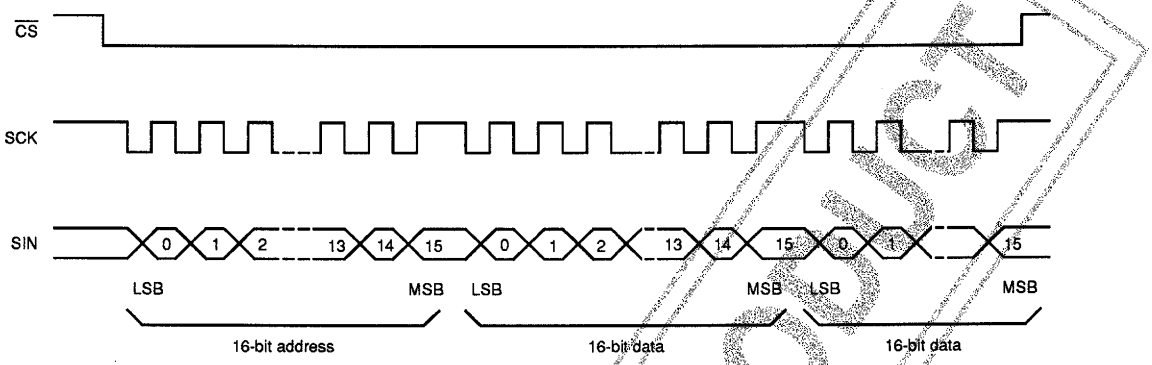


Figure 1. Input timing

RAM Memory Configuration

RAM memory is organized as 16-bit words as shown in table 1. Locations 000H to 0AFH are display RAM, locations 0B0H through to 0BBH are display line address registers, locations 0BCH to 0BDH are display control registers, location 0BEH is the video signal control register and location 0BFH is the general control register.

Table 1. Memory configuration

Address	Memory contents																Description
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
000H to 0AFH	0	0	0	0	0	0	0	0	FL	C_6	C_5	C_4	C_3	C_2	C_1	C_0	Display RAM with 7-bit character code and flashing enable bit
0B0H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 1 in line ROM
0B1H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 2 in line ROM
0B2H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 3 in line ROM
0B3H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 4 in line ROM
0B4H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 5 in line ROM
0B5H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 6 in line ROM
0B6H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 7 in line ROM
0B7H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 8 in line ROM
0B8H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 9 in line ROM
0B9H	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 10 in line ROM
0BAH	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 11 in line ROM
0BBH	0	0	0	0	×	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 12 in line ROM
0BCH	0	0	0	0	HSZ31	HSZ30	HSZ21	HSZ20	HSZ11	HSZ10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal character position and deimension
0BDH	0	0	0	0	VSZ31	VSZ30	VSZ21	VSZ20	VSZ11	VSZ10	VP5	VP4	VP3	VP2	VP1	VP0	Vertivcal character position and deimension
0BEH	0	0	0	0	$\overline{INT}$/ NON	×	$2f_{SC}$/ $4f_{SC}$	OSC STP	DSP ON	×	SYS RST	×	×	PH2	PH1	PH0	Video signal phase, display blanking, oscillator control and system reset selection
0BFH	0	0	0	0	TST MOD	×	×	BLK1	BLK0	×	FL2	FL1	FL0	EXT	CB OFF	BCOL	Character blanking, flashing, and test mode selection

Note

× = don't care

Horizontal Display Control Register

The function of each bit in the horizontal display control register is shown in table 2. Note that all bits can be reset to 0 by a reset pulse on $\overline{RST}$.

Table 2. Horizontal display control register (0BCH)

Data bit	Name	Function
0	HP0	Selects the horizontal start position of hte display on the screen, HS, as given by the following equation $HS = T_C \times (4 \times \sum_{n=0}^{5} 2^n HPn)$ where T_C is the period of the dot clock oscillator. Note that HS increments in multiples of $4T_C$.
1	HP1	
2	HP2	
3	HP3	
4	HP4	
5	HP5	
6	HSZ10	Selects the horizontal dimension of characters in line 1 as shown in table 3
7	HSZ11	
8	HSZ20	Selects the horizontal dimension of characters in line 2 as shown in table 4
9	HSZ21	
A	HSZ30	Selects the horizontal dimension of characters in lines 3 to 12 as shown in table 5
B	HSZ31	
C	–	No function

Table 3. Horizontal dimension of characters in line 1

HSZ11	HSZ10	Horizontal dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

Table 4. Horizontal dimension of characters in line 2

HSZ21	HSZ20	Horizontal dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

Table 5. Horizontal dimension of characters in lines 3 to 12

HSZ31	HSZ30	Horizontal dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

Vertical Display Control Register

The function of each bit in the vertical display control register is shown in table 6. Note that all bits can be reset to 0 by a reset pulse on $\overline{RST}$.

Table 6. Vertical display control register (0BDH)

Data bit	Name	Function
0	VP0	Selects the vertical start position of hte display on the screen, VS, as given by the following equation $VS = H \times (4 \times \sum_{n=0}^{5} 2^n VPn)$ where H is the horizontal sync pulsewidth. Note that VS increments in multiples of 4 lines from line 0 to line 64
1	VP1	
2	VP2	
3	VP3	
4	VP4	
5	VP5	
6	VSZ10	Selects the vertical dimension of characters in line 1 as shown in table 7
7	VSZ11	
8	VSZ20	Selects the vertical dimension of characters in line 2 as shown in table 8
9	VSZ21	
A	VSZ30	Selects the vertical dimension of characters in lines 3 to 12 as shown in table 9
B	VSZ31	
C	–	No function

Table 7. Vertical dimension of characters in line 1

HSZ11	HSZ10	Vertical dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

Table 8. Vertical dimension of characters in line 2

HSZ21	HSZ20	Vertical dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

Table 9. Vertical dimension of characters in lines 3 to 12

VSZ31	VSZ30	Vertical dimension
0	0	$1T_C$/dot
0	1	$2T_C$/dot
1	0	$3T_C$/dot
1	1	$4T_C$/dot

The relationships between the vertical sync and horizontal sync pulses and between the horizontal and vertical display start positions are shown in figure 2.

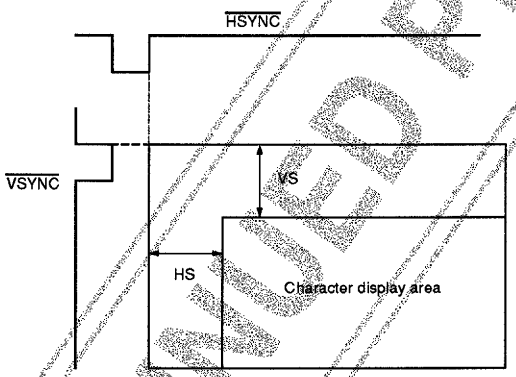


Figure 2. Vertical and horizontal sync pulses

Video Signal Control Register

The function of each bit in the video signal control register is shown in table 10. Note that all bits can be reset to 0 by a reset pluse on $\overline{RST}$.

Table 10. Video signal control register (0BEH)

Data bit	Name	Function
0	PH0	Selects the phase, and hence the background color, in the color burst as shown in table 11 and figure 3
1	PH1	
2	PH2	
3	–	No function
4	–	No function
5	SYS RST	Resets all registers and turns the display OFF when 1. Note that a system reset also occurs when $\overline{CS}$ goes LOW
6	–	No function
7	DSP ON	Selects character display OFF when 0, and ON, when 1
8	OSC STP	Allows the crystal oscillator and LC oscillator to be turned OFF when 1, and prevents this, when 0. Note that external synchronization is effective only when the character display is OFF
9	$\overline{2f_{SC}}/4f_{SC}$	Selects a clock frequency of $2f_{SC}$ when 0, and $4f_{SC}$, when 1
A	–	No function
B	$\overline{INT}$/NON	Selects 312.5 lines/field, interlaced display when 0, and 313 lines/field, non-interlaced display, when 1
C	–	No function

Table 11. Phase selection

PH2	PH1	PH0	Phase	Color
0	0	0	±π/2	Cyan
0	0	1	0	Yellow
0	1	0	±π/2	Red
0	1	1	±π	Blue
1	0	0	±3π/4	Blue-cyan
1	0	1	±π/4	Green
1	1	0	±π/4	Red-yellow
1	1	1	±3π/4	Magenta

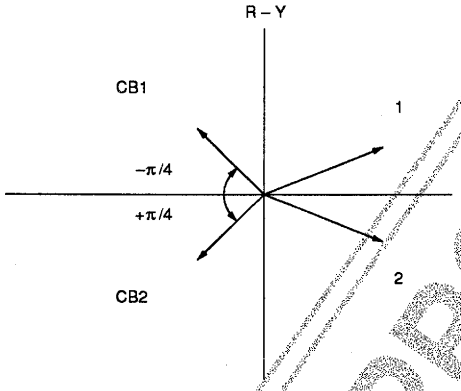


Figure 3. Background color-phase vector diagram

General Control Register

The function of each bit in the general control register is shown in table 12. Note that all bits can be reset to 0 by a reset pulse on $\overline{RST}$.

Table 12. General control register

Data bit	Name	Function
0	BCOL	Selects background color ON when 0 (valid for internal synchronization only), and 0FF, when 1
1	CB OFF	Selects the color burst when 0, or when 1 and BCOL is 1
2	EXT	Selects external horizontal and vertical synchronization when 0, and internal, when 1
3	FL0	Selects the display flashing duty cycle as shown in table 13
4	FL1	
5	FL2	Selects a flashing period of approximately 1 s when 0, and of approximately 0.5 s, when 1
6	–	No function
7	BLK0	Selects the blanking area of the display as shown in table 14
8	BLK1	
9	–	No function
A	–	No function
B	TST MOD	Selects normal operation when 0, and test mode, when 1. Note that test mode should not be selected during normal operation
C	–	No function

Table 13. Flashing duty cycle selection

FL1	FL0	Duty cycle
0	0	Flashing OFF
0	1	25%
1	0	50%
1	1	75%

Table 14. Blanking area selection

BLK1	BLK0	Blanking area
0	0	Blanking OFF
0	1	Character size
1	0	Frame size
1	1	Total area

Line ROM Configuration

The line ROM is configured as 1,536 words from address 000H to 5FFH as shown in table 15. Each word comprises a 16-bit address code and a single control bit. When the control bit is 0, the 7-bit character code is significant and is used to address the character ROM, and when 1, the 7-bit character code in ROM is ignored and the character code is read from display RAM. The display RAM address is incremented automatically by one each time a character code is read from RAM. Note that your local SANYO representative can offer advice on how to specify character ROM.

Table 15. Line ROM configuration

Address	Video signal control bits																Description
	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0	
000H	0	0	0	0	0	0	0	0	$\overline{\text{ROM}}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 1
to																	
017H	0	0	0	0	0	0	0	0	$\overline{\text{ROM}}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of twenty-fourth character of line 1
018H	0	0	0	0	0	0	0	0	$\overline{\text{ROM}}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of first character of line 2
to																	
5FFH	0	0	0	0	0	0	0	0	$\overline{\text{ROM}}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Address of twenty-fourth character of line 64

The function of each significant bit in a line ROM word is shown in table 16.

Table 16. Line ROM word data

Data bit	Name	Description
0	ADR0	Specifies the character ROM address. ADR0 to ADR6 should be set to 0 when bit 7 is 1
1	ADR1	
2	ADR2	
3	ADR3	
4	ADR4	
5	ADR5	
6	ADR6	
7	$\overline{\text{ROM}}$/RAM	Selects direct ROM addressing
		Selects indirect ROM addressing from RAM.

The line addresses in line ROM are shown in table 17.

Table 17. Line ROM addresses

Line	Address(hex)	Line	Address(hex)	Line	Address(hex)	Line	Address(hex)
1	00	17	180	33	300	49	480
2	18	18	198	34	318	50	498
3	30	19	1B0	35	330	51	4B0
4	48	20	1C8	36	348	52	4C8
5	60	21	1E0	37	360	53	4E0
6	78	22	1F8	38	378	54	4F8
7	90	23	210	39	390	55	510
8	A8	24	228	40	3A8	56	528
9	C0	25	240	41	3C0	57	540
10	D8	26	258	42	3D8	58	558
11	F0	27	270	43	3F0	59	570
12	108	28	288	44	408	60	588
13	120	29	2A0	45	420	61	5A0
14	138	30	2B8	46	438	62	5B8
15	150	31	2D0	47	450	63	5D0
16	168	32	2E8	48	468	64	5E8

Screen Configuration

The character screen display is configured as 12 lines × 24 characters, making a maximum number of 288 characters when the smallest character size is used. The number of characters that can be displayed reduces as character size is increased. The character screen configuration is shown in table 18.

Table 18. Screen configuration

Line	Character number																							
1	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
2	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
4	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
5	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
6	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
7	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
8	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
9	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
10	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
11	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
12	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

The start address for each of the twelve display lines is specified in the display line address registers in RAM. An example arrangement of ROM and RAM addresses is shown in table 19. Note how both the RAM and ROM addresses increment.

Table 19. Example ROM and RAM configuration

Line	Character RAM and ROM configuration (hex)																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 00	ROM 01	ROM 02	ROM 03	ROM 04	ROM 05	ROM 06	ROM 07	ROM 08	ROM 09	ROM 0A	ROM 0B	ROM 0C	ROM 0D	ROM 0E	ROM 0F	RAM 00	RAM 01	RAM 02	RAM 03	RAM 04	RAM 05	ROM 16	ROM 17
2	ROM 18	RAM 06	RAM 07	RAM 08	RAM 09	ROM 1D	ROM 1E	ROM 1F	ROM 20	ROM 21	RAM 0A	RAM 0B	RAM 0C	RAM 0D	RAM 0E	RAM 0F	ROM 28	ROM 29	ROM 2A	ROM 2B	ROM 2C	ROM 2D	ROM 2E	ROM 2F
3	ROM 30	RAM 10	RAM 11	RAM 12	RAM 13	RAM 14	ROM 36	ROM 37	ROM 38	ROM 39	RAM 15	RAM 16	RAM 17	RAM 18	RAM 19	RAM 1A	RAM 1B	RAM 1C	RAM 1D	RAM 1E	ROM 44	ROM 45	ROM 46	ROM 47
4	ROM 48	ROM 49	ROM 4A	ROM 4B	ROM 4C	RAM 1F	RAM 20	RAM 21	RAM 22	ROM 51	RAM 23	RAM 24	ROM 54	RAM 25	RAM 26	ROM 57	RAM 27	RAM 28	ROM 5A	ROM 5B	ROM 5C	ROM 5D	ROM 5E	ROM 5F
5	ROM 60	RAM 29	RAM 2A	RAM 2B	RAM 2C	RAM 2D	RAM 2E	RAM 2F	RAM 30	ROM 69	RAM 31	RAM 32	ROM 6C	RAM 33	RAM 34	ROM 6F	RAM 35	RAM 36	ROM 72	ROM 73	ROM 74	ROM 75	ROM 76	ROM 77
6	ROM 78	RAM 37	RAM 38	RAM 39	RAM 3A	RAM 3B	RAM 3C	RAM 3D	ROM 80	RAM 3E	RAM 3F	RAM 40	RAM 41	ROM 85	RAM 42	RAM 43	RAM 44	RAM 45	RAM 46	ROM 8B	RAM 47	RAM 48	ROM 8E	ROM 8F
7	RAM 49	RAM 4A	RAM 4B	RAM 4C	RAM 4D	RAM 4E	RAM 4F	RAM 50	RAM 51	RAM 52	RAM 53	RAM 54	ROM 9C	ROM 9D	ROM 9E	ROM 9F	ROM A0	ROM A1	ROM A2	ROM A3	ROM A4	ROM A5	ROM A6	ROM A7
8	RAM 55	RAM 56	RAM 57	RAM 58	RAM 59	RAM 5A	RAM 5B	RAM 5C	RAM 5D	RAM 5E	RAM 5F	RAM 60	ROM B4	ROM B5	ROM B6	ROM B7	ROM B8	ROM B9	ROM BA	ROM BB	ROM BC	ROM BD	ROM BE	ROM BF
9	ROM C0	ROM C1	ROM C2	ROM C3	ROM C4	ROM C5	ROM C6	ROM C7	ROM C8	ROM C9	ROM CA	ROM CB	RAM 61	RAM 62	RAM 63	RAM 64	RAM 65	RAM 66	RAM 67	RAM 68	RAM 69	RAM 6A	RAM 6B	RAM 6C
10	ROM D8	ROM D9	ROM DA	ROM DB	ROM DC	RAM 6D	RAM 6E	RAM 6F	RAM 70	RAM 71	RAM 72	RAM 73	RAM 74	RAM 75	RAM 76	RAM 77	RAM 78	RAM 79	RAM 7A	ROM EB	ROM EC	ROM ED	ROM EE	ROM EF
11	ROM F0	ROM F1	ROM F2	ROM F3	ROM F4	ROM F5	ROM F6	ROM F7	ROM F8	ROM F9	ROM FA	ROM FB	ROM FC	ROM FD	ROM FE	RAM 7B	RAM 7C	ROM 101	RAM 7D	RAM 7E	ROM 104	RAM 7F	RAM 80	ROM 107
12	RAM 81	RAM 82	RAM 83	RAM 84	RAM 85	RAM 86	RAM 87	RAM 88	RAM 89	RAM 8A	RAM 8B	RAM 8C	RAM 8D	RAM 8E	RAM 8F	RAM 90	RAM 91	RAM 92	RAM 93	RAM 94	RAM 95	RAM 96	RAM 97	ROM 11F

Composite Video Output

The character and background images are superimposed onto the composite video signal, which is shown in figure 4.

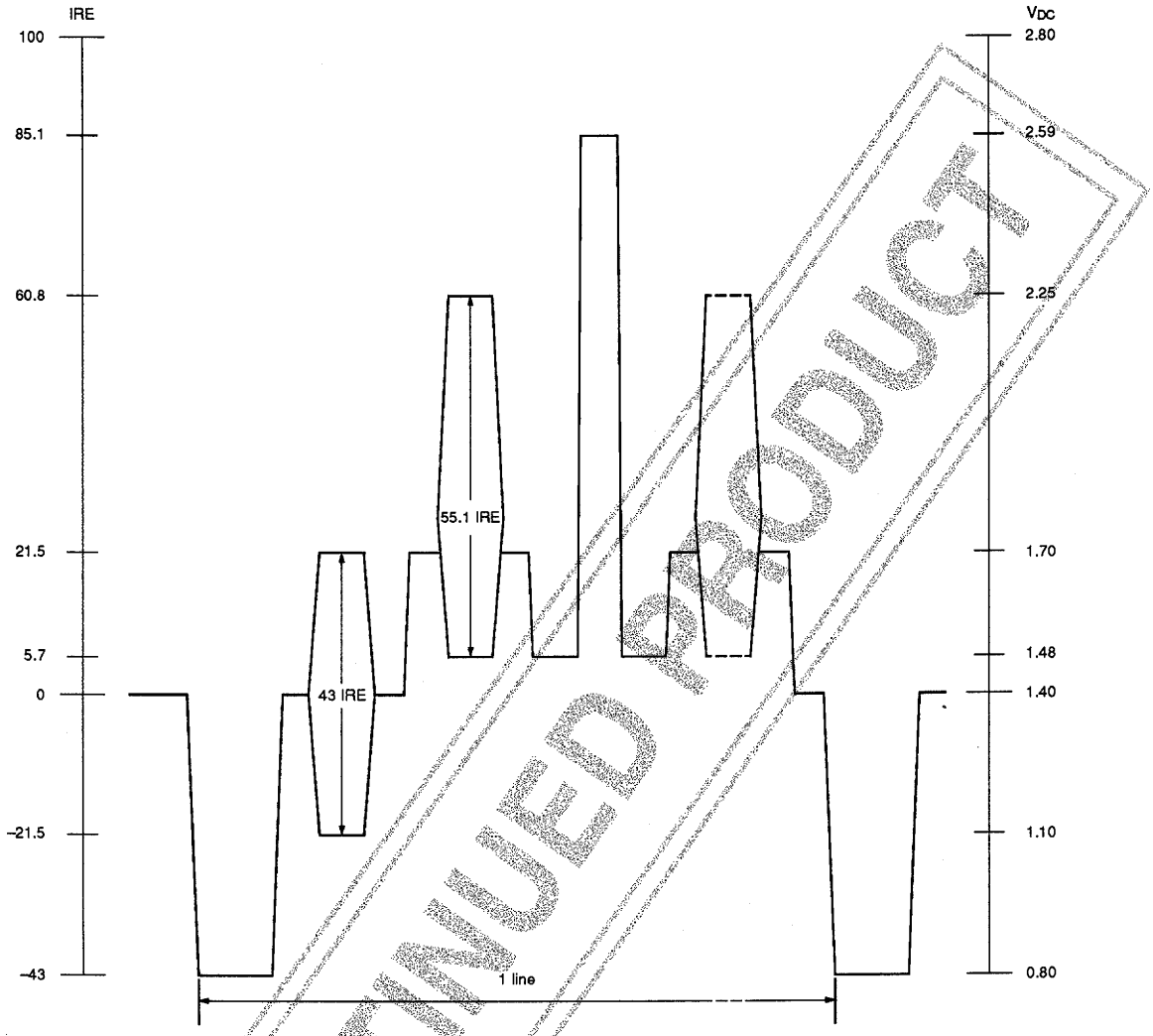


Figure 4. Composite video output waveform

The relative carrier amplitude and the corresponding DC voltage output amplitude are shown in table 20.

Table 20. Relative amplitude and DC output amplitude

Relative carrier amplitude (IRE)	Output voltage amplitude (V)
100.0	2.80
85.1	2.59
60.8	2.25
21.5	1.70
5.7	1.48
0	1.40
–21.5	1.10
–43.0	0.80

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products(including technical data,services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of July, 2001. Specifications and information herein are subject to change without notice.