

On-Screen Display Controller

Preliminary

Overview

The LC74735W is an on-screen display CMOS IC that displays characters and patterns on a TV screen.

For QVGA display, the LC74735W supports the use of both a 12×18 dot character font and a 12×18 dot graphics font with 16 colors with a total of 512 characters and glyphs.

For WVGA display, the LC74735W supports the use of both a 24×32 dot character font and a 12×16 dot graphics font with 16 colors with a total of 512 characters and glyphs.

The LC74735W can also implement extremely varied displays by the use of an external ROM.

The LC74735W supports both QVGA (480×234) and WVGA (800×480).

Features

- · Screen structure
 - Main:

QVGA mode: 40 characters × 13 lines (up to 520 characters) on a QVGA panel

WVGA mode: 33 characters × 15 lines (up to 495 characters) on a WVGA panel

- Wallpaper display screen: Permanent repetition of a 2×2 (horizontal × vertical) character pattern
- · Character structure
 - QVGA mode:

12 dots (horizontal) × 18 dots (vertical): Character

12 dots (horizontal) × 18 dots (vertical): Graphic glyph display

- WVGA mode:

24 dots (horizontal) × 32 dots (vertical): Character display

- 12 dots (horizontal) × 16 dots (vertical): Graphic glyph display (1 pixel: 2x2 dots)
- Character display clock: About 9 MHz QVGA with an LC oscillator
 - 33.2 MHz (maximum: 40 MHz) WVGA with an external clock signal input
- *: The ROM image is known when QVGA or WVGA mode is specified.
- Number of characters: 512 (internal) Up to 2048 characters when an external 16-bit 4M ROM is used.
- Character sizes: Four horizontal sizes (1x, 2x, 3x, and $4\times$)

Four vertical sizes $(1\times, 2\times, 3\times, \text{ and } 4\times)$

The character size is specified in line units.

• Display start positions: 512 positions in the horizontal direction and 256 positions in the vertical direction.

QVGA mode - WVGA mode

Setting units: Horizontal: 1 dot - 2 dots (In screen units)

Vertical: 1 dot - 2 dots (In screen units)

- Display functions
 - Blinking specification (In character units)

Period: 1/64, 1/32, and 1/16 of the vertical sync signal (In screen units)

Duty: Fixed at 50%

— Box (raised or recessed) display

Raised/depressed specification (In character units)

Left: Off/on specification (In character units)

Right: Off/on specification (In character units)

Top: Off/on specification (In character units)

Bottom: Off/on specification (In character units)

— Border specification (In line units): Only valid with glyphs from the character font.

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· Color specification

Character

- Character color (In character units): 1 of 16 colors can be specified.
- Character background color (In character units): 1 of 16 colors can be specified.
- Border color (In line units): 1 of 16 colors can be specified.
- Graphic
 - 16 types can be specified by ROM data
- Box color (line units): 1/16 cdors
- Background color (screen units): 1/16 colors
- Color table (palette)
 - Sixteen colors can be selected from a set of 512 colors (One of which is specified to be transparent.)
 - Number of color tables: 2. This allows up to 32 colors to be displayed at the same time.
- Wallpaper screen (Graphics glyphs only)

Wallpaper display: Repeated display under the main screen (2 characters horizontally by 2 characters vertically).

Sprite character display: Displayed above the main screen (2 characters horizontally by 2 characters vertically)

- Output
 - QVGA

Analog RGB output

BLK (OSD display period signal)

— WVGA

Digital RGB output (3 bits per color)

BLK (OSD display period signal)

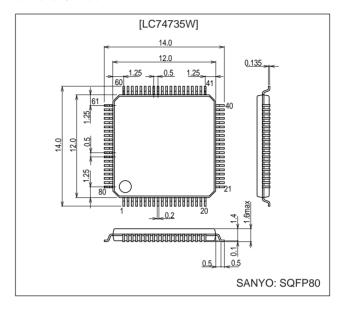
• Package: SQFP80

• Voltage: 3.3 V

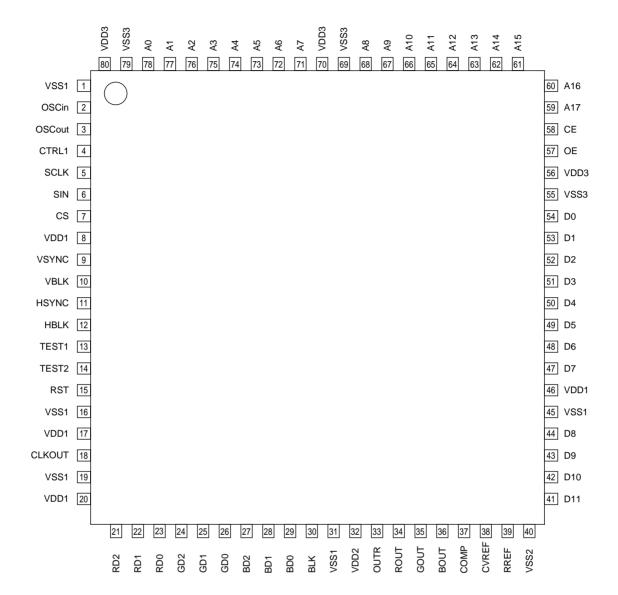
Package Dimensions

unit: mm

3220-SQFP80



Pin Assignment



Pin Functions

Pin No.	Symbol	Туре	Functional description
1	V _{SS} 1	Ground	Digital system ground
2	OSCin		Connections for the character output dot clock generator oscillator coil and capacitor.
3	OSCout	LC oscillator	May also be used for external clock input.
4	CTRL1	OSCin oscillator input control	Switches between external clock input mode and LC oscillator mode. Low: LC oscillator, high: external clock input MORE+
5	SCLK	Clock input	Clock input for the serial data input system MORE+ (This input has hysteresis characteristics.)
6	SIN	Data input	Serial data input MORE+ (This input has hysteresis characteristics.)
7	CS	Enable input	Enable input for the serial data input system. Serial data input is enabled when this pin is low. MORE+ (This input has hysteresis characteristics.)
8	VDD1	Power supply (+3.3 V)	Digital system power supply: +3.3 V
9	VSYNC	Vertical sync signal input	Vertical sync signal input MORE+ (This input has hysteresis characteristics.)
10	VBLK	Vertical blanking signal input	Vertical blanking signal input MORE+ (This input has hysteresis characteristics.)
11	HSYNC	Horizontal sync signal input	Horizontal sync signal input —— MORE+ (This input has hysteresis characteristics.)
12	HBLK	Horizontal blanking signal input	Horizontal blanking signal input MORE+ (This input has hysteresis characteristics.)
13	TEST1	Test mode control 1	Test mode control 1 Low: normal operation, high: test mode MORE+
14	TEST2	Test mode control 2	Test mode control 2 Low: normal operation, high: test mode (scan mode) MORE+
15	RST	Reset input	System reset input MORE+ (This input has hysteresis characteristics.)
16	VSS1	Ground	Digital system ground
17	VDD1	Power supply (+3.3 V)	Digital system power supply: +3.3 V
18	CLKOUT	Clock output	Clock output
19	VSS1	Ground	Digital system ground
20	VDD1	Power supply (+3.3 V)	Digital system power supply: +3.3 V
21	RD2	Rout output: bit 2	Pour output
22	RD1	Rout output: bit 1	Rout output This is a 3-bit digital output with values from 000 to 111.
23	RD0	Rout output: bit 0	The following standard and the standard
24	GD2	Gout output: bit 2	Gout output
25	GD1	Gout output: bit 1	This is a 3-bit digital output with values from 000 to 111.
26	GD0	Gout output: bit 0	
27	BD2	Bout output: bit 2	Bout output
28	BD1	Bout output: bit 1	This is a 3-bit digital output with values from 000 to 111.
29	BD0	Bout output: bit 0	
30	BLK	Blanking signal output	This signal indicates the OSD display period.
31	VSS1	Ground	Digital system ground
32	VDD2	Power supply (+3.3 V)	Analog system power supply: +3.3 V
33	Outr	outr output: analog	Output. Connect a resistor Ro (67 Ω) to this pin.
34	Rout	Rout output: analog	D/A converter (3 bits) output. Connect a resistor Ro (200 Ω) to this pin.
35	Gout	Gout output: analog	D/A converter (3 bits) output. Connect a resistor Ro (200 Ω) to this pin.
36	Bout	Bout output: analog	D/A converter (3 bits) output. Connect a resistor Ro (200 Ω) to this pin.
37	CCOMP	Phase correction capacitor connection	Capacitor connection: 1.5 μF
38	CVREF	Reference voltage output	Capacitor connection: 0.1 µF
39	RREF	Reference resistor connection	Resistor connection: ro, 1540 Ω
40	VSS2	Ground	D/A converter ground

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Pin No.	Symbol	Туре	Functional description
41	D11	Data input 11	ROM data input 11. MORE+
42	D10	Data input 10	ROM data input 10. MORE+
43	D9	Data input 9	ROM data input 9. MORE+
44	D8	Data input 8	ROM data input 8. MORE+
45	VSS1	Ground	Digital system ground
46	VDD1	Power supply (+3.3 V)	Digital system power supply: +3.3 V
47	D7	Data input 7	ROM data input 7. MORE+
48	D6	Data input 6	ROM data input 6. MORE+
49	D5	Data input 5	ROM data input 5. MORE+
50	D4	Data input 4	ROM data input 4. MORE+
51	D3	Data input 3	ROM data input 3. MORE+
52	D2	Data input 2	ROM data input 2. MORE+
53	D1	Data input 1	ROM data input 1. MORE+
54	D0	Data input 0	ROM data input 0. MORE+
55	VSS3	Ground	External ROM output system ground
56	VDD3	Power supply (+3.3 or +5.5 V)	External ROM output system power supply
57	ŌĒ	Output enable	ROM output enable output. This is an active low output.
58	CE	Chip enable	ROM chip enable output. This is an active low output.
59	A17	Address output 17	ROM address output 17
60	A16	Address output 16	ROM address output 16
61	A15	Address output 15	ROM address output 15
62	A14	Address output 14	ROM address output 14
63	A13	Address output 13	ROM address output 13
64	A12	Address output 12	ROM address output 12
65	A11	Address output 11	ROM address output 11
66	A10	Address output 10	ROM address output 10
67	A9	Address output 9	ROM address output 9
68	A8	Address output 8	ROM address output 8
69	VSS3	Ground	External ROM output system ground
70	VDD3	Power supply (+3.3 or +5.5 V)	External ROM output system power supply
71	A7	Address output 7	ROM address output 7
72	A6	Address output 6	ROM address output 6
73	A5	Address output 5	ROM address output 5
74	A4	Address output 4	ROM address output 4
75	A3	Address output 3	ROM address output 3
76	A2	Address output 2	ROM address output 2
77	A1	Address output 1	ROM address output 1
78	A0	Address output 0	ROM address output 0
79	VSS3	Ground	External ROM output system ground
80	VDD3	Power supply (+3.3 or +5.5 V)	External ROM output system power supply

Specifications Maximum Ratings

Parameter	Symbol	Conditions	Rat	ings	Unit
Falameter	Symbol	Conditions	min	max	Offic
Supply voltage	V _{DD} 1	$V_{DD}1, V_{DD}2$	V _{SS} - 0.3	V _{SS} + 4.6	V
Supply voltage	V _{DD} 3	V _{DD} 3 (A0 to A17, CE, OE)	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V
Input voltage	V _{IN}	All input pins	$V_{SS} - 0.3$	$V_{DD}1 + 0.3$	V
Output voltage	V _{OUT} 1	RD2:0, GD2:0, BD2:0, and BLK outputs	$V_{SS} - 0.3$	$V_{DD}1 + 0.3$	V
Output voltage	V _{OUT} 2	A0 to A17, OE, CE outputs	$V_{SS} - 0.3$	$V_{DD}1 + 0.3$	V
Maximum power dissipation	Pdmax		_	230	mW
Operating temperature	Topg		-30	+85	°C
Storage temperature	Tstg		-40	+125	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions		Ratings		Unit	
Farameter	Symbol	Symbol		typ	max	Offile	
Supply voltage	V _{DD} 1	$V_{DD}1, V_{DD}2$	3.0	3.3	3.6	V	
Supply voltage	V _{DD} 3	V _{DD} 3	3.0	3.3	5.5	V	
	V _{IH} 1	CTRL1, TEST1, TEST2	0.7 V _{DD} 1	_	5.5	V	
High-level input voltage	V _{IH} 2	SCLK, SIN, CS, VSYNC, HSYNC, RST	0.8 V _{DD} 1		5.5	V	
	V _{IH} 3	D0 to D11	0.7 V _{DD} 1	_	5.5	V	
	V _{IL} 1	CTRL1, TEST1, TEST2	V _{SS} - 0.3	_	0.3 V _{DD} 1	V	
Low-level input voltage	V _{IL} 2	SCLK, SIN, CS, VSYNC, HSYNC, RST	V _{SS} - 0.3		0.2 V _{DD} 1	V	
	V _{IL} 3	D0 to D11	V _{SS} - 0.3		0.3 V _{DD} 1	V	
Oscillator frequency	F _{OSC1}	OSCin and OSCout oscillator pins (LC oscillator)	_	10	_	MHz	
	F _{OSC2}	OSCin, V _{DD} 1 = 3.3 V	_	33	40	MHz	
External clock input	V _{IN} 1	V _{DD} 1 = 3.3 V, CTRL1 = high	0.5	_	3.3	Vp-p	
	Vrefda	Reference voltage	_	1.1	_	V	
D/A (2 bit 2 cb)	Rfda	Output load resistance ROUT, GOUT, and BOUT	_	200	_	Ω	
D/A (3 bit 3 ch)	Rfbda	Output load resistance OUTR	_	67	_	Ω	
	Rref	Reference load resistor, RREF	_	1540	_	Ω	

Electrical Characteristics at $Ta=-30~to~+85^{\circ}C,\,V_{DD}=3.3~V$ unless otherwise specified.

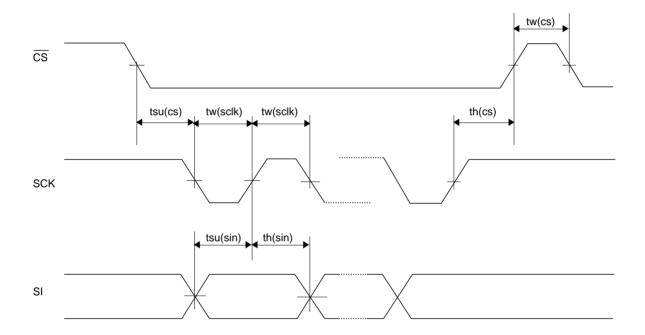
Parameter	Symbol	Pin	Conditions		Unit		
Farameter	Symbol	FIII	Conditions	min	typ	max	Offic
	V _{OH} 1	RD2:0, GD2:0, BD2:0, and BLK outputs	$V_{DD}1 = 3.0 \text{ V}$ $I_{OH}1 = -8 \text{ mA}$	V _{DD} 1 – 0.8	_	_	V
High-level output voltage	V _{OH} 2	A0:17, OE, and CE	$V_{DD}3 = 3.0 \text{ V}$ $I_{OH}2 = -8 \text{ mA}$	V _{DD} 3 – 0.8	_	_	٧
	V _{OH} 3	A0:17, OE, and CE	$V_{DD}3 = 4.5 \text{ V}$ $I_{OH}3 = -8 \text{ mA}$	V _{DD} 3 – 0.8	_	_	٧
	V _{OL} 1	RD2:0, GD2:0, BD2:0, and BLK outputs	V _{DD} 1 = 3.0 V I _{OL} 1 = 8 mA	_	_	0.4	٧
Low-level output voltage	V _{OL} 2	A0:17, OE, and CE	$V_{DD}3 = 3.0 \text{ V}$ $I_{OL}2 = 8 \text{ mA}$	_	_	0.4	V
	V _{OL} 3	A0:17, OE, and CE	$V_{DD}3 = 4.5 \text{ V}$ $I_{OL}3 = 8 \text{ mA}$	_	_	0.4	٧
	I _{IH} 1	CTRL1, TEST1, TEST2, SCLK, SIN, CS, VSYNC, HSYNC, RST	$V_{IN} = V_{DD}1$	_	_	10	μA
Input current	I _{IH} 2	D0:11	$V_{IN} = V_{DD}3$	_	_	10	μA
input current	I _{IL} 1	CTRL1, TEST1, TEST2, SCLK, SIN, CS, VSYNC, HSYNC	V _{IN} = V _{SS}	-10	_	_	μA
	I _{IL} 2	D0:11	V _{IN} = V _{SS}	-10	_	_	μA
	I _{DD} 1	V _{DD} 1	All outputs open OSCin: 40 MHz	_	_	37	mA
Operating current drain	I _{DD} 2	V _{DD} 2	D/A on	_	_	22	mA
	I _{DD} 3	V _{DD} 3		_	_	20	mA
	CLK	Clock frequency		_	_	20	MHz
D/A	Vmax	Maximum output voltage	V _{DD} 2 = 3.3 V	_	1	_	V
	Vmin	Minimum output voltage	V _{DD} 2 = 3.3 V	_	0	_	V

Timing Characteristics

OSD Write (See figure 1.) at Ta=-30 to $+85^{\circ}C,\,V_{DD}1=3.3\pm0.3~V$

Parameter	Symbol	Conditions		Unit		
Farameter	Symbol		min	typ	max	Offic
Minimum input pulse width	tw (sclk)	SCK	200	_	_	ns
williman input puise width	tw (cs)	CSB (The period CS is high)	1	_	_	μs
Data setup time	tsu (cs)	CSB	200	_	_	ns
Data setup time	tsu (sin)	SI	200	_	_	ns
Data hold time	th (cs)	CSB	2	_	_	μs
Data Hold time	th (sin)	SI	200	_	_	ns
One word write time	tword	The time to write 8 bits of data	4.2	_	_	μs
One word write tille	twt	RAM data write time	1	_	_	μs

Supplementary Materials



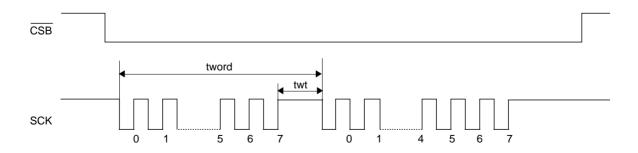
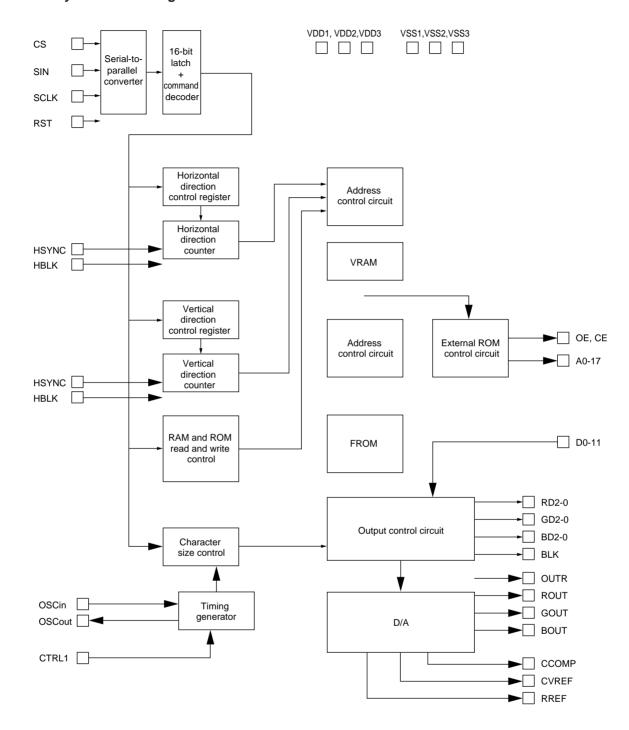


Figure 1 OSD Serial Data Input Timing

LC74735W System Block Diagram



Display Control Commands

The display control commands have serial input format that consists of 8-bit units transmitted LSB first. A commands consists of a command identification code in the first byte and data in the second and following bytes. Both a first byte and a second byte (16 bits) must be transmitted for each command. Commands 10, 11, and 71 set the IC to continuous write mode. (Continuous write mode is cleared by setting the CS pin high.)

Display Control Command Table

				First	t byte							Secor	nd byte			
Command	Comn	nand ide	ntification	code		D	ata					Da	ata			
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND00 (Write address) Main	1	0	0	0	0	0	V3	V2	V1	V0	H5	H4	НЗ	H2	H1	H0
COMMAND01 (Write address) Sub (Wallpaper)	1	0	0	0	0	1	0	0	0	SV0	0	0	0	0	0	SH0
	1	0	0	1	0	0	RM2	RM1(1)	0	0	at	BXS	BXL	BXR	BXU	BXD
Command 10 (Character write)								(2)	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
Main								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
								(4)	C7	C6	C5	C4	C3	C2	C1	C0
	1	0	0	1	0	1	RM2	RM1(1)	0	0	0	0	0	0	0	0
Command 11 (Character write)								(2)	0	0	0	0	0	0	0	0
Sub (Wallpaper)								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
								(4)	C7	C6	C5	C4	C3	C2	C1	C0
COMMAND20 (System control)	1	0	1	0	0	0	0	0	TSTMD2	TSTMD1	Q/W2	Q/W1	SYSRST	CTERS	SRMERS	MRMERS
COMMAND21 (Display control)	1	0	1	0	0	0	0	1	LCSOFF	BK1	BK0	SBG1	SBG0	DSPBG	DSPGS	DSPGM
COMMAND22 (I/O polarity control)	1	0	1	0	0	0	1	0	BLD1	BLO0	BLOP	BLO1	BLO0	CKP	VIP	HIP
COMMAND23 (Screen background color)	1	0	1	0	0	0	1	1	0	0	BGCT1	BGCT0	BGC3	BGC2	BGC1	BGC0
COMMAND24 (I/O polarity control 2)	1	0	1	0	0	1	0	0	DSPMD1	DSPMD0	DASEL	VBLKON	HBLKON	CKOP	VPB	HPB
COMMAND25 (Output control 3)	1	0	1	0	0	1	0	1	0	0	0	OTM2	OTM1	OTM0	QRM1	QRM0
COMMAND30 (Vertical display start position: main)	1	0	1	1	0	0	0	0	VPM7	VPM6	VPM5	VPM4	VPM3	VPM2	VPM1	VPM0
COMMAND31 (Horizontal display start position: main)	1	0	1	1	0	0	1	HPM8	HPM7	HPM6	HPM5	HPM4	НРМ3	HPM2	HPM1	НРМ0
COMMAND32 (Vertical display start position: sub)	1	0	1	1	0	1	0	0	VPS7	VPS6	VPS5	VPS4	VPS3	VPS2	VPS1	VPS0
COMMAND33 (Horizontal display start position: sub)	1	0	1	1	0	1	1	HPS8	HPS7	HPS6	HPS5	HPS4	HPS3	HPS2	HPS1	HPS0
COMMAND34 (Vertical display start position: screen)	1	0	1	1	1	0	0	0	VPG7	VPG6	VPG5	VPG4	VPG3	VPG2	VPG1	VPG0
COMMAND35 (Horizontal display start position: screen)	1	0	1	1	1	0	1	HPG8	HPG7	HPG6	HPG5	HPG4	HPG3	HPG2	HPG1	HPG0
COMMAND40 (Character size control)	1	1	0	0	0	0	0	0	0	0	0	0	SZV1	SZV0	SZH1	SZH0
COMMAND41 (Character size control: line setting U)	1	1	0	0	0	1	0	0	LSZ7	LSZ6	LSZ5	LSZ4	LSZ3	LSZ2	LSZ1	LSZ0
COMMAND42 (Character size control: line setting D)	1	1	0	0	1	0	0	0	LSZ15	LSZ14	LSZ13	LSZ12	LSZ11	LSZ10	LSZ9	LSZ8
COMMAND50 (Box control U)	1	1	0	1	0	0	0	0	BXUW	BXLW	0	BXUCT0	BXUC3	BXUC2	BXUC1	BXUC0
COMMAND51 (Box control D)	1	1	0	1	0	1	0	0	BXDW	BXRW	0	BXDCT0	BXDC3	BXDC2	BXDC1	BXDC0
COMMAND52 (Box control: line setting U)	1	1	0	1	1	0	0	0	LBX7	LBX6	LBX5	LBX4	LBX3	LBX2	LBX1	LBX0
COMMAND53 (Box control: line setting D)	1	1	0	1	1	1	0	0	LBX15	LBX14	LBX13	LBX12	LBX11	LBX10	LBX9	LBX8
COMMAND60 (Border control)	1	1	1	0	0	0	BLK1	BLK0	0	0	0	EGCT0	EGC3	EGC2	EGC1	EGC0
COMMAND61 (Border control: line setting U)	1	1	1	0	0	1	0	0	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
COMMAND62 (Border control: line setting D)	1	1	1	0	1	0	0	0	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
COMMAND70 (Write address) Color Table	1	1	1	1	0	0	0	0	0	0	0	CIN1	CTA3	CTA2	CTA1	CTA0
COMMAND71 (Data write) Color Table	1	1	1	1	0	1	0	RM3(1)	0	0	0 TG2	0 TG1	TCK TG0	TB2 TR2	TB1 TR1	TB0 TR0

Command 00 (Main screen write address set command)

• First byte

DA0 to 7	Pogistor		Content	Notes		
DAU IU 7	to 7 Register State		Function	Notes		
7	_	1				
6	_	0	Command 0 identification code			
5	_	0	Main screen write address setting			
4	_	0				
3	_	0	Sub-identification code: 0			
2	_	0	Sub-identification code. 0			
1	V3	0				
'	<msb></msb>	1				
0	V2	0				
U	٧Z	1				

DA040.7	Domintor		Content	Notes
DA0 to 7	Register	State	Function	Notes
7	V1	0	Main screen memory line address	
	VI	1	(0 to E, hexadecimal)	
6	V0	0	QVGA mode: 13 lines	
0	<lsb></lsb>	1	WVGA mode: 15 lines	
5	H5	0		
5	<msb></msb>	1		
4	H4	0		
4	П4	1		
3	H3	0	Main screen memory character position address	
3	пэ	1	(00 to 27, hexadecimal)	
2	H2	0	QVGA mode: 40 characters	
	П2	1	WVGA mode: 33 characters	
1	H1	0		
	пІ	1		
0	H0	0		
	<lsb></lsb>	1		

Command 01 (Subscreen write address set command)

• First byte

DA0 to 7	Pogistor		Content	Notes
DAU IU 7	0 to 7 Register S		Function	Notes
7	_	1		
6	_	0	Command 0 identification code	
5	_	0	Subscreen memory write address setting	
4	_	0		
3	_	0	Sub-identification code: 1	
2	_	1	Sub-lideritification code. 1	
1	_	0		
0	_	0		

DAO to 7	DA0 to 7 Register		Content	Notes
DAU 10 7			Function	Notes
7	_	0		
6	V0	0	Subscreen memory line address	
6	٧٥	1	(0 to 1, hexadecimal) 2 lines	
5	_	0		
4	_	0		
3	_	0		
2	_	0		
1	_	0		
0	HO	0	Subscreen memory character address	
	<lsb></lsb>	1	(0 to 1, hexadecimal) 2 characters	

Command 10 (Main screen display character data write setting command)

• First byte

DA0 to 7	Pogistor		Content	Notes			
DAU to 7	Register	State	Function	Notes			
7	_	1					
6	_	0	Command 1 identification code	When this command has been issued, the IC remains in display character data write mode until the CS pin is set high.			
5	_	0	Display character data write setting				
4	_	1					
3	_	0	Sub-identification code 0				
2	_	0	Sub-identification code o				
1	RM2	0	RM2 RM1 Mode				
'	KIVIZ	1	0 0 (1)(2)(3)(4) End 0 1 (1)(2)(3)(4) Continuous	Continuous write mode selection			
0	RM1	0	1 0 (3)(4) Continuous	Commission with most school of			
0	KIVI I	1	1 1 (2)(3)(4 Continuous				

• Second byte (1)

DA040.7	Dogiotor		Content	Notes	
DA0 to 7	7 Register	/ Register	State	Function	Notes
7	_	0			
6	_	0			
5	at	0	Blinking off	Plinking appoification	
5	aı	1	Blinking on	Blinking specification	
4	BXS	0	Protruding	Pay apacification: raised/rassand	
4	BAS	1	Recessed	Box specification: raised/recessed	
3	BXL	0	None	Box specification: left side	
3	BAL	1	Box displayed	Box specification: left side	
2	BXR	0	None	Box specification: right side	
	DAK	1	Box displayed	Box specification. fight side	
1	BXU	0	None	Day an addication, tan	
'	BAU	1	Box displayed	Box specification: top	
0	BXD	0 None	None	D " " D "	
	DVD	1	Box displayed	Box specification: Bottom	

• Second byte (2)

DA0 to 7	Dogistor		Content	Notes
DAU 10 7	DA0 to 7 Register	State	Function	Notes
7	CB3	0		
,	[MSB]	1		
6	CB2	0		
6	CBZ	1	Character background color specification	Character background color specification When a character glyph is specified, 1 of 16 colors
5	CB1	0	0000 to 1111, or 0 to F (hexadecimal)	may be selected.
5	СВТ	1		
4	CB0	0		
4	[LSB]	1		
3	CC3	0		
3	[MSB]	1		
2	CC2	0		Character color specification When a character glyph is specified, 1 of 16 colors
	002	1	Character color specification	
1	CC1	0	0000 to 1111, or 0 to F (hexadecimal)	may be selected.
	001	1		
0	CC0	0		
	<lsb></lsb>	1		

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

• Second byte (3)

DA0 to 7	Dogistor		Content	Notes
DAU to 7	Register	State	Function	Notes
7	_	0		
6	_	0		
5	CT0	0	Color table number 1	Color table selection
5	CIO	1	Color table number 2	Color table selection
4	I/E	0	Internal ROM	ROM selection
4	1/ 🗀	1	External ROM	ROW Selection
3	M/G	0	Character	Character/graphic specification
3	IVI/G	1	Graphic	Character/graphic specification
2	C10	0		
	[MSB]	1		
1	C9	0		Character code specification
'	1 69	1		Character code specification
0	C8	0		
		1		

• Second byte (4)

DA04- 7	Desistes	Content		Neter	
DA0 to 7 Register	State	Function	Notes		
7	C7	0			
'	C/	1			
6	C6	0			
6	Co	1	Character code		
5	CF	C5	0	Internal ROM: 512 characters 000 to 1FF (hexadecimal)	
5	Co	1	0 to 511		
4	C4	0			
4	C4	1	External ROM: 2048 characters 000 to 7FF (hexadecimal)		
3	C3	0	0 to 2047	Character code specification	
3	Co	1			
2	C2	0	* Transparent character specification I/E = 0 (Internal ROM)		
	2 02	1	M/G = 0 (Character)		
1	C1	0	Code = 1FF (hexadecimal)		
'	OI	1			
0	C0	0			
U	[LSB]	1			

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 11 (Subscreen display character data write setting command)

• First byte

DA0 to 7	to 7 Degister		Content	Notes	
DAU 10 7	Register	State	Function	Notes	
7	_	1			
6	_	0	Command 1 identification code	When this command has been issued, the IC remains in display character data write mode until	
5	_	0	Display character data write setting	the CS pin is set high.	
4	_	1			
3	_	0	Sub-identification code 1		
2	_	0	Sub-identification code 1		
1	RM2	0	RM2 RM1 Mode		
'	KIVIZ	1	0 0 [1][2][3][4] End 0 1 [1][2][3][4] Continuous	Continuous write mode selection	
0	RM1	0	1 0 [3][4] Continuous	Continuous with mode selection	
	IXIVII	1	1 1 [2][3][4] Continuous		

• Second byte (1)

DAO to 7	DA0 to 7 Register		Content	Notes
DAU to 7	Register	State	Function	Notes
7	_	0		
6	_	0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

• Second byte (2)

DA0 to 7	Degister		Content	Notes
DAU 10 7	Register	State	Function	Notes
7		0		
6		0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

• Second byte (3)

DA0 to 7	Dogiotor		Content	Notes	
DAU IO 1	7 Register	State	Function	Notes	
7	_	0			
6	_	0			
5	СТО	0	Color table number 1	Color table selection	
5	CIO	1	Color table number 2	Color table selection	
4	l/E -	1/5	0	0 Internal ROM	ROM selection
4		1	External ROM	ROW SELECTION	
3	M/G	0	Only when transparent is selected	Craphia only	
3	IVI/G	1	Graphic only	Graphic only	
2	C10	0			
	[MSB]	1			
1	C9	0		Character and appointment	
'	1 69	1		Character code specification	
0	C8	0			
	C0	1			

• Second byte (4)

DA04- 7	Danistan		Content	Nata
DA0 to 7	DA0 to 7 Register	State	Function	Notes
7	C7	0		
_ ′	C7	1		
6	C6	0		
0	Co	1	Character code	
5	C5	0	Internal ROM: 512 characters 000 to 1FF (hexadecimal)	
5	C5	1	0 to 511	
4	C4	0		
4	04	1	External ROM: 2048 characters 000 to 7FF (hexadecimal)	Character code specification
3	C3	0	0 to 2047	Character code specification
3	CS	1		
2	C2	0	* Transparent character specification I/E = 0 (Internal ROM)	
	2 02	1	M/G = 0 (Character)	
1	1 C1	0	Code = 1FF (hexadecimal)	
_ '	CI	1		
0	C0	0		
	[LSB]	1		

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 20 (System control settings command)

• First byte

DA0 to 7	Pogistor		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5		1	System control settings	
4		0		
3		0		
2		0	Sub-identification code 0	
1		0	Sub-identification code 0	
0		0		

DA0 to 7	Dogiotor		Content	Notes	
DAU 10 7		State	Function	Notes	
7	TSTMD2	0	Normal operation	Do not use test mode. This bit must be set to 0.	
	1311/102	1	Test mode 2	Do not use test mode. This bit must be set to 0.	
6	TSTMD1	0	Normal operation	Do not use test mode. This bit must be set to 0.	
0	TSTIVIDT	1	Test mode 1	Do not use test mode. This bit must be set to 0.	
5	Q/W2	0	Normal mode	Normal / Independent	
5	Q/VVZ	1	Independent mode	Normal / Independent	
4	Q/W1	0	QVGA mode	OVGA / WVGA	
4	Q/VV I	1	WVGA mode	QVGA/ WVGA	
3	CVCDCT	SYSRST	0		The registers are reset when the CSB pin is low.
3	313831	1	Reset all registers (All bits set to 0.)	The reset state is cleared when the CSB pin goes high.	
2	CTERS	0		Applications must provide a wait time of about 1ms.	
	CILKS	1	Erase the color table. (Sets all values to 00.)	Use DSPOFF to execute this operation.	
		0		A - li-stir-s	
1	SRMERS	1	Erase main RAM. (Sets all values to 00.) Wallpaper	Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.	
		0		A1:4:	
0	MRMERS	1	Erase sub-RAM. (Sets all values to 00.) Main screen	Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.	

Command 21 (Display control settings command)

• First byte

DAO to 7	DA0 to 7 Register		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5	_	1	Display control	
4	_	0		
3	_	0		
2	_	0	Sub-identification code 1	
1		0	Sub-identification code i	
0		1		

DA0 to 7	Register		Content	Notes	
DAU IO /	A0 to 7 Register	State	Function	Notes	
7	100055	0	Enables stopping the LC oscillator	LOilleten stemstem	
'	LCSOFF	1	Disables stopping the LC oscillator	LC oscillator stop control	
	DICA	0	BK1 BK0		
6	BK1	1	0 0 1/16	Blinking period	
_	DICO	0	0 1 1/32 1 0 1/64	Specified for screen units.	
5	BK0	1	1 0 1/04		
4	SBG1	0	Display before the main screen	Subscroon display specification	
4	SBGT	1	Display after the main screen	Subscreen display specification	
3	SBG0	0	Iterated display (wallpaper)	Subserses display apositionties	
3	SBGU	1	Horizontal 2-character x vertical 2-character display (sprite)	Subscreen display specification	
2	DSPBG	0	Display off	Screen background color	
	DSFBG	1	Display on	Screen background color	
1	DSPGS	0	Display off	Subserses (wellpener)	
	DSPGS	1	Display on	Subscreen (wallpaper)	
0	DSDCM	0	Display off	- Main screen	
U	DSPGM	1	Display on	Walli Screen	

 $[\]ast :$ This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}\,\text{pin}.$

Command 22 (I/O polarity control settings command)

• First byte

DAO to 7	DA0 to 7 Register		Content	Notes
DAU to 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5	_	1	Display character data write settings	
4	_	0		
3	_	0		
2	_	0	Extended command identification code 2	
1		1	Exterided command identification code 2	
0		0		

DA0 to 7	Degister		Content	Notes
DAU 10 7	to 7 Register		Function	Notes
7	BLD1	0	BLD1 BLD0	
'	BLUI	1	0 0 ±0 0 1 +1	BLK output delay setting
6	DI DO	0	1 0 +2	In dot clock units
0	BLD0	1	1 1 +3	
-	DI OD	0	BLK output: positive polarity	DI K autaut adarity adartica
5	5 BLOP	1	BLK output: negative polarity	BLK output polarity selection
4	BLO1	0	BLO1 BLO0	
4	BLOT	1	0 0 Text + character background + wallpaper + screen background 0 1 Text + character background + wallpaper	BLK output control
3	BLO0	0	1 0 Text + character background	BEN output control
3	BLOU	1	1 1 Text	
2	CKP	0	Clock input: positive polarity	Clear input palarity adjection
2	CKP	1	Clock input: negative polarity	Clock input polarity selection
4	VIP	0	VSYNC input: negative polarity	VSVNC input palarity adjection
	VIP	1	VSYNC input: positive polarity	VSYNC input polarity selection
	HIP	0	HSYNC input: negative polarity	LICYNIC input polarity polarity
0		1	HSYNC input: positive polarity	HSYNC input polarity selection

 $[\]ast :$ This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 23 (Screen background color settings command)

• First byte

DA0 to 7	Dogistor	Content		Notes
DAU IO 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5	_	1	Display character data write settings	
4	_	0		
3	1	0		
2		0	Extended command identification code 3	
1		1	Exterided command identification code 3	
0		1		

DA0 to 7	Dogistor		Content	Notes
DA0 to 7	Register	State	Function	Notes
7	_	0		
6	1	0		
5	BGCT1	0	T1 T0	
3	ВОСТТ	1	0 0 Color table No. 2	Screen background color
4	BGCT0	0	0 1 Invalid setting 1 X Color table No. 1	Color table setting
4	BGC10	1	1 X Gold table (10. 1	
3	BGC3	0		
3	ВОСЗ	1		
2	BGC2	0		
	BGC2	1	Screen background color 0000 to 1111	Screen background color
1	BGC1	0	0 to F (hexadecimal)	Selects 1 of 16 values.
	ВОСТ	1		
0	BGC0	0		
	DGC0	1		

 $[\]ast :$ This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}\,\text{pin}.$

Command 24 (I/O polarity control settings command)

• First byte

DA0 to 7	Pogistor	Content		Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5	_	1	Display character data write settings	
4	_	0		
3	_	0		
2	_	1	Extended command identification code 4	
1		0	Extended command identification code 4	
0		0		

DAO to 7	Degister		Content	Notes
DA0 to 7	Register	State	Function	Notes
7	DSPMD1	0	MD1 MD0	Main screen display area selection
	DSFINIDT	1	0 0 40 characters × 13 lines	Clock output polarity selection
6	DSPMD0	0	0 1 33 characters × 15 lines 1 0 40 characters × 16 lines	Only valid in independent mode. COM20 to COM2
6	DSFINIDO	1	1 0 40 Glaracters × 10 lines	COM20 to COM2
5	D/ASEL	0	On	D/A converter used/unused selection
5	DIASEL	1	Off	Only valid in independent mode. COM20 to COM2
4	VBLKON	0	Disabled	VBLK input selection
4	VBLKON	1	Enabled	VBLK Input selection
3	HBLKON	0	Disabled	HPLK input coloction
3	HBLKON	1	Enabled	HBLK input selection
2	СКОР	0	Clock output positive polarity	Clock output polarity selection
	CKOP	1	Clock output negative polarity	Clock output polarity selection
4	4 1/00	0	VBLK input negative polarity	VPLK input polarity solection
	VBP	1	VBLK input positive polarity	VBLK input polarity selection
0	LIDD	0	HBLK input negative polarity	UPLK input polarity colorion
U	HBP	1	HBLK input positive polarity	HBLK input polarity selection

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

Command 25 (Output control 3 settings command)

• First byte

DAO to 7	DA0 to 7 Register		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6		0	Command 2 identification code	
5	_	1	Display character data write settings	
4	_	0		
3		0		
2		1	Extended command identification code 5	
1		0	Extended command identification code 5	
0		1		

• Second byte

DA0 to 7	Dogiotor		C	Content	Notes
DAU IU 7	Register	State		Function	Notes
7	_	0			
6	_	0			
5	_	0			
4	OTMDa	0			
4	OTMD2	1	OTMD2 OTMD1 OT	•	
3	OTMD1	0	0 0	0 Normal 1 RGB No. 1	A0:17 output selection
3	OTIVIDT	1	0 1	0 RGB No. 2	7.6.17 Galpat Goldston
2	OTMD0	0	0 1	1 High-impedance state	
2	OTMDO	1			
1	QRM1	0	QRM1 QRM0	ROM selection	
'	QKIVII	1	0 0	ROM1	POM collection when character output is appointed
		0	0 1	ROM2	ROM selection when character output is specified in QVGA mode
0	QRM0	1	1 0 1	ROM3 ROM4	

^{*:} This register is set to the all bits zero state when the IC is reset by the RST pin.

• When RGB No. 1 or RGB No. 2 is selected:

The A17:9 output is set to the

RDB2 to BD0 three-value output. (Supported by connecting external resistors.)

* It will not be possible to use external ROM in this case. (Only internal ROM can be used.)

No. 1: RGB = 000 = Black only. Here the output will go to the high-impedance state giving the middle level due to the external resistor. For areas other than the display area, the output will be at the low level.

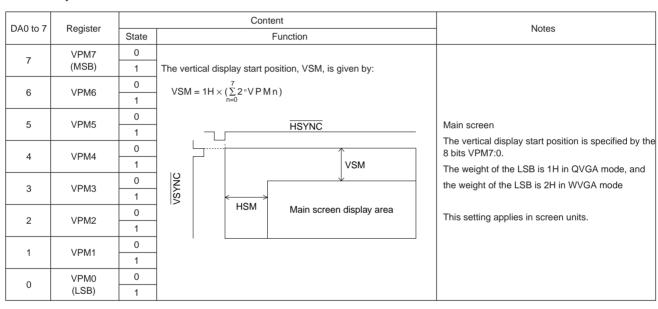
No. 2: When any individual color is zero, the output will go to the high-impedance state giving the middle level due to the external resistor.

For areas other than the display area, the output will be at the low level.

Command 30 (Main screen: vertical display start position setting command)

• First byte

DAO to 7	DA0 to 7 Register		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 3 identification code	
5	_	1	Main screen: vertical display start position setting	
4	_	1		
3	_	0		
2		0	Extended command identification code 0	
1	_	0	Extended command identification code o	
0	_	0		



Command 31 (Main screen: horizontal display start position setting command)

• First byte

DA0 to 7	Dogiotor	Content		Notes
DAU to 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 3 identification code	
5	_	1	Main screen: horizontal display start position setting	
4	_	0		
3	_	0		
2	_	0	Extended command identification code 1	
1	_	1		
0	HPM8	0		
	(MSB)	1		

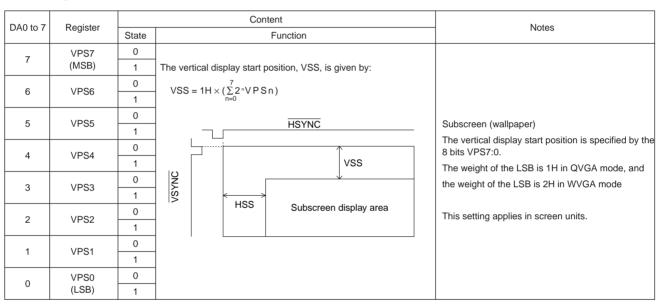
DA0 to 7	Register		Content	Notes
DAU to 7	Register	State	Function	Notes
7	HPM7	0		
·		1		
6	HPM6	0	The horizontal display start position, HSM, is given by:	
	111 1010	1	8 8 8 8	
5	HPM5	0	$HSM = 1Tc \times (\sum_{n=0}^{\infty} 2^{n} H P M n) + \alpha$	Main screen
		1	α = 57 Tc	The horizontal display start position is specified by
4	HPM4	0	To The insulation to the control of	the 9 bits HPM8:0.
		1	Tc: The input clock frequency in operating mode.	The weight of the LSB is 1TC in QVGA mode, and
3	HPM3	0		the weight of the LSB is 2TC in WVGA mode
		1		
2	HPM2	0	Setting disable range	This setting applies in screen units.
_		1	QVGA: 00 to 0F HEX	
1	HPM1	0	WVGA: 00 to 07 HEX	
_ '	1411	1		
0	HPM0	0		
	(LSB)	1		

^{* :} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

Command 32 (Subscreen: vertical display start position setting command)

• First byte

DA0 to 7	0A0 to 7 Register		Content	Notes
DAU IU 7	Register	State Function		Notes
7	_	1		
6		0	Command 3 identification code	
5		1	Subscreen: vertical display start position setting	
4		1		
3		0		
2		1	Extended command identification code 2	
1		0		
0		0		



Command 33 (Subscreen: horizontal display start position setting command)

• First byte

DAO to 7	DA0 to 7 Register		Content	Notes
DAU IO 7			Function	Notes
7	_	1		
6	_	0	Command 3 identification code	
5	_	1	Subscreen: horizontal display start position setting	
4	_	0		
3	_	0		
2	_	1	Extended command identification code 3	
1		1		
0	HPS8	0		
	(MSB)	1		

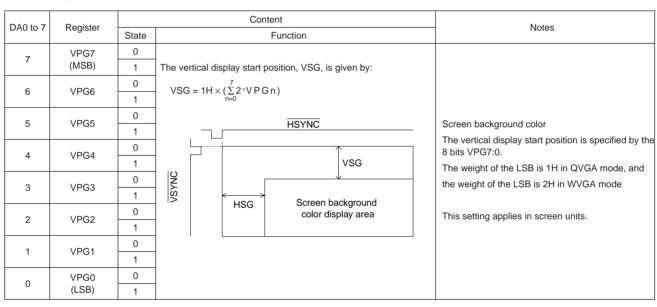
DA0 to 7	Register		Content	Notes
DAU to 7	Register	State	Function	Notes
7	HPS7	0		
,	111 01	1		
6	HPS6	0	The horizontal display start position, HSS, is given by:	
	111 00	1	8 (FO-LIDO)	
5	HPS5	0	HSS = $1\text{Tc} \times (\sum_{n=0}^{\infty} 2^n \text{HPS} n) + \alpha$ $\alpha = 14 \text{ Tc}$	Subscreen (wallpaper)
4	HPS4	0	Tc: The input clock frequency in operating mode.	The horizontal display start position is specified by the 9 bits HPS8:0.
		1	To the input disentinoquency in operating measur	The weight of the LSB is 1TC in QVGA mode, and
3	HPS3	0		the weight of the LSB is 2TC in WVGA mode
		0		
2	HPS2	1	Setting disable range	This setting applies in screen units.
1	HPS1	0	QVGA: 00 to 2F HEX	
·		1	WVGA: 00 to 17 HEX	
0	HPS0	0		
	(LSB)	1		

^{* :} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

Command 34 (Screen background color: vertical display start position setting command)

• First byte

DA0 to 7	Register	Pogiator		Content	Notes
DAU to 7	Register	State	Function	Notes	
7	_	1			
6	_	0	Command 3 identification code		
5	_	1	Screen background color: vertical display start position setting		
4	_	1			
3	_	1			
2	_	0	Extended command identification code 4		
1	_	0			
0	_	0			



Command 35 (Screen background color: horizontal display start position setting command)

• First byte

DAO to 7	Pogistor		Content	Notes
DAU to 7	DA0 to 7 Register		Function	Notes
7	_	1		
6	_	0	Command 3 identification code	
5	_	1	Screen background color: horizontal display start position setting	
4	_	1		
3	_	1		
2	_	0	Extended command identification code 5	
1		1		
0	HPS8	0		
	(MSB)	1		

DA0 to 7	Dogistor		Content	Notes
DA0 to 7	A0 to 7 Register		Function	Notes
7	HPG7	0		
_ ′	пРСТ	1		
6	HPG6	0	The horizontal display start position, HSG, is given by:	
6	HPG6	1	8	
5	HPG5	0	$HSG = 1Tc \times (\sum_{n=0}^{\infty} 2^{n} H P G n)$	
3	HFG5	1	Tc: The input clock frequency in operating mode.	Screen background color
4	HPG4	0		The horizontal display start position is specified by
4	HFG4	1		the 9 bits HPG8:0.
3	LIDCa	0		The weight of the LSB is 1TC in QVGA mode, and
3	HPG3	1		the weight of the LSB is 2TC in WVGA mode
2	LIDOS	0		This setting applies in screen units.
2	HPG2	1		
1	LIDC4	0		
	HPG1	1		
0	HPG0	0		
	(LSB)	1		

^{* :} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

Command 40 (Character size control setting command)

• First byte

DA0 to 7	A0 to 7 Register		Content	Notes
DAU IO 7	Register	State	Function	Notes
7	_	1		
6	_	1	Command 4 identification code	
5	_	0	Display character data write settings	
4	_	0		
3	_	0	Extended command identification code 0	
2	_	0	Exterided Command Identification code o	
1		0		
0		0		

DA0 to 7	Dogiotor	Content		Notes		
DAU 10 7	DA0 to 7 Register	State			Function	Notes
7	_	0				
6	_	0				
5	_	0				
4	_	0				
3	SZV1	0	SZV1	SZV0	Character size	
3	32 V I	1	0	0	1×	Specifies the character size in the vertical direction.
		0	0	1	2×	This setting applies in line units.
2	SZV0	1	1 1	0 1	3× 4×	
4	SZH1	0	SZH1	SZH0	Character size	
'	52H1	1	0	0	1×	Specifies the character size in the horizontal
0	SZH0	0	0 1 1		2× 3× 4×	direction. This setting applies in line units.

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\mbox{RST}}$ pin.

Command 41 (Character size line U control setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	1	Command 4 identification code	
5	_	0	Character size line U control	
4	_	0		
3	_	0	Extended command identification code 1	
2	_	1	Extended command identification code 1	
1	_	0		
0	_	0		

DA040.7	Dogiotor		Content	Notes
DA0 to 7	7 Register Sta		Function	Notes
7	LSZ7	0	Do not set for line 8.	
'	L521	1	Set for line 8.	
6	LSZ6	0	Do not set for line 7.	
0	L526	1	Set for line 7.	
5	LSZ5	0	Do not set for line 6.	
5	L5Z5	1	Set for line 6.	
4	LSZ4 0	0	Do not set for line 5.	
4		1	Set for line 5.	Character size line setting control
3	LSZ3	0	Do not set for line 4.	Upper lines
3	LSZS	1	Set for line 4.	
2	LSZ2	0	Do not set for line 3.	
2	LSZZ	1	Set for line 3.	
1	LSZ1	0	Do not set for line 2.	
'	LSZT	1	Set for line 2.	
0	LSZ0	0	Do not set for line 1.	
	L320	1	Set for line 1.	

Command 42 (Character size line D control setting command)

• First byte

DA0 to 7	DAO to 7 Register		Content	Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	1	Command 4 identification code	
5	_	0	Character size line D control	
4	_	0		
3	_	1	Extended command identification code 2	
2	_	0	Extended Command Identification Code 2	
1	_	0		
0	_	0		

DA0 to 7	Dogiotor		Content	Notes		
DA0 to 7	Register State		Function	Notes		
7	1.0745	0	Do not set for line 16.			
'	LSZ15	1	Set for line 16.			
6	LSZ14	0	Do not set for line 15.			
0	L5Z14	1	Set for line 15.			
5	LSZ13	0	Do not set for line 14.			
5	L5Z13	1	Set for line 14.			
4	LSZ12 0 1	1 9712	1 9712	0	Do not set for line 13.	
4		1	Set for line 13.	Character size line setting control		
3	LSZ11	0	Do not set for line 12.	Lower lines		
3	LSZTT	1	Set for line 12.			
2	LSZ10	0	Do not set for line 11.			
	L3Z10	1	Set for line 11.			
1	LSZ9	0	Do not set for line 10.			
_ '	L329	1	Set for line 10.			
0	LSZ8	0	Do not set for line 9.			
	L020	1	Set for line 9.			

Command 50 (Box control: U setting command)

• First byte

DA0 to 7	Register	Content		Notes
DAU IU 7		State	Function	Notes
7	_	1		
6	_	1	Command 5 identification code	
5	_	0	Display character data write settings	
4	_	1		
3	_	0	Extended command identification code 0	
2	_	0	Extended command identification code o	
1	_	0		
0	_	0		

DAO to 7	DA0 to 7 Register		Content	Notes
DAU IU 7		State	Function	Notes
7	BXUW	0	Box display: upper side is 1 dot.	Box display: upper side
'	BAUW	1	Box display: upper side is 2 dot.	Dot width. This setting applies in line units.
6	BXLW	0	Box display: left side is 1 dot.	Box display: left side
0	BALVV	1	Box display: left side is 2 dot.	Dot width. This setting applies in line units.
5	_	0		
4	BXUCT0	0		Box display: upper side Color table specification
-		1	Color table No. 2	This setting applies in line units.
3	BXUC3	0		
3	BAUCS	1		
2	BXUC2	0		
	BAUCZ	1	Box display: upper side color specification 0000 to 1111	Box display: upper side Color specification
1	BXUC1	0	0 to F (hexadecimal)	This setting applies in line units.
!	BAUCT	1		
0	BYLICO	BXUC0 0 1		
	DAGGO			

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 51 (Box control: D setting command)

• First byte

DA0 to 7	Register	Content		Notes
DAU IU 7		State	Function	Notes
7	_	1		
6	_	1	Command 5 identification code	
5	_	0	Display character data write settings	
4	_	1		
3	_	0	Extended command identification code 1	
2	_	1	Extended command identification code 1	
1	_	0		
0	_	0		

DA0 to 7	Pogiator		Content	- Notes
DAU IO 7	Register	State	Function	
7	BXDW	0	Box display: lower side is 1 dot.	Box display: lower side
1	BYDW	1	Box display: lower side is 2 dot.	Dot width. This setting applies in line units.
6	BXRW	0	Box display: right side is 1 dot.	Box display: right side
0	DARW	1	Box display: right side is 2 dot.	Dot width. This setting applies in line units.
5	_	0		
4	BXDCT0	0	Color table No. 1	Box display: lower side Color table specification
7		1	Color table No. 2	This setting applies in line units.
3	BXDC3	0		
3	BADC3	1		
2	BXDC2	0		
2	BADGZ	1	Box display: lower side color specification 0000 to 1111	Box display: lower side Color specification
1	BXDC1	0	0 to F (hexadecimal)	This setting applies in line units.
1	BADCI	1	` '	
0	BXDC0	0		
U		1		

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 52 (Box control: U line setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU IU 7		State	Function	Notes
7	_	1		
6	_	1	Command 5 identification code	
5	_	0	Character size: line U control	
4	_	1		
3	_	1	Extended command identification code 2	
2	_	0	Extended command identification code 2	
1	_	0		
0	_	0		

DA04-7	Daviston		Content	Notes	
DA0 to 7	A0 to 7 Register	State	Function	Notes	
7	LBX7	0	Do not set for line 8.		
'	LDA/	1	Set for line 8.		
6	LBX6	0	Do not set for line 7.		
6	LD/0	1	Set for line 7.		
5	LDVE	F LDVF	0	Do not set for line 6.	
5	LBX5	1	Set for line 6.		
4	LBX4	0	Do not set for line 5.		
4		1	Set for line 5.	Box control line setting control	
3	LBX3	0	Do not set for line 4.	Upper lines	
3	LDV3	1	Set for line 4.		
2	2 LBX2	0	Do not set for line 3.		
	LDAZ	1	Set for line 3.		
1	LBX1	0	Do not set for line 2.		
'	LDAI	1	Set for line 2.		
0	LBX0	0	Do not set for line 1.		
U	LBX0	1	Set for line 1.		

Command 53 (Character size: Line D control setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU IU 7		State	Function	Notes
7	_	1		
6	_	1	Command 5 identification code	
5	_	0	Character size line D control	
4	_	1		
3	_	1	Extended command identification code 3	
2	_	1	Extended command identification code 3	
1	_	0		
0	_	0		

DA040.7	Dogiotor		Content	Notes	
DA0 to 7	Register	State	Function	Notes	
7	LDV45	0	Do not set for line 16.		
'	LBX15	1	Set for line 16.		
6	LBX14	0	Do not set for line 15.		
0	LBA14	1	Set for line 15.		
5	1.57/40	L DV40	0	Do not set for line 14.	
5	LBX13	1	Set for line 14.		
4	LBX12	0	Do not set for line 13.		
4		1	Set for line 13.	Box control line setting control	
3	LBX11	0	Do not set for line 12.	Lower lines	
3	LBATT	1	Set for line 12.		
2	LBX10	0	Do not set for line 11.		
	LDAIU	1	Set for line 11.		
1	LBX9	0	Do not set for line 10.		
	LDVA	1	Set for line 10.		
0	LBX8	0	Do not set for line 9.		
	LDAO	1	Set for line 9.		

Command 60 (Border control settings command)

• First byte

DA0 to 7	Register		Content	- Notes
DAU to 7		State	Function	
7	_	1		
6	_	1	Command 6 identification code	
5	_	1	Display character data write settings	
4	_	0		
3	_	0	Extended command identification code 0	
2	_	0	Extended command identification code o	
1	BLK1	0	BLK1 BLK0	
'	BLKT	1	0 0 Normal display 0 1 Border	Border mode specification
0	BLK0	0	1 0 Shadow 1 (lower side)	This setting applies in line units.
	BLKU	1	1 1 Shadow 2 (lower and right sides)	

DA0 to 7	Pogistor		Content	Notes
DA0 to 7	Register	State	Function	
7	_	0		
6	_	0		
5	_	0		
4	EGCT0	0	Color table No. 1	Border display Color table specification
4	EGC10	1	Color table No. 2	This setting applies in line units.
3	EGC3	0		
3	LGC3	1		
2	EGC2	0		
	EGC2	1	Border display: color specification 0000 to 1111	Border display color specification
1	EGC1		0 to F (hexadecimal)	This setting applies in line units.
'	EGCT	1	` '	
0	FCC0	EGC0 0 1		
	EGC0			

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

Command 61 (Border control U line settings command)

• First byte

DA0 to 7	Pogistor	Content		Notes
DAU IU 7	Register	State	Function	Notes
7	_	1		
6	_	1	Command 6 identification code	
5	_	1	Character size: line U control	
4	_	0		
3	_	0	Extended command identification code 1	
2	_	1	Extended command identification code i	
1	_	0		
0	_	0		

• Second byte

DA0 to 7	Dogiotor		Content	Notes	
DA0 to 7	7 to 7 Register	NO to 7 Register	State	Function	Notes
7	LFC7	0	Do not set for line 8.		
'	LFC/	1	Set for line 8.		
6	LFC6	0	Do not set for line 7.		
0	LFC6	1	Set for line 7.		
5	LFC5	0	Do not set for line 6.		
5	LFC5	1	Set for line 6.		
4	LFC4	0	Do not set for line 5.		
4	LFC4	1	Set for line 5.	Border control line settings control	
3	LFC3	0	Do not set for line 4.	Upper lines	
3	LFC3	1	Set for line 4.		
2	LFC2	0	Do not set for line 3.		
	LFC2	1	Set for line 3.		
1	LFC1	0	Do not set for line 2.		
'	LFC1	1	Set for line 2.		
0	LECO	0	Do not set for line 1.		
	D LFC0	1	Set for line 1.		

Command 62 (Border control D line settings command)

• First byte

DA0 to 7	Register		Content	Notes
DAU to 7		State	Function	Notes
7	_	1		
6	_	1	Command 6 identification code	
5	_	1	Character size: line D control	
4	_	0		
3	_	1	Extended command identification code 2	
2	_	0	Extended command identification code 2	
1	_	0		
0	_	0		

• Second byte

DA0 to 7	Pogistor		Content	Notes
DAU IO 7	Register	State	Function	Notes
7		0	Do not set for line 16.	
/	LFC15	1	Set for line 16.	
6	LFC14	0	Do not set for line 15.	
0	LFC14	1	Set for line 15.	
5	LFC13	0	Do not set for line 14.	
5	LFC13	1	Set for line 14.	
4	LFC12	0	Do not set for line 13.	
4	LFC12	1	Set for line 13.	Border control line settings control
3	LFC11	0 Do not set for line 12.	Lower lines	
3	LFCTT	1	Set for line 12.	
2	LFC10	0	Do not set for line 11.	
2	LFC10	1	Set for line 11.	
1	LFC9 —	0	Do not set for line 10.	
'		1	Set for line 10.	
0	LFC8	0	Do not set for line 9.	
U	LI 00	1	Set for line 9.	

Command 70 (Color table write address setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU IU 7		State	Function	Notes
7	_	1		
6	_	1	Command 7 identification code	
5	_	1	Color table write address setting	
4	_	1		
3	_	0	Sub-identifier code 0	
2	_	0	Sub-identifier code o	
1	_	0		
0	_	0		

• Second byte

DA0 to 7	Register	Content		Notes
DA0 to 7		State	Function	Notes
7	_			
6	_			
5	_			
4	CTN1	0	Color table No. 1 selected	Color table selection
4	CINI	1	Color table No. 2 selected	No. 1 or No. 2
3	CTA3	0		Addresses of the color tables
3	<msb></msb>	1		
2	CTA2	0		
	CTAZ	1	Color table address 0 to 15	
1	CTA1	0	0 to F (hexadecimal) 16 values	
		1		
0	CTA0	0		
	<lsb></lsb>	1		

Command 71 (Color table data write setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU to 7		State	Function	Notes
7	_	1		
6	_	1	Command 7 identification code	When this command has been issued, the IC remains in display character data write mode until
5	_	1	Display character data write setting	the CS pin is set high.
4	_	1		
3	_	0	Sub-identifier code 1	
2	_	1	Sub-identifier code i	
1	_	0		
0	RM3	0	RM3 Mode 0 [1][2] End	Continuous write mode selection
	1400	1	1 [1][2] Continuous	33

• Second byte (1)

DA0 to 7	Register	Content		Notes
DAU 10 7		State	Function	Notes
7	_	0		
6	_	0		
5	_	0		
4	_	0		
3	ТОК	0	Color	
3		1	Transparent (BLK output: low)	
2	TB2	0		
	I DZ	1	Color table	
1	TB1	0	B output	Color table setting B
'	101	1	000 to 111	
0	TPO	0	0 to 7 (hexadecimal)	
	TB0	1		

• Second byte (2)

DA0 to 7	Pogiator	Content		Neter
DA0 to 7	Register	State	Function	Notes
7	_	0		
6	_	0		
5	TG2	0		
5	162	1	Color table	
4	TG1	0	G output	Color table setting G
4	IGI	1	000 to 111	Color table setting G
3	TCO	0	0 to 7 (hexadecimal)	
3	TG0	1		
2	TR2	0		
2	IR2	1	Color table	Color table setting R
1	TD4	0 R output		
	TR1	1	000 to 111	
0	TDO	0 to 7 (hexadecimal)		
0	TR0	1		

^{*:} This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

When transparent is selected, the BLK output is set to the low level. (Transparent state)

The RGB outputs are values from the color table.

The transparent specification is best for color table 1, address 0000.

Since the data is set to all zeros by a RAM clear operation,

The RGB output will be 000 (black) and the BLK output will be 1. $\,$

Transparent is specified by setting the TOK bit to 1. (The BLK output will go to the low level.)

Display Structure

The display screen consists of a 40-character × 15-line grid.

QVGA mode (12×18 dot characters)

40-character \times 13-line QVGA panel (480 \times 234)

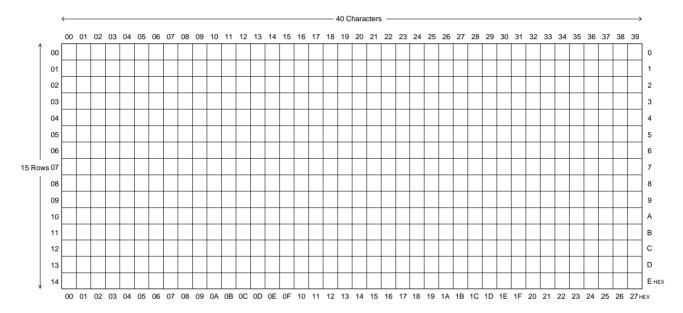
WVGA mode (12×16 dot characters)

33-character \times 15-line WVGA panel (800 \times 480)

Up to a maximum of 600 characters can be displayed.

If the character size is increased, the number of characters that can be displayed will decrease to be fewer than 600 characters

Display memory is addressed by specifying a line address (0 to 14 (decimal) and a character position address (0 to 39 (decimal)).



Display Structure (Display memory address)

Operational Description

Command transfer method

Overview

(1) Commands are transferred in 8-bit units, LSB first.

Always send a first byte and a second byte (16 bits).

(2) Command 10 (Main RAM write)

Command 11 (Wallpaper write)

Command 71 (Color table write)

When these commands specify continuous mode (RM2, 1 RM3), the IC is locked in continuous write mode. (Continuous write mode is cleared by setting the \overline{CS} pin high.)

Writing data to VRAM

(1) Write start address specification

Use command 00 to set the write start address.

V3:0: Vertical direction, H5:0: Horizontal direction

(2) Data write

Continuous write mode differs depending on the write mode specification. (RM1, RM2)

- 1. Normal (RM2 = 0, RM1 = 0: initial state) *Continuous mode not used*
 - -- COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 command wait state --
- 2. Write continuous (RM2 = 0, RM1 = 1): Mode 2 COM10-1 10-2-1 10-2-2 10-2-3 10-2-4
- 3. Write continuous (RM2 = 1, RM1 = 0): Mode 3 COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-3 10-2-4
- 4. Write continuous (RM2 = 1, RM1 = 1): Mode 4

 COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 10-2-2 10-2-3 10-2-4
- *: In modes 2, 3, and 4, the IC remains locked in continuous write mode until the CS pin is set high.
 - The write address is automatically incremented.
 - The write address is retained unless the IC is reset or a new write address is issued.

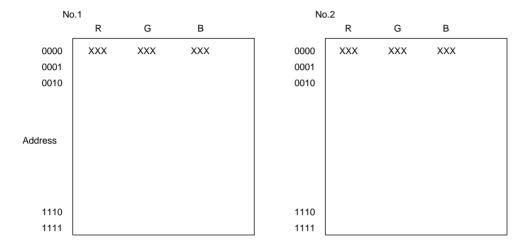
Color table write

(1) Write start address specification

Use command 70 to set the color table write start address.

CTN

:1: Color table specification (No.1, No.2), CTA3:0: Address specification



(2) Data write

Continuous write mode differs depending on the write mode specification. (RM3)

- 1. Normal (RM3 = 0: initial state) *Continuous mode not used*
 - -- COM71-1 71-2-1 71-2-2 command wait state ---
- 2. Write continuous (RM3 = 1) mode

- *: In mode 2, the IC remains locked in continuous write mode until the CS pin is set high.
 - The write address is automatically incremented.
 - The write address is retained unless the IC is reset or a new write address is issued.

Display Format

Color specification related items

(1) When a character is specified

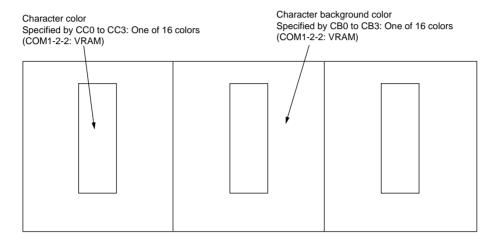
Color specification for the character color (character area) and character background color (outside the character area)

Character color: One of 16 colors

Character background color: One of 16 colors

Color tables: Table No. 1 or No. 2 specified by CT1:0. (COM1-2-3: VRAM)

→ One of 32 types



(2) When a graphic is specified

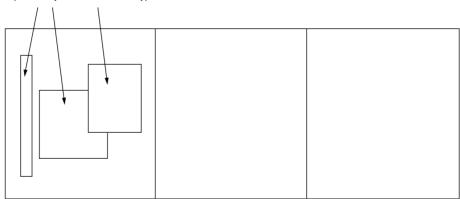
Color is specified in dot units $(12 \times 18 \text{ or } 12 \times 16)$

One of 16 colors (FROM)

Color tables: Table No. 1 or No. 2 specified by CT1:0. (COM1-2-3: VRAM)

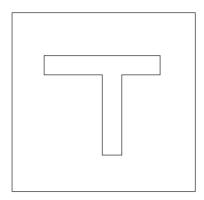
→ One of 32 types

Specified by FROM: One of 16 types



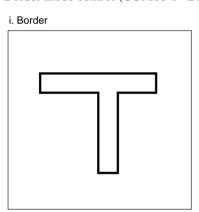
Display control related items

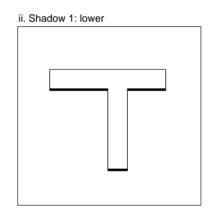
- (1) Blinking: In character units
 - 1. Normal at1 = 0 (COM1-2-1: VRAM)



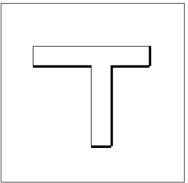
2. Blinking at 1 = 1
Display alternates between normal and transparent with the blinking period. (COM21-2: BK1, 0)

- (2) Border display: Only valid for font specified characters
 - 1. Border color: One of 16 colors (COM60-2 EGC3 to 0)
 Color table specification (COM60-2 EGCT0)
 → One of 32 types
 - 2. Border mode control (COM60-1 BLK1, 0)





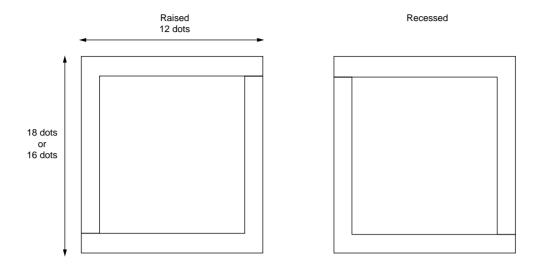
iii. Shadow 2: lower + right



(3) Character size: Specified in line units

The character size is specified as 1x to 4x independently for the vertical and horizontal directions. (COM40-2)

Box display (raised/recessed)



- (1) Raised/recessed specification: In character units (COM10-2-1 BXS)
- (2) Left side displayed/undisplayed specification: in character units (COM10-2-1 BXL)
- (3) Right side displayed/undisplayed specification: in character units (COM10-2-1 BXR)
- (4) Upper side displayed/undisplayed specification: in character units (COM10-2-1 BXU)
- (5) Lower side displayed/undisplayed specification: in character units (COM10-2-1 BXD)
- (6) Color specification: In line units

COM50 (Upper side)

COM51 (Lower side)

BXUC3:0: One of 16 colors

BXDC3:0: One of 16 colors

Color table specification

BXUCT0

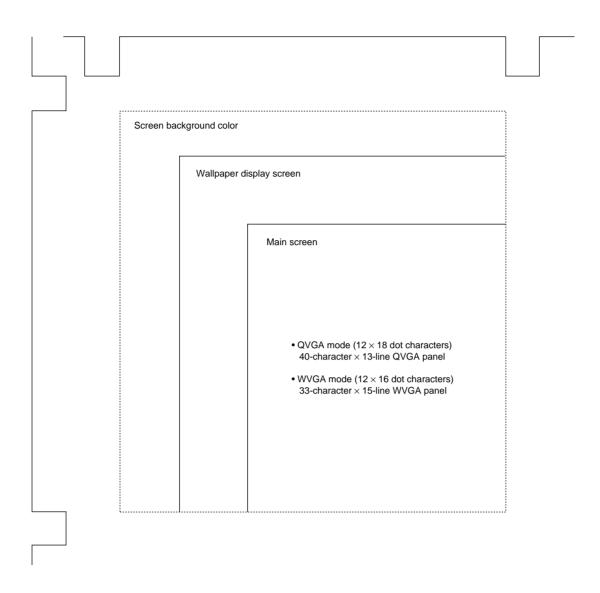
BXDCT0

→ One of 32 types

Dot width specification: 1 or 2 dots

Each of left, right, upper, and lower can be specified independently. (BXLW BXRW BXUW BXDW)

Screen structure

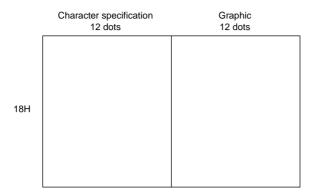


- For each screen: Display on/off (transparent) can be specified independently.
- For each screen: The display start position can be specified independently.

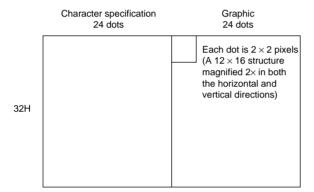
 The wallpaper display screen and the main screen are displayed up to the horizontal direction start position. (The XXX clock is required.)

Display format

(1) QVGA



(2) WVGA



ROM structure

Internal ROM (512 characters)

(1) Character font

QVGA: 12×18 -dot structure

WVGA: 24×32 -dot structure, i.e. 12×16 times 4

(2) Graphics

CQVGA: 12×18 -dot structure

WVGA: 12×16 -dot structure, i.e. displayed magnified $2 \times$ in both the horizontal and vertical directions.

Note that the contents of ROM differs for QVGA and WVGA. (That is, different ROMs for QVGA and WVGA must be created.)

• Data

Unused

D15 to D12, D11 to D0

Used

External ROM (2048 characters)

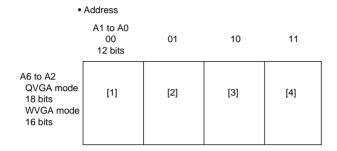
(1) Conditions

Use a 16-bit 4M ROM with an access time less than 3 times the dot clock period

Example: DCLK = $50 \text{ MHz} = 20 \text{ ns period} \times 3 = \text{under } 60 \text{ ns}$

DCLK = $10 \text{ MHz} = 100 \text{ ns period} \times 3 = \text{under } 300 \text{ ns}$

(2) ROM map



A17 to A7 (10 bits) = 2048 characters = character codes

- (3) Display appearance
 - 1. QVGA: 1 character = 12×18 dots

Character font: [1]

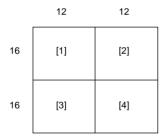
Graphics: [1] + [2] + [3] + [4]

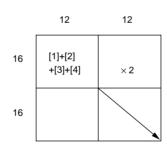
2. WVGA: 1 character = 12×16 dots

Character font: [1] [2]

[3] [4]

Graphics: ([1] + [2] + [3] + [4]) displayed magnified $2 \times$ in both the horizontal and vertical directions.





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