

SANYO**LC74721, LC74721M****On-screen Video Display Controllers
for NTSC or PAL-M****Overview**

The LC74721 and LC74721M are CMOS, video display controllers for superimposing text and low-level graphics onto an NTSC or PAL-M compatible television receiver. Up to 240, 8 × 8-pixel characters can be displayed under microprocessor control on a 24-character by 10-line display.

The LC74721 and LC74721M feature selectable pixel width and height, and 64 vertical and 64 horizontal display start positions. It also features a flashing enable bit for each character position.

The LC74721 and LC74721M operate from a 5V supply. The LC74721 is available in 24-pin DIPs, and the LC74721M, in 24-pin MFPs.

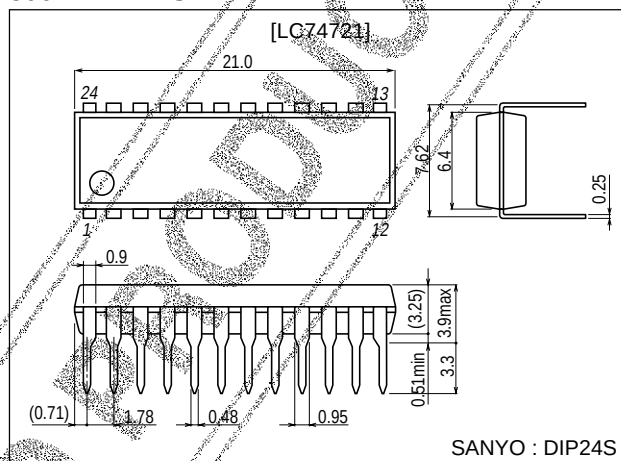
Features

- Complete text and graphics vide overlay circuitry.
- 64-character internal character generator ROM.
- 8 × 8-pixel characters.
- Three pixel widths and three pixel heights.
- Selectable background color.
- Built-in synchronization check and separation circuitry.
- Approximately 0.5 or 1 s period character flashing option.
- NTSC or PAL-M format compatibility.
- 8-bit serial input format.
- 5V supply.
- 24-pin plastic DIP (300mil) and 24-pin plastic MFP (375mil).

Package Dimensions

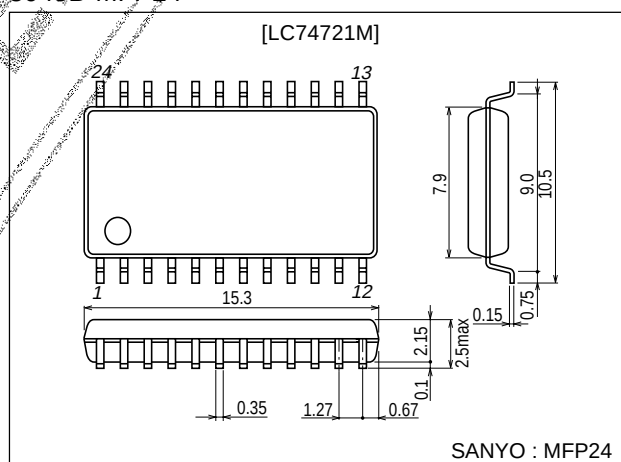
unit:mm

3067A-DIP24S



unit:mm

3045B-MFP24



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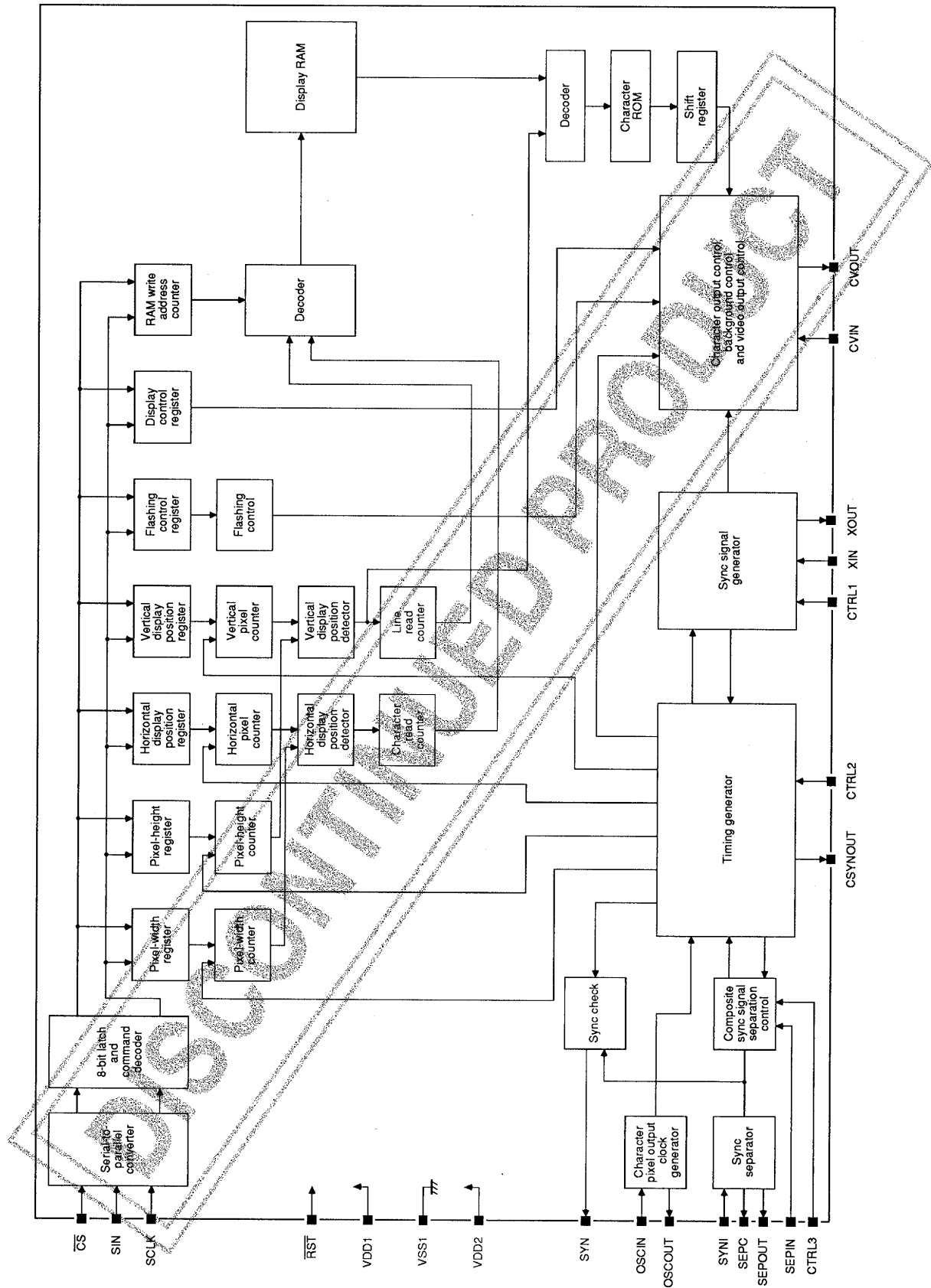
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Block Diagram



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Pin Functions

Number	Name	Description
1	V _{SS1}	Ground
2	XIN	Internal sync signal crystal oscillator capacitor connections or external clock input (2f _{SC} or 4f _{SC})
3	XOUT	
4	CTRL1	Clock input mode select. HIGH for external clock input mode, and LOW for crystal oscillator mode.
5	CSYNOUT	Composite synchronization signal output. During reset (RST LOW), crystal oscillator clock is output. No output for internal reset command
6	OSCIN	LC oscillator input. LC circuit for pixel clock generation character output
7	OSCOUT	LC oscillator output. LC circuit for pixel clock generation character output
8	SYNC	External synchronization signal check output. During reset (RST LOW), pixel clock is output. No output for internal reset command
9	$\overline{CS}$	Serial data input enable when LOW, with pull-up resistance
10	SCLK	Clock input for serial data input, with pull-up resistance
11	SIN	Serial data input, with pull-up resistance
12	V _{DD2}	Power supply for composite video image signal level modulation (for analog system)
13	CVOUT	Composite video image signal output
14	NC	No connection
15	CVIN	Composite video image signal input
16	V _{DD1}	5V power supply for digital system
17	SYNCIN	Synchronization separation circuit input. If internal sync separation circuit is not used, use SYNCIN to input an external horizontal or composite synchronization signal
18	SEPC	Synchronization separation circuit modulator capacitor connection. Leave open if not used
19	SEPOUT	Composite synchronization separation circuit output. Outputs SYNCIN signal if internal sync separation is not used
20	SEPIN	Vertical synchronization signal input. Tie to V _{DD1} if not used
21	CTRL2	NTSC/PAL-M sync signal generation method select input. LOW for NTSC
22	CTRL3	SEPIN input control. VSYNC input signal when LOW
23	RST	System reset input, with pull-up resistance
24	V _{DD1}	5V power supply for digital system

Specifications

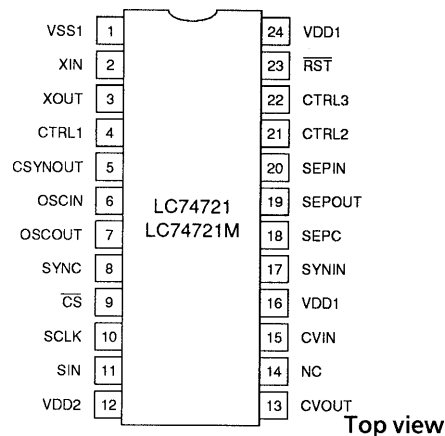
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD1} V _{DD2}		V _{SS} -0.3 to V _{SS} +7.0	V
Input voltage	V _I		V _{SS} -0.3 to V _{DD} +0.3	V
Output voltage	V _O		V _{SS} -0.3 to V _{DD} +0.3	V
Allowable power dissipation	P _D	T _a = 25°C	350	mW
Operating temperature	T _{opr}		-30 to +70	°C
Storage temperature	T _{stg}		-40 to +125	°C

Reommeded Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Logic supply voltage	V _{DD1}		5.0	V
Analog supply voltage	V _{DD2}		5.0	V
Logic supply voltage range	V _{DD1}		4.5 to 5.5	V
Analog supply voltage range	V _{DD2}		4.5 to (1.27V _{DD1})	V

Pin Assignment



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Electrical Characteristics at Ta = -30 to +70°C, V_{DD1} = 5V, unless otherwise noted

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V _{DD1} logic supply current	I _{DD1}	All outputs open, 7.159MHz crystal oscillator, 8MHz LC oscillator			15	mA
V _{DD2} analog supply current	I _{DD2}	V _{DD2} =5V			20	mA
CVIN input leakage current	I _{L1}				1	μA
CVOUT output leakage current	I _{L2}				1	μA
CTRL1, CTRL2, CTRL3 and OSCIN low-level input current	I _{IL}	V _I =V _{SS1}	-1.0			μA
RST, CS, SIN, SCLK, CTRL1, SEPIN, CTRL2 and CTRL3 high-level input current	I _{IH}	V _I =V _{DD1}			1.0	μA
RST, CS, SIN and SCLK low-level input voltage	V _{IL1}		V _{SS} -0.3		0.2V _{DD1}	V
CTRL1, CTRL2, CTRL3 and SEPIN low-level input voltage	V _{IL2}		V _{SS} -0.3		0.3V _{DD1}	V
RST, CS, SIN and SCLK high-level input voltage	V _{IH1}		0.8V _{DD1}		V _{DD1} +0.3	V
CTRL1, CTRL2, CTRL3 and SEPIN high-level input voltage	V _{IH2}		0.7V _{DD1}		V _{DD1} +0.3	V
CVIN composite video input voltage	V _{I1}	Measured peak to peak		2.0		Vp-p
SYNCIN composite video input voltage	V _{I2}	Measured peak to peak		2.0	2.5	Vp-p
XIN input voltage	V _{I3}	External clock input, f _{IN} =2f _{SC} or 4f _{SC}	0.20		5.0	Vp-p
CSYNOUT, SYNC and SEPOUT low-level output voltage	V _{OL1}	V _{DD1} =4.5V, I _{OL} =1.0 mA			1.0	V
CSYNOUT, SYNC and SEPOUT high-level output voltage	V _{OH1}	V _{DD1} =4.5V, I _{OH} =-1.0 mA	3.5			V
CVOUT sync voltage	V _{SN}	See note 1.	0.70	0.82	0.94	V
		See note 2.	0.87	0.99	1.11	V
CVOUT pedestal voltage	V _{PD}	See note 1.	1.27	1.39	1.51	V
		See note 2.	1.44	1.56	1.68	V
CVOUT low-level color burst voltage	V _{CBL}	See note 1.	0.98	1.10	1.22	V
		See note 2.	1.15	1.27	1.39	V
CVOUT high-level color burst voltage	V _{CBH}	See note 1.	1.58	1.70	1.82	V
		See note 2.	1.74	1.86	1.98	V
CVOUT low-level background color voltage	V _{RS1}	See note 1.	1.42	1.54	1.66	V
		See note 2.	1.59	1.71	1.83	V
CVOUT high-level background color voltage	V _{RS2}	See note 1.	1.94	2.06	2.18	V
		See note 2.	2.11	2.23	2.35	V
CVOUT border voltage	V _{BK}	See note 1.	1.50	1.62	1.74	V
		See note 2.	1.68	1.80	1.92	V
CVOUT character voltage	V _{CHA}	See note 1.	2.61	2.73	2.85	V
		See note 2.	2.80	2.92	3.04	V
RST, CS, SIN and SCLK pull-up resistance	R _{PU}	Depends on optional settings at pins	25	50	90	kΩ
XIN and XOUT oscillator frequency	f _{OSC1}	NTSC (2f _{SC})		7.159		MHz
		NTSC (4f _{SC})		14.318		MHz
		PAL-M (4f _{SC})		14.302		MHz
OSCIN and OSCOUT oscillator frequency	f _{OSC2}	LC oscillator	5		10	MHz

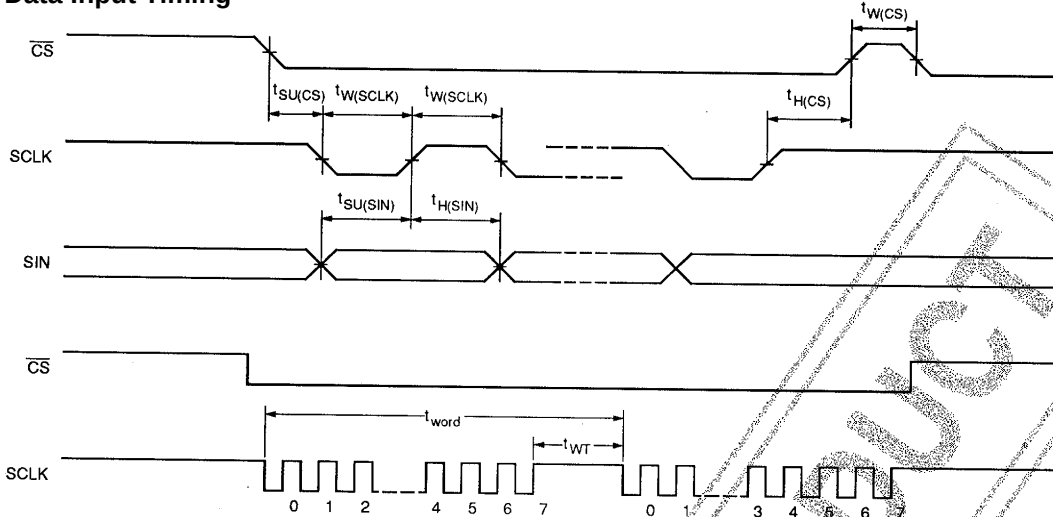
Notes

1. CV_{OUT} at V_{DD1} = V_{DD2} = 5V, 0.8V sync level
2. CV_{OUT} at V_{DD1} = V_{DD2} = 5V, 1.0V sync level

Timing Characteristics at Ta = -30 to +75°C, V_{DD1} = 5 ± 0.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCLK input pulsewidth	t _W (SCLK)		200			ns
CS high-level input pulsewidth	t _W (CS)		1			μs
CS input setup time	t _{SU} (CS)		200			ns
SIN data input setup time	t _{SU} (SIN)		200			ns
CS input hold time	t _H (CS)		2			μs
SIN data input hold time	t _H (SIN)		200			ns
8-bit data word write time	t _{WORD}		4.2			μs
RAM data write time	t _{WT}		1			μs

Serial Data Input Timing



Display Control Features and Characteristics

Display Control Command Structure

The display control commands, COMMAND0 to COMMAND5, are shifted in 8-bit serial units. The first byte of a command consists of an identification code and data. The second byte consists of data only. Once the command identification code in byte 1 has been written, it is saved until

the next time the first byte is written. If COMMAND1 is written, the display character write mode begins and the first byte does not change. When $\overline{CS}$ is HIGH, COMMAND0 is set.

Display Control Command Data

Command	First byte								Second byte							
	Command code				Data or register storing data				Data or register storing data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND00 Display memory (VRAM) write address setting command	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND01 Display character data write command	1	0	0	1	0	0	0	0	at	0	C5	C4	C3	C2	C1	C0
COMMAND02 Vertical display position and character size setting command	1	0	1	0	VS21	VS20	VS11	VS10	0	FS	VP5	VP4	VP3	VP2	VP1	VP0
COMMAND03 Horizontal display position and character size setting command	1	0	1	1	HS21	HS20	HS11	HS10	0	LC	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND04 Display control setting command	1	1	0	0	ST MOD	CB	OSC STP	SYS RST	0	0	NON	EG	BK1	BK0	RV	DSP ON
COMMAND05 Synchronization signal control setting command	1	1	0	1	PH1	PH0	BCL	INT	0	RN2	RN1	RN0	SN3	SN2	SN1	SN0

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COMMAND0: Display Memory Write Address Setting Command

COMMAND0: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	V0	0	Display memory address 0 to 9H	
		1		
1	V1	0		
		1		
2	V2	0		
		1		
3	V3	0		
		1		
4		0	COMMAND0 identification code	
5		0		
6		0		
7		1		

COMMAND0: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	H0	0	Display memory address 0 to 17H	
		1		
1	H1	0		
		1		
2	H2	0		
		1		
3	H3	0		
		1		
4	H4	0		
		1		
5		0	Second byte identification bit	
6		0		
7		0		

Note

On system reset with $\overline{\text{RST}}$, the status of all registers is set to 0.

COMMAND1: Display Character Data Write Command

COMMAND1: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0		0	COMMAND1 identification code	After command is input, display character data write mode is set until $\overline{\text{CS}}$ is set HIGH
1		0		
2		0		
3		0		
4		1		
5		0		
6		0		
7		1		

COMMAND1: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	C0	0	Character code 0 to 3FH	
		1		
1	C1	0		
		1		
2	C2	0		
		1		
3	C3	0		
		1		
4	C4	0		
		1		
5	C5	0		
		1		
6		0		
7	at	0	Character attribute OFF	
		1	Character attribute ON	

Note

On system reset with $\overline{\text{RST}}$, the status of all registers is set to 0.

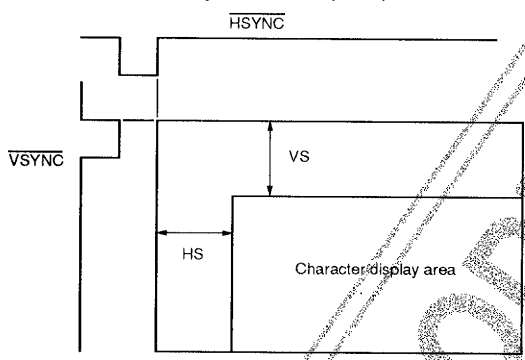
COMMAND2: Vertical Display Position and Character Size Setting Command

COMMAND2: first byte

DA0 to DA7	Register name	Register Contents			Remarks														
		Status	Function																
0	VS10	0	<table><tr><th>VS11</th><th>VS10</th><th>Height</th></tr><tr><td>0</td><td>0</td><td>1H/pixel</td></tr><tr><td>0</td><td>1</td><td>2H/pixel</td></tr><tr><td>1</td><td>0</td><td>3H/pixel</td></tr><tr><td>1</td><td>1</td><td>1H/pixel</td></tr></table>		VS11	VS10	Height	0	0	1H/pixel	0	1	2H/pixel	1	0	3H/pixel	1	1	1H/pixel
		VS11	VS10	Height															
0	0	1H/pixel																	
0	1	2H/pixel																	
1	0	3H/pixel																	
1	1	1H/pixel																	
1	VS11	0																	
		1																	
2	VS20	0	<table><tr><th>VS21</th><th>VS20</th><th>Height</th></tr><tr><td>0</td><td>0</td><td>1H/pixel</td></tr><tr><td>0</td><td>1</td><td>2H/pixel</td></tr><tr><td>1</td><td>0</td><td>3H/pixel</td></tr><tr><td>1</td><td>1</td><td>1H/pixel</td></tr></table>		VS21	VS20	Height	0	0	1H/pixel	0	1	2H/pixel	1	0	3H/pixel	1	1	1H/pixel
		VS21	VS20	Height															
0	0	1H/pixel																	
0	1	2H/pixel																	
1	0	3H/pixel																	
1	1	1H/pixel																	
3	VS21	0																	
		1																	
4		0	COMMAND2 identification code																
5		1																	
6		0																	
7		1																	

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COMMAND2: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	VP0	0	Initial vertical coordinate position determined by $VS = H \times \left(2 \sum_{n=0}^5 2^n VP_n \right)$ where H is the horizontal synchronization pulse period 	The initial vertical coordinate position is set in 6 bits, VP0 to VP5, where the lsb, VP0, corresponds to 2H
		1		
1	VP1	0		
		1		
2	VP2	0		
		1		
3	VP3	0		
		1		
4	VP4	0		
		1		
5	VP5	0		
		1		
6	FS	0	2f _{SC} crystal oscillator frequency	
		1	4f _{SC} crystal oscillator frequency	
7		0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND3: Horizontal Display Position and Character Size Setting Command

COMMAND3: first byte

DA0 to DA7	Register name	Register Contents				Remarks							
		Status	Function										
0	HS10	0	<table><tr><td>HS11</td><td>HS10</td><td>Width</td></tr><tr><td>0</td><td>0</td><td>1T_C/pixel</td></tr></table>			HS11	HS10	Width	0	0	1T _C /pixel	First row horizontal character size	
		HS11	HS10	Width									
0	0	1T _C /pixel											
1	<table><tr><td>0</td><td>1</td><td>2T_C/pixel</td></tr><tr><td>1</td><td>0</td><td>3T_C/pixel</td></tr><tr><td>1</td><td>1</td><td>1T_C/pixel</td></tr></table>			0	1	2T _C /pixel	1	0	3T _C /pixel	1	1		1T _C /pixel
0	1	2T _C /pixel											
1	0	3T _C /pixel											
1	1	1T _C /pixel											
1	HS11	0											
		1											
2	HS20	0	<table><tr><td>HS21</td><td>HS20</td><td>Width</td></tr><tr><td>0</td><td>0</td><td>1T_C/pixel</td></tr></table>			HS21	HS20	Width	0	0	1T _C /pixel	Second row horizontal character size	
		HS21	HS20	Width									
0	0	1T _C /pixel											
1	<table><tr><td>0</td><td>1</td><td>2T_C/pixel</td></tr><tr><td>1</td><td>0</td><td>3T_C/pixel</td></tr><tr><td>1</td><td>1</td><td>1T_C/pixel</td></tr></table>			0	1	2T _C /pixel	1	0	3T _C /pixel	1	1		1T _C /pixel
0	1	2T _C /pixel											
1	0	3T _C /pixel											
1	1	1T _C /pixel											
3	HS21	0											
		1											
4		1	COMMAND3 identification code										
5		1											
6		0											
7		1											

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COMMAND3: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	HP0	0	The initial horizontal coordinate position is given by $HS = T_C \times \left(2 \sum_{n=0}^5 2^n HP_n \right)$ where T_C is the OSCIN and OSCOUT operation mode oscillation period	The initial horizontal coordinate position is set in 6 bits, HP0 to HP5, where the lsb, HP0, corresponds to $2T_C$
		1		
1	HP1	0		
		1		
2	HP2	0		
		1		
3	HP3	0		
		1		
4	HP4	0		
		1		
5	HP5	0		
		1		
6	LC	0	LC oscillator dot clock	Selects the dot clock used for the character display transverse direction
		1	Crystal oscillator dot clock	
7		0	Second byte identification bit	

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND4: Display Control Setting Command

COMMAND4: first byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	SYSRST	0	Resets all registers and turns the display OFF	A system reset also occurs when CS goes LOW
		1		
1	OSCSTP	0	Crystal and LC oscillator stop disable	External sync mode character display
		1	Crystal and LC oscillator circuitry stop enable	
2	CB	0	Color burst signal is output	When BCL is HIGH only
		1	Color burst signal is not output	
3	TSTMOD	0	Normal operating mode	Test mode should not be selected during normal operation
		1	Test mode	
4		0	COMMAND4 identification code	
5		0		
6		1		
7		1		

COMMAND4: second byte

DA0 to DA7	Register name	Register Contents		Remarks
		Status	Function	
0	DSPON	0	Character display OFF	
		1	Character display ON	
1	RV	0	Inverse characters OFF	
		1	Inverse characters ON	
2	BK0	0	Blinking OFF	When blinking inverse characters, characters alternate between normal and inverse
		1	Blinking ON	
3	BK1	0	Blinking period 0.5 s	Selects blinking period
		1	Blinking period 1.0 s	
4	EG	0	Border OFF	Interlaced/non-interlaced switching
		1	Border ON	
5	NON	0	Interlaced scanning, 262.5 H/field	
		1	Non-interlaced scanning, 263 H/field	
6		0	Second byte identification bit	
7		0		

Note

On system reset with $\overline{RST}$, the status of all registers is set to 0.

COMMAND5: Synchronization Signal Control Setting Command

COMMAND5: first byte

DA0 to DA7	Register name	Register Contents				Remarks														
		Status	Function																	
0	INT	0	External synchronization			Switches between external and internal synchronization														
		1	Internal synchronization																	
1	BCL	0	Background color available			Only available with internal synchronization														
		1	Background color not available (background level only set)																	
2	PH0	0	<table><tr><td>PH1</td><td>PH0</td><td>Background color's phase</td></tr><tr><td>0</td><td>0</td><td>$\pi/2$</td></tr><tr><td>0</td><td>1</td><td>π</td></tr><tr><td>1</td><td>0</td><td>$3\pi/2$</td></tr><tr><td>1</td><td>1</td><td>In phase</td></tr></table>			PH1	PH0	Background color's phase	0	0	$\pi/2$	0	1	π	1	0	$3\pi/2$	1	1	In phase
		PH1				PH0	Background color's phase													
0	0	$\pi/2$																		
0	1	π																		
1	0	$3\pi/2$																		
1	1	In phase																		
3	PH1	0				Phase selection. In PAL-M mode, there is only one background color (blue-black). Otherwise, there are 4 types														
		1																		
4		1	COMMAND5 identification code																	
		0																		
5		0																		
6		1																		
7		1																		

COMMAND5: second byte

DA0 to DA7	Register name	Register Contents					Remarks	
		Status	Function					
0	SN0	0					External sync signal detection control. Determines when the signal goes from ON to OFF. Selects the sampling period, in units of the horizontal sync signal cycle (1H), for which the sync continues and cannot be detected.	
		1	SN3	SN2	SN1	SN0		Detection frequency
1	SN1	0	0	0	0	No detection		
		1	0	0	0	1		32 times
2	SN2	0	0	0	1	0		64 times
		1	0	1	0	0		128 times
3	SN3	0	1	0	0	0		256 times
		1						
4	RN0	0	RN2	RN1	RN0	Detection frequency		External sync signal detection control. Determines when the signal goes from OFF to ON. Selects the sampling period, in units of the horizontal sync signal cycle (1H), for which the sync continues and can be detected.
		1	0	0	0	0 times		
5	RN1	0	0	0	1	4 times		
		1	0	1	0	8 times		
6	RN2	0	1	0	0	16 times		
		1						
7		0	Second byte identification bit					

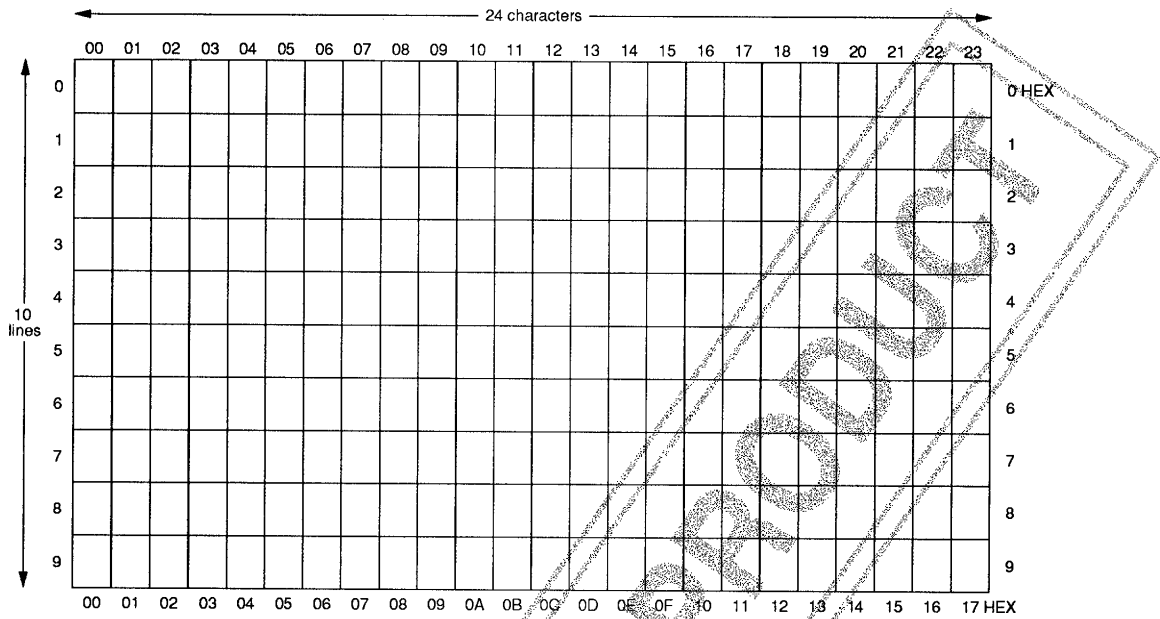
Note

On system reset with $\overline{\text{RST}}$, the status of all registers is set to 0.

Display Configuration

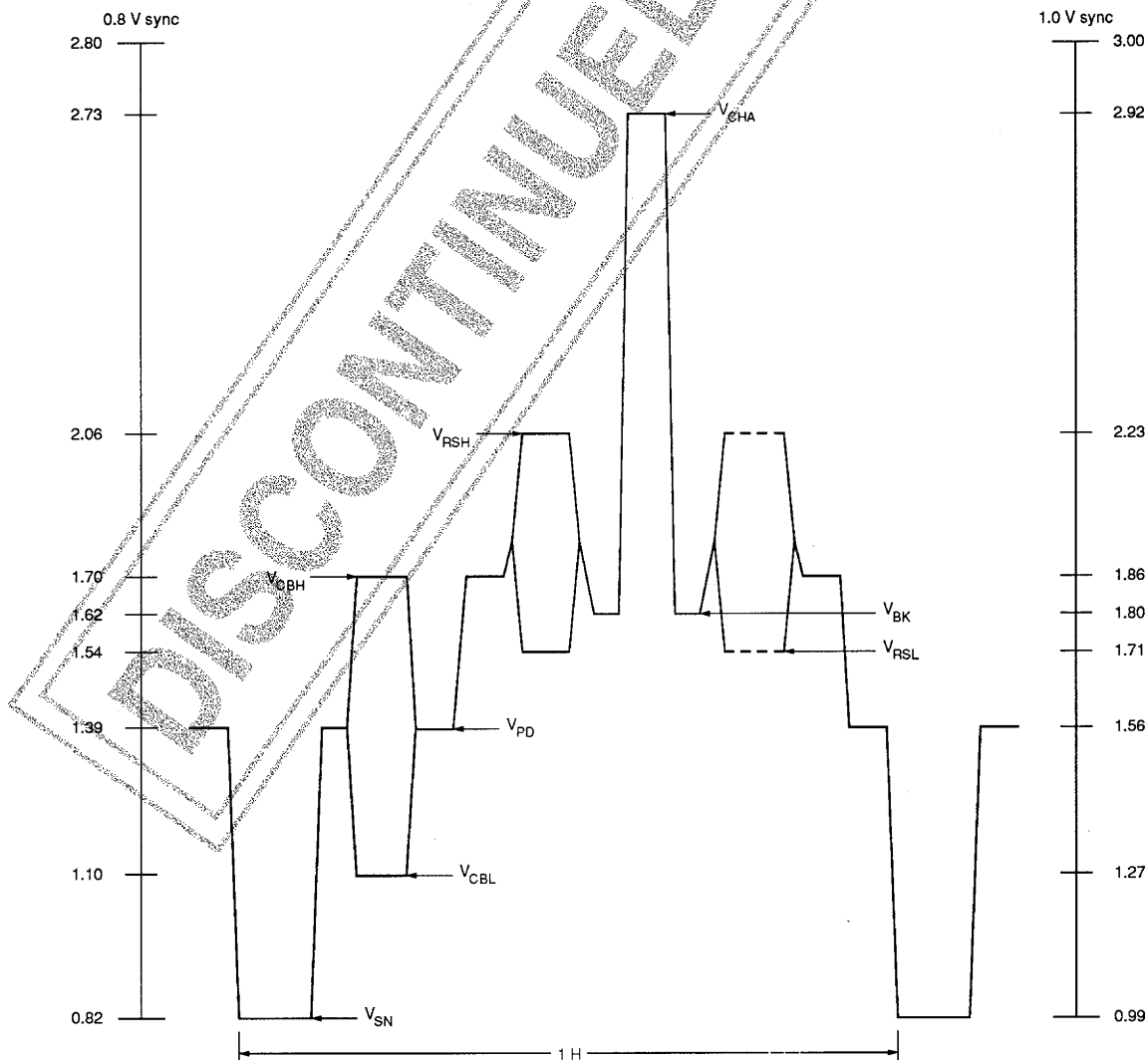
The display is 24 characters by 10 rows large. Up to 240 characters can be displayed, unless the character size is expanded. The display memory address is set as a row address in the range 0 to 9 and a column address in the range

0 to 23.



Composite Video Output

CVOUT Output Waveform ($V_{DD2}=5.00V$)



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Output voltage level	Symbol	Output voltage at 0.8V sync (V)	Output voltage at 1.0V sync (V)
Character	V _{CHA}	2.73	2.92
High-level background color	V _{RSH}	2.06	2.23
High-level color burst	V _{CBH}	1.70	1.86
Low-level background color	V _{RSL}	1.54	1.71
Border	V _{BK}	1.62	1.80
Pedestal	V _{PD}	1.39	1.56
Low-level color burst	V _{CBL}	1.10	1.27
Sync	V _{SN}	0.82	0.99

Note

V_{DD2} = 5.00V

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