

**LC74711****Controller LSI for On-screen Displays****Preliminary****Overview**

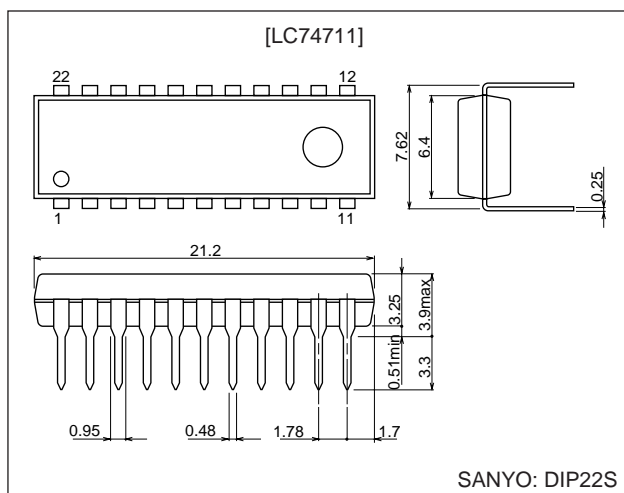
The LC74711 is a CMOS LSI for applications involving microcomputer control of on-screen character and graphics displays. Built-in character ROM supplies 128 alphanumeric characters and each character is generated in a 12 by 18 pixel format. The display is capable of supporting a maximum of 288 characters within a 24 characters by 12 line array.

**Functions and Applications**

- (1) Screen construction:  
24 characters X 12 lines
- (2) Number of characters displayed:  
Maximum 288 characters capacity
- (3) Display control ROM (line ROM):  
64 lines (line unit control: 24 character construction)
- (4) Display RAM:  
176 characters (supporting extended character selection)
- (5) Character construction: 12 (horizontal) X 18 (vertical) pixels
- (6) Character set: 128 types of characters
- (7) Character size:  
4 horizontal types and 4 vertical types
- (8) Display starting position: 64 types horizontally and 64 types vertically
- (9) Blinking: Character units
- (10) Blinking types: 2 types with approximate 1.0 s and 0.5 s cycles and 3-type selection for 25%, 50% and 75% duty
- (11) Blanking: Font complete blanking (12 X 18 pixels)
- (12) Background color: 8 background tints (during internal synchronizing operation: 4 fsc when using crystal oscillator)
- (13) External control input: Serial data input
- (14) Synchronizing signal: Internal synchronizing, supports external synchronizing changeover
- (15) Built-in synchronizing separator circuit
- (16) Video output: NTSC system composite video output
- (17) Superimpose: Characters superimposed over composite video output
- (18) Package: DIP-22S

**Package Dimensions**

unit : mm

**3059-DIP22S**

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## Specifications

### Absolute Maximum Ratings

Item	Symbol	Conditions/Pins	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$	$V_{DD1}, V_{DD2}$	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Maximum input voltage	$V_{IN\ max}$	All input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Maximum output voltage	$V_{OUT\ max}$		$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Allowable power dissipation	$P_d\ max$	$T_a = 25^{\circ}C$	300	mW
Operating temperature	$T_{opr}$		$-30$ to $+70$	$^{\circ}C$
Storage temperature	$T_{stg}$		$-40$ to $+125$	$^{\circ}C$

### Allowable Operating Ranges at $T_a = -30$ to $+70^{\circ}C$

Item	Symbol	Conditions/Pins	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD1}$	$V_{DD1}$ pin	4.5	5.0	5.5	V
	$V_{DD2}$	$V_{DD2}$ pin	4.5	5.0	$1.27V_{DD1}$	V
Input "H" level voltage	$V_{IH}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, SEPIN pin	$0.8V_{DD1}$		$V_{DD1}+0.3$	V
Input "L" level voltage	$V_{IL}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, SEPIN pin	$V_{SS}-0.3$		$0.2V_{DD1}$	V
Composite video input voltage	$V_{IN1}$	CV <sub>IN</sub> pin		$2V_{P-P}$		V
	$V_{IN2}$	SYNI pin		$2V_{P-P}$	$2.5V_{P-P}$	
Oscillation frequency	$F_{OSC1}$	Xtal oscillation pin (2 fsc)		7.159		MHz
	$F_{OSC2}$	Xtal oscillation pin (4 fsc)		14.318		MHz
	$F_{OSC3}$	LC oscillation pin (when using LC oscillation)	5	7	10	MHz

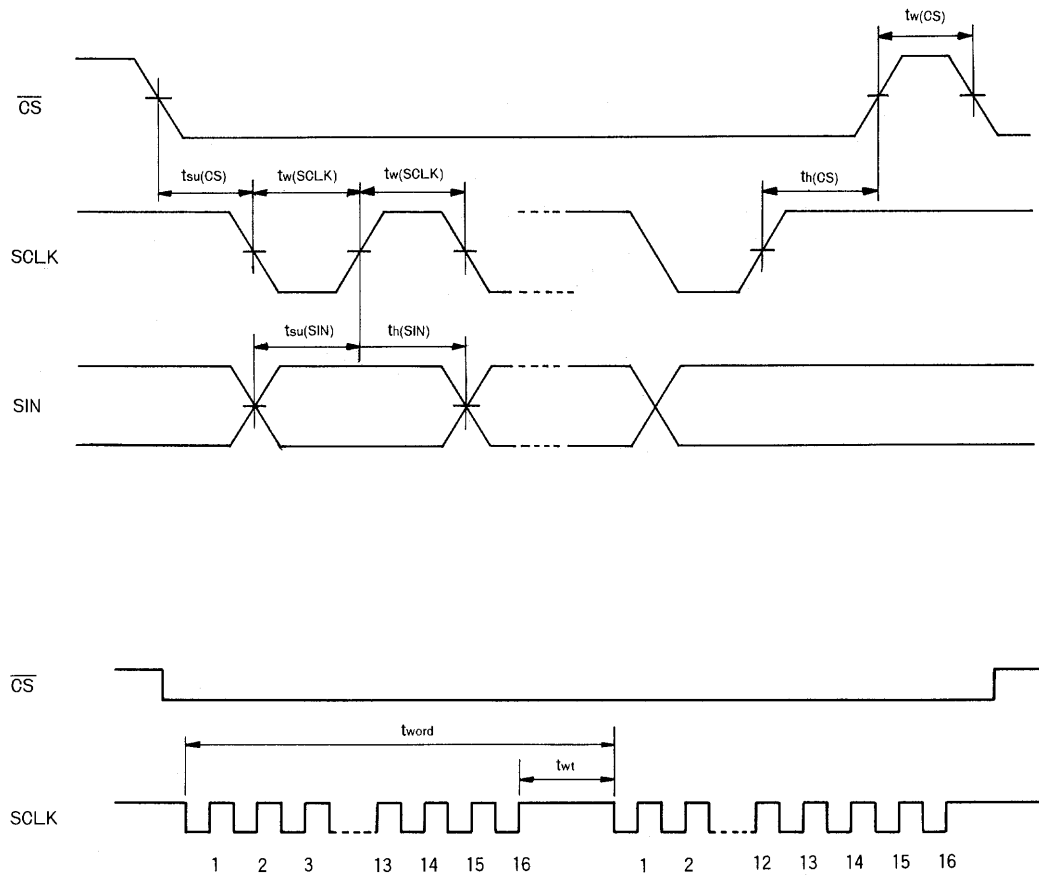
### Electrical Characteristics at $T_a = -30$ to $+70^{\circ}C$ , default of $V_{DD1} = 5$ V

Item	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
Output off leak current	$I_{leak}$	CV OUT pin				10	$\mu A$
Output "H" level voltage	$V_{OH1}$	SEP OUT pin	$V_{DD1} = 4.5V$ , $I_{OH} = -1.0mA$	3.5			V
Output "L" level voltage	$V_{OL1}$	SEP OUT pin	$V_{DD1} = 4.5V$ , $I_{OL} = 1.0mA$			1.0	V
Input current	$I_{IH}$	$\overline{CS}$ , SIN, $\overline{RST}$ , SCLK, SEPIN pin	$V_{IN} = V_{DD1}$			1	$\mu A$
	$I_{IL}$	OSCIN pin	$V_{IN} = V_{SS}$	-1			$\mu A$
Current consumption during operation	$I_{DD1}$	$V_{DD1}$ pin	All output are OPEN Xtal = 14.318MHz, LC = 7MHz			10	mA
	$I_{DD2}$	$V_{DD2}$ pin	$V_{DD2} = 5.0V$			15	mA

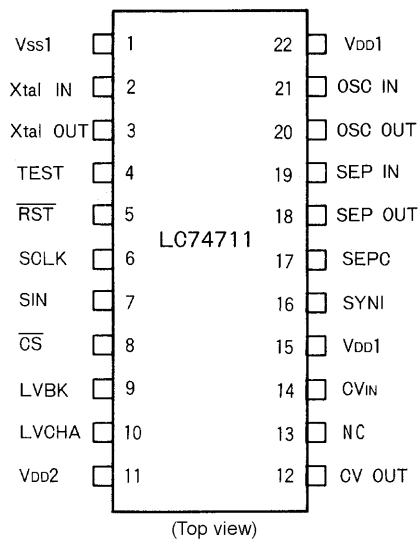
### Timing Characteristics at $T_a = -30$ to $+70^{\circ}C$ , $V_{DD1} = 5 \pm 0.5$ V

Item	Symbol	Conditions/Pins	Ratings			Unit
			min	typ	max	
Input minimum pulse width	$t_w$ (SCLK)	SCLK pin	200			ns
	$t_w$ ( $\overline{CS}$ )	$\overline{CS}$ pin (with $\overline{CS}$ set to "H" period)	1			$\mu s$
Data setup time	$t_{su}$ ( $\overline{CS}$ )	$\overline{CS}$ pin	200			ns
	$t_{su}$ (SIN)	SIN pin	200			ns
Data hold time	$t_h$ ( $\overline{CS}$ )	$\overline{CS}$ pin	2			$\mu s$
	$t_h$ (SIN)	SIN pin	200			ns
Single word and write time	$t_{word}$	16-bit write time	10			$\mu s$
	$t_{wt}$	RAM data write time	1			$\mu s$

## Serial Data Input Timing



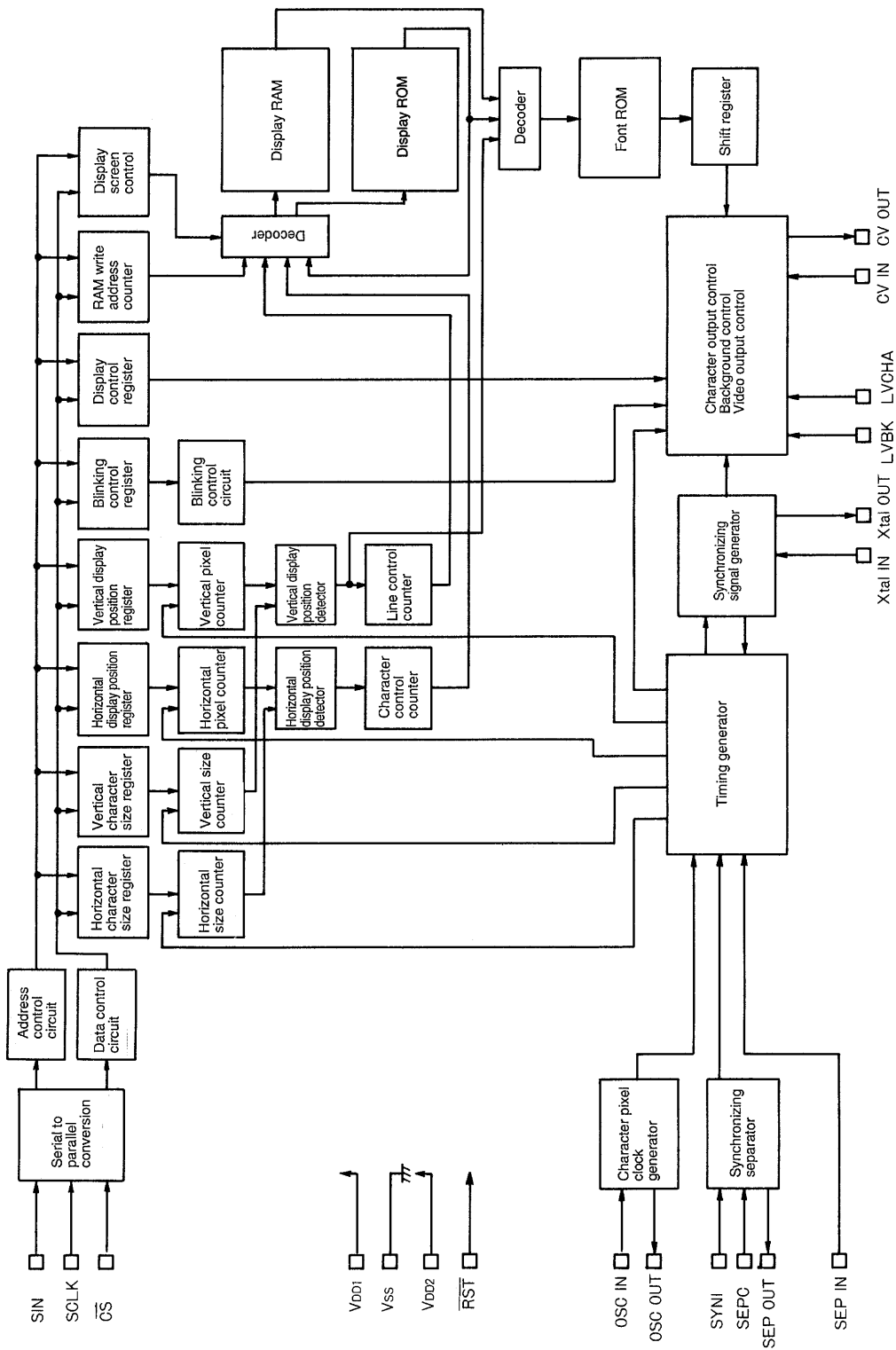
## Pin Assignment



## Pin Functions

Pin No.	Pin Symbol	Pin name	Functions
1	V <sub>SS1</sub>	Ground pin	Pin for connecting to ground (GND) (grounding pin for digital system).
2	Xtal IN	Xtal oscillation pin	Pin for connecting to capacitor or crystal of crystal oscillator for internal synchronizing signal oscillation applications.
3	Xtal OUT		
4	TEST	Test output pin	Pin for test data output.
5	RST	Reset input pin	Pin for system reset input (hysteresis input).
6	SCLK	Clock input pin	Pin for clock input using serial data input (hysteresis input).
7	SIN	Data input pin	Pin for serial data input (hysteresis input). Input in 16-bit units.
8	CS	Enable input pin	Pin for enable input for serial data processing (hysteresis input). "L" serial data input switches to enable.
9	LVBK	Blanking level adjustment input pin	Pin for level input for blanking level adjusting.
10	LVCHA	Character level adjustment input pin	Pin for level input for character level adjusting.
11	V <sub>DD2</sub>	Supply pin	Pin for power supply for adjusting signal level of composite video (power supply for analog system).
12	CV OUT	Video signal output pin	Pin for composite video signal output.
13	NC		Non connection.
14	CV IN	Video signal input pin	Pin for composite video signal input.
15	V <sub>DD1</sub>	Power supply pin	Pin for power supply (+5V).
16	SYNI	Synchronizing separator circuit input pin	Pin for input of separator circuit composite synchronizing signal.
17	SEPC	Synchronizing separator circuit adjustment pin	Pin for adjusting synchronizing separator circuit (connecting capacitor).
18	SEP OUT	Composite synchronizing signal output pin	Pin for output of composite synchronizing signal for synchronizing separator circuit.
19	SEP IN	Vertical synchronizing signal input pin	Pin for input of vertical synchronizing signal and integrating output signal of SEP OUT pin. Applied when connecting an integrating circuit to the SEP OUT pin.
20	OSC OUT	LC oscillation pin	Pin for connecting a capacitor or oscillator coil for pixel clock generation and character output applications.
21	OSC IN		
22	V <sub>DD1</sub>	Power supply pin (+5V)	Pin for power supply (+5V).

System Block Diagram



## Screen Construction

Display mode supports 24 characters and 12 lines.

Maximum number of displayed characters is 288 characters.

When character size is enlarged, the maximum number of characters displayed is reduced to less than 288 characters.

Display line ROM (12-line setting) or display RAM (176 characters).

- Displays using line ROM specify the fixed character set.
- Extended character set are available using display RAM and program setting of characters.

← 24 characters →																							
00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

## Memory Construction (display RAM and control RAM)

Memory addresses and data 16-bit processing.

Addresses 0 (000<sub>HEX</sub>) to 175 (0AF<sub>HEX</sub>) are reserved for display memory (RAM) data.

Addresses 176 (0B0<sub>HEX</sub>) to 191 (0BF<sub>HEX</sub>) are reserved for display control register data.

bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	BLANK	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	<div> <div>Display RAM</div> <div> <div>Blinking</div> <div>Character code</div> </div> </div>
175 (0AFh)	0	0	0	0	0	0	0	0	BLANK	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	
176 (0B0h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	
177 (0B1h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of second line
178 (0B2h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of third line
179 (0B3h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fourth line
180 (0B4h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fifth line
181 (0B5h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of sixth line
182 (0B6h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of seventh line
183 (0B7h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eighth line
184 (0B8h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of ninth line
185 (0B9h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of tenth line
186 (0BAh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eleventh line
187 (0BBh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position Horizontal character size
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position Vertical character size
190 (0BEh)	0	0	0	0	INT/ NON	LC/ XTAL	2fsc/ 4fsc	OSC STP	DSP ON	—	SYS RST	—	—	PHASE 2	PHASE 1	PHASE 0	Video signal and other
191 (0BFh)	0	0	0	0	TST MOD	—	—	BLK 1	BLK 0	—	BLINK 2	BLINK 1	BLINK 0	EX	GB0FF	BC0L	Control register

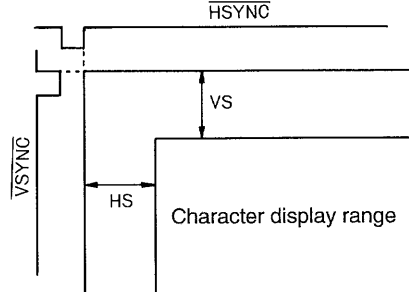
(1) Address 188 (0 BC<sub>HEX</sub>)

DA 0 to C	Register Name	Contents		Notes									
		Setting	Function										
0	HP0 (LSB)	0	When the horizontal display starting position is set to HS, $HS = T_c \times (4 \sum_{n=0}^5 2^n HP_n)$ $T_c$ : represents oscillation cycle of OSC IN and OUT oscillator during operation mode	Horizontal display starting position sets using 6-bit found at HP5 to HP0. Single bit significance is $4T_c$ .									
		1											
1	HP1	0											
		1											
2	HP2	0											
		1											
3	HP3	0											
		1											
4	HP4	0											
		1											
5	HP5 (MSB)	0											
		1											
6	HSZ10	0	<table><tr><td><div>HSZ11 \ HSZ10</div></td><td>0</td><td>1</td></tr><tr><td>0</td><td><math>1T_c/1 \text{ dot}</math></td><td><math>2T_c/1 \text{ dot}</math></td></tr><tr><td>1</td><td><math>3T_c/1 \text{ dot}</math></td><td><math>4T_c/1 \text{ dot}</math></td></tr></table>	<div>HSZ11 \ HSZ10</div>	0	1	0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$	1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$	First line horizontal character size.
<div>HSZ11 \ HSZ10</div>	0	1											
0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$											
1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$											
		1											
7	HSZ11	0											
		1											
8	HSZ20	0	<table><tr><td><div>HSZ21 \ HSZ20</div></td><td>0</td><td>1</td></tr><tr><td>0</td><td><math>1T_c/1 \text{ dot}</math></td><td><math>2T_c/1 \text{ dot}</math></td></tr><tr><td>1</td><td><math>3T_c/1 \text{ dot}</math></td><td><math>4T_c/1 \text{ dot}</math></td></tr></table>	<div>HSZ21 \ HSZ20</div>	0	1	0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$	1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$	Second line horizontal character size.
<div>HSZ21 \ HSZ20</div>	0	1											
0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$											
1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$											
		1											
9	HSZ21	0											
		1											
A	HSZ30	0	<table><tr><td><div>HSZ31 \ HSZ30</div></td><td>0</td><td>1</td></tr><tr><td>0</td><td><math>1T_c/1 \text{ dot}</math></td><td><math>2T_c/1 \text{ dot}</math></td></tr><tr><td>1</td><td><math>3T_c/1 \text{ dot}</math></td><td><math>4T_c/1 \text{ dot}</math></td></tr></table>	<div>HSZ31 \ HSZ30</div>	0	1	0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$	1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$	Lines 3 to 12 horizontal character sizes.
<div>HSZ31 \ HSZ30</div>	0	1											
0	$1T_c/1 \text{ dot}$	$2T_c/1 \text{ dot}$											
1	$3T_c/1 \text{ dot}$	$4T_c/1 \text{ dot}$											
		1											
B	HSZ31	0											
		1											
C	—	0											
		1											

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).



(2) Address 189 (0 BD<sub>HEX</sub>)

DA 0 to C	Register Name	Contents		Notes									
		Setting	Function										
0	VP0 (LSB)	0	<p>When the vertical display starting position is set to VS,</p> $VS = H \times (4 \sum_{n=0}^5 2^n VP_n)$ <p>H: represents horizontal synchronizing pulse cycle</p> 	Vertical display starting position sets using 6-bit found at VP5 to VP0. Single bit significance is 4H.									
1	VP1	0											
		1											
2	VP2	0											
		1											
3	VP3	0											
		1											
4	VP4	0											
		1											
5	VP5 (MSB)	0											
		1											
6	VSZ10	0			<table><tr><td>VSZ11 \ VSZ10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table>	VSZ11 \ VSZ10	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot
VSZ11 \ VSZ10	0	1											
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
		1											
7	VSZ11	0											
		1											
8	VSZ20	0	<table><tr><td>VSZ21 \ VSZ20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table>	VSZ21 \ VSZ20	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Second line vertical character size.
VSZ21 \ VSZ20	0	1											
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
		1											
9	VSZ21	0											
		1											
A	VSZ30	0	<table><tr><td>VSZ31 \ VSZ30</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table>	VSZ31 \ VSZ30	0	1	0	1H/1 dot	2H/1 dot	1	3H/1 dot	4H/1 dot	Lines 3 to 12 vertical character sizes.
VSZ31 \ VSZ30	0	1											
0	1H/1 dot	2H/1 dot											
1	3H/1 dot	4H/1 dot											
		1											
B	VSZ31	0											
		1											
C	—	0											
		1											

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).

(3) Address 190 (0 BE<sub>HEX</sub>)

DA 0 to C	Register Name	Contents				Notes																																				
		Setting	Function																																							
0	PHASE0	0	<table><tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>Background tint</th></tr><tr><td>0</td><td>0</td><td>0</td><td><math>\pi/2</math></td></tr><tr><td>0</td><td>0</td><td>1</td><td><math>\pi</math></td></tr><tr><td>0</td><td>1</td><td>0</td><td><math>3\pi/2</math></td></tr><tr><td>0</td><td>1</td><td>1</td><td>In-phase</td></tr><tr><td>1</td><td>0</td><td>0</td><td><math>\pi/4</math></td></tr><tr><td>1</td><td>0</td><td>1</td><td><math>3\pi/4</math></td></tr><tr><td>1</td><td>1</td><td>0</td><td><math>5\pi/4</math></td></tr><tr><td>1</td><td>1</td><td>1</td><td><math>7\pi/4</math></td></tr></table>				PHASE2	PHASE1	PHASE0	Background tint	0	0	0	$\pi/2$	0	0	1	$\pi$	0	1	0	$3\pi/2$	0	1	1	In-phase	1	0	0	$\pi/4$	1	0	1	$3\pi/4$	1	1	0	$5\pi/4$	1	1	1	$7\pi/4$
		PHASE2					PHASE1	PHASE0	Background tint																																	
0	0	0					$\pi/2$																																			
0	0	1					$\pi$																																			
0	1	0					$3\pi/2$																																			
0	1	1					In-phase																																			
1	0	0					$\pi/4$																																			
1	0	1					$3\pi/4$																																			
1	1	0					$5\pi/4$																																			
1	1	1					$7\pi/4$																																			
1																																										
1	PHASE1	0																																								
		1																																								
2	PHASE2	0																																								
		1																																								
3	—	0																																								
		1																																								
4	—	0																																								
		1																																								
5	SYSRST	0																																								
		1	All registers reset and display set to off																																							
6	—	0																																								
		1																																								
7	DSPON	0	Character display off																																							
		1	Character display on																																							
8	OSCSTP	0	Crystal oscillator circuit and LC oscillator circuit is not stopped																																							
		1	Crystal oscillator circuit and LC oscillator circuit is stopped																																							
9	$\overline{2fsc}$ /4fsc	0	Clock frequency 2 fsc																																							
		1	Clock frequency 4 fsc																																							
A	$\overline{LC}$ /XTAL	0	Using LC oscillation for pixel clock																																							
		1	Using crystal oscillation for pixel clock																																							
B	$\overline{INT}$ /NON	0	Interlaced (312.5 H/1 field)																																							
		1	Non-interlaced (313 H/1 field)																																							
C	—	0																																								
		1																																								

Note: \* When reset using the  $\overline{RST}$  pin, all registers are set to 0 (zero).

**(4) Address 191 (0BF<sub>HEX</sub>)**

DA 0 to C	Register Name	Contents			Notes									
		Setting	Function											
0	BCOL	0	With background tint (only enabled with internal synchronizing)											
		1	No background tint (background level setting only)											
1	CBOFF	0	Burst signal always output											
		1	When BCOL is set to "H", burst signal also does not output											
2	EX	0	External synchronizing		HSYNC and VSYNC signal changeover to external or internal supported.									
		1	Internal synchronizing											
3	BLINK0	0	<table><tr><td>BLINK0 BLINK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blinking off</td><td>25% duty</td></tr><tr><td>1</td><td>50% duty</td><td>75% duty</td></tr></table>		BLINK0 BLINK1	0	1	0	Blinking off	25% duty	1	50% duty	75% duty	Blinking duty comparative variability.
BLINK0 BLINK1	0	1												
0	Blinking off	25% duty												
1	50% duty	75% duty												
4	BLINK1	0												
		1												
5	BLINK2	0	Blinking cycle approximately 0.5 s		Variable blinking cycle.									
		1	Blinking cycle approximately 1 s											
6	—	0												
		1												
7	BLK0	0	<table><tr><td>BLK0 BLK1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking off</td><td>Character size</td></tr><tr><td>1</td><td>Trimming size</td><td>Total overall size</td></tr></table>		BLK0 BLK1	0	1	0	Blanking off	Character size	1	Trimming size	Total overall size	Variable blanking size.
		BLK0 BLK1			0	1								
0	Blanking off	Character size												
1	Trimming size	Total overall size												
8	BLK1	0												
		1												
9	—	0												
		1												
A	—	0												
		1												
B	TSTMOD	0	Normal operation mode		Fixes to zero (0) condition.									
		1	Test operation mode											
C	—	0												
		1												

Note: \* When reset using the  $\overline{\text{RST}}$  pin, all registers are set to 0 (zero).

DA 0 to 8	Register Name	Contents		Notes	
		Setting	Function		
0	ADR0	0	Character ROM address setting		
		1	When display control RAM is specified, DA7 equals “1” and ADR0 to ADR6 are set to “0”		
1	ADR1	0	Character ROM address setting range is 0 to 127 (7F <sub>HEX</sub> )		
		1			
2	ADR2	0			
		1			
3	ADR3	0			
		1			
4	ADR4	0			
		1			
5	ADR5	0			
		1			
6	ADR6	0			
		1			
7	ROM/ RAM	0			Character ROM is accessed and read directly
		1			Character ROM is accessed and read through display RAM

Line Address Table for Display Line ROM

Line	Address	Line	Address
1 line	00 <sub>HEX</sub> (0000)	33 line	300 <sub>HEX</sub> (0768)
2 line	18 <sub>HEX</sub> (0024)	34 line	318 <sub>HEX</sub> (0792)
3 line	30 <sub>HEX</sub> (0048)	35 line	330 <sub>HEX</sub> (0816)
4 line	48 <sub>HEX</sub> (0072)	36 line	348 <sub>HEX</sub> (0840)
5 line	60 <sub>HEX</sub> (0096)	37 line	360 <sub>HEX</sub> (0864)
6 line	78 <sub>HEX</sub> (0120)	38 line	378 <sub>HEX</sub> (0888)
7 line	90 <sub>HEX</sub> (0144)	39 line	390 <sub>HEX</sub> (0912)
8 line	A8 <sub>HEX</sub> (0168)	40 line	3A8 <sub>HEX</sub> (0936)
9 line	C0 <sub>HEX</sub> (0192)	41 line	3C0 <sub>HEX</sub> (0960)
10 line	D8 <sub>HEX</sub> (0216)	42 line	3D8 <sub>HEX</sub> (0984)
11 line	F0 <sub>HEX</sub> (0240)	43 line	3F0 <sub>HEX</sub> (1008)
12 line	108 <sub>HEX</sub> (0264)	44 line	408 <sub>HEX</sub> (1032)
13 line	120 <sub>HEX</sub> (0288)	45 line	420 <sub>HEX</sub> (1056)
14 line	138 <sub>HEX</sub> (0312)	46 line	438 <sub>HEX</sub> (1080)
15 line	150 <sub>HEX</sub> (0336)	47 line	450 <sub>HEX</sub> (1104)
16 line	168 <sub>HEX</sub> (0360)	48 line	468 <sub>HEX</sub> (1128)
17 line	180 <sub>HEX</sub> (0384)	49 line	480 <sub>HEX</sub> (1152)
18 line	198 <sub>HEX</sub> (0408)	50 line	498 <sub>HEX</sub> (1176)
19 line	1B0 <sub>HEX</sub> (0432)	51 line	4B0 <sub>HEX</sub> (1200)
20 line	1C8 <sub>HEX</sub> (0456)	52 line	4C8 <sub>HEX</sub> (1224)
21 line	1E0 <sub>HEX</sub> (0480)	53 line	4E0 <sub>HEX</sub> (1248)
22 line	1F8 <sub>HEX</sub> (0504)	54 line	4F8 <sub>HEX</sub> (1272)
23 line	210 <sub>HEX</sub> (0528)	55 line	510 <sub>HEX</sub> (1296)
24 line	228 <sub>HEX</sub> (0552)	56 line	528 <sub>HEX</sub> (1320)
25 line	240 <sub>HEX</sub> (0576)	57 line	540 <sub>HEX</sub> (1344)
26 line	258 <sub>HEX</sub> (0600)	58 line	558 <sub>HEX</sub> (1368)
27 line	270 <sub>HEX</sub> (0624)	59 line	570 <sub>HEX</sub> (1392)
28 line	288 <sub>HEX</sub> (0648)	60 line	588 <sub>HEX</sub> (1416)
29 line	2A0 <sub>HEX</sub> (0672)	61 line	5A0 <sub>HEX</sub> (1440)
30 line	2B8 <sub>HEX</sub> (0696)	62 line	5B8 <sub>HEX</sub> (1464)
31 line	2D0 <sub>HEX</sub> (0720)	63 line	5D0 <sub>HEX</sub> (1488)
32 line	2E8 <sub>HEX</sub> (0744)	64 line	5E8 <sub>HEX</sub> (1512)

## Screen Construction (Sample Display)

Setting of 12-line display using display line ROM (64 lines).

Within line ROM, setting of extended characters is made available through display control RAM.

Display control RAM addresses are automatically allocated to display array from 0 to 175 (AF<sub>HEX</sub>).

 (thick line) indicates character setting using display control RAM.

 (thin line) indicates character setting using line ROM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 0Fh	RAM 000 10h	RAM 001 11h	RAM 002 12h	RAM 003 13h	RAM 004 14h	RAM 005 15h	ROM 022 16h	ROM 023 17h
2	ROM 024 18h	RAM 006 18h	RAM 007 19h	RAM 008 1Ah	RAM 009 1Bh	ROM 029 1Ch	ROM 030 1Dh	ROM 031 1Eh	ROM 032 1Fh	ROM 033 20h	ROM 034 21h	RAM 016 22h	RAM 017 23h	RAM 018 24h	RAM 019 25h	RAM 020 26h	RAM 021 27h	RAM 022 28h	RAM 023 29h	RAM 024 2Ah	RAM 025 2Bh	RAM 026 2Ch	RAM 027 2Dh	ROM 046 2Eh
3	ROM 048 18h	ROM 049 19h	ROM 050 1Ah	ROM 051 1Bh	ROM 052 1Ch	ROM 053 1Dh	ROM 054 1Eh	ROM 055 1Fh	ROM 056 20h	ROM 057 21h	ROM 058 22h	ROM 059 23h	ROM 060 24h	ROM 061 25h	ROM 062 26h	ROM 063 27h	RAM 028 28h	RAM 029 29h	RAM 030 2Ah	RAM 031 2Bh	RAM 032 2Ch	RAM 033 2Dh	RAM 034 2Eh	ROM 070 2Fh
4	ROM 072 48h	ROM 073 49h	ROM 074 4Ah	ROM 075 4Bh	ROM 076 4Ch	ROM 077 4Dh	ROM 078 4Eh	ROM 079 4Fh	ROM 080 50h	ROM 081 51h	ROM 082 52h	ROM 083 53h	ROM 084 54h	ROM 085 55h	ROM 086 56h	ROM 087 57h	RAM 035 58h	RAM 036 59h	RAM 037 5Ah	RAM 038 5Bh	RAM 039 5Ch	RAM 040 5Dh	RAM 041 5Eh	ROM 085 5Fh
5	ROM 088 60h	ROM 089 61h	ROM 090 62h	ROM 091 63h	ROM 092 64h	ROM 093 65h	ROM 094 66h	ROM 095 67h	ROM 096 68h	ROM 097 69h	ROM 098 6Ah	ROM 099 6Bh	ROM 100 6Ch	ROM 101 6Dh	ROM 102 6Eh	ROM 103 6Fh	RAM 042 70h	RAM 043 71h	RAM 044 72h	RAM 045 73h	RAM 046 74h	RAM 047 75h	RAM 048 76h	ROM 119 77h
6	ROM 120 78h	ROM 121 79h	ROM 122 7Ah	ROM 123 7Bh	ROM 124 7Ch	ROM 125 7Dh	ROM 126 7Eh	ROM 127 7Fh	ROM 128 80h	ROM 129 81h	ROM 130 82h	ROM 131 83h	ROM 132 84h	ROM 133 85h	ROM 134 86h	ROM 135 87h	RAM 049 88h	RAM 050 89h	RAM 051 8Ah	RAM 052 8Bh	RAM 053 8Ch	RAM 054 8Dh	RAM 055 8Eh	ROM 143 8Fh
7	RAM 073 48h	RAM 074 49h	RAM 075 4Ah	RAM 076 4Bh	RAM 077 4Ch	RAM 078 4Dh	RAM 079 4Eh	RAM 080 4Fh	RAM 081 50h	RAM 082 51h	RAM 083 52h	RAM 084 53h	RAM 085 54h	RAM 086 55h	RAM 087 56h	RAM 088 57h	RAM 089 58h	RAM 090 59h	RAM 091 5Ah	RAM 092 5Bh	RAM 093 5Ch	RAM 094 5Dh	RAM 095 5Eh	ROM 167 5Fh
8	RAM 085 58h	RAM 086 59h	RAM 087 5Ah	RAM 088 5Bh	RAM 089 5Ch	RAM 090 5Dh	RAM 091 5Eh	RAM 092 5Fh	RAM 093 60h	RAM 094 61h	RAM 095 62h	RAM 096 63h	RAM 097 64h	RAM 098 65h	RAM 099 66h	RAM 100 67h	RAM 101 68h	RAM 102 69h	RAM 103 6Ah	RAM 104 6Bh	RAM 105 6Ch	RAM 106 6Dh	RAM 107 6Eh	ROM 181 6Fh
9	ROM 182 C0h	ROM 183 C1h	ROM 184 C2h	ROM 185 C3h	ROM 186 C4h	ROM 187 C5h	ROM 188 C6h	ROM 189 C7h	ROM 190 C8h	ROM 191 C9h	ROM 192 CAh	ROM 193 CBh	ROM 194 CCh	ROM 195 CDh	ROM 196 CEh	ROM 197 CFh	RAM 108 D0h	RAM 109 D1h	RAM 110 D2h	RAM 111 D3h	RAM 112 D4h	RAM 113 D5h	RAM 114 D6h	ROM 239 DFh
10	ROM 216 D8h	ROM 217 D9h	ROM 218 DAh	ROM 219 DBh	ROM 220 DCh	ROM 221 DDh	ROM 222 DEh	ROM 223 DFh	ROM 224 E0h	ROM 225 E1h	ROM 226 E2h	ROM 227 E3h	ROM 228 E4h	ROM 229 E5h	ROM 230 E6h	ROM 231 E7h	RAM 115 E8h	RAM 116 E9h	RAM 117 EAh	RAM 118 EBh	RAM 119 ECh	RAM 120 EDh	RAM 121 EEh	ROM 239 EFh
11	ROM 240 F0h	ROM 241 F1h	ROM 242 F2h	ROM 243 F3h	ROM 244 F4h	ROM 245 F5h	ROM 246 F6h	ROM 247 F7h	ROM 248 F8h	ROM 249 F9h	ROM 250 FAh	ROM 251 FBh	ROM 252 FCh	ROM 253 FDh	ROM 254 FEh	ROM 255 FFh	RAM 122 00h	RAM 123 01h	RAM 124 02h	RAM 125 03h	RAM 126 04h	RAM 127 05h	RAM 128 06h	ROM 263 07h
12	RAM 129 08h	RAM 130 09h	RAM 131 0Ah	RAM 132 0Bh	RAM 133 0Ch	RAM 134 0Dh	RAM 135 0Eh	RAM 136 0Fh	RAM 137 10h	RAM 138 11h	RAM 139 12h	RAM 140 13h	RAM 141 14h	RAM 142 15h	RAM 143 16h	RAM 144 17h	RAM 145 18h	RAM 146 19h	RAM 147 1Ah	RAM 148 1Bh	RAM 149 1Ch	RAM 150 1Dh	RAM 151 1Eh	ROM 287 1Fh

## Input Timing of External Control Data

Input format is set at 16-bit, serial input for address and data input.

### Address and Data Serial Input

#### ① Address Input with 16-bit Construction

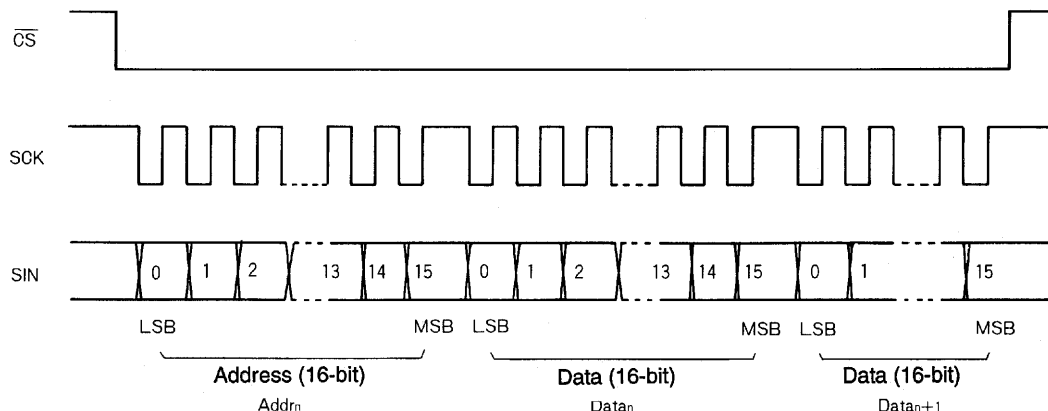
Lower 8 bits are reserved for address assignments while the upper 8 bits are fixed to "0".

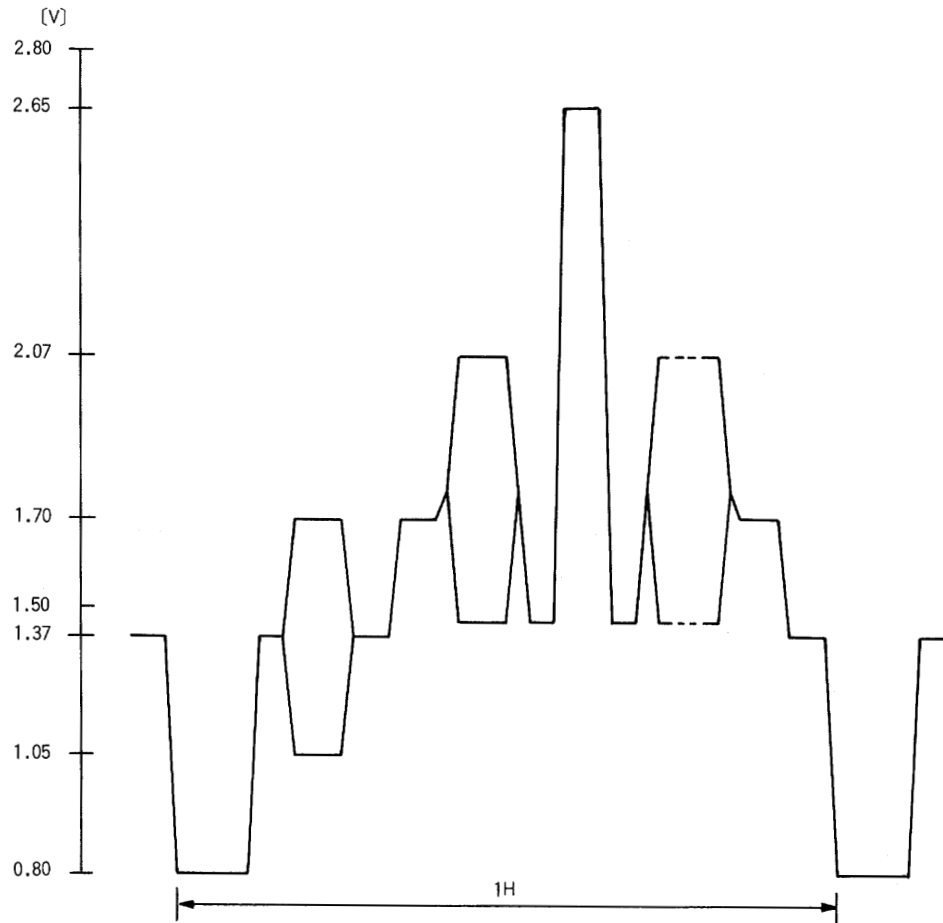
#### ② Data Input with 16-bit Construction

- Lower 8 bits having addresses 000<sub>HEX</sub> through 0AF<sub>HEX</sub> are reserved for data assignments while the upper 8 bits are fixed to "0".
- Lower 11 bits having addresses 0B0<sub>HEX</sub> through 0BB<sub>HEX</sub> are reserved for data assignments while the upper 5 bits are fixed to "0".
- Lower 12 bits having addresses 0BC<sub>HEX</sub> through 0BF<sub>HEX</sub> are reserved for data assignments while the upper 4 bits are fixed to "0".

#### ③ Data Input Format

After the onset of CS, the first 16 bits are processed as address information, and thereafter information is processed as data in 16-bit units. Addresses are automatically allocated in 16-bit increments.



**Composite Video Signal Output Level (Internal generation level: synchronization chip level = 0.8 V)**


Output Level	Output Voltage ( $V_{DC}$ )
Character level	2.650
Background color "H" level	2.075
Burst "L" level	1.700
Background color "L" level	1.500
Trimming level	1.500
Pedestal level	1.375
Burst "L" level	1.050
Synchronization chip level	0.800

 $V_{DD2} = 5.000V_{DC}$

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