CMOS IC

LC7455A/M

U.S. Closed Caption Signal Extraction IC

Overview

The LC7455A/M receives the composite video signal from V/C (Video Chroma) signal processor and extracts the closed caption data with several signals from the decoder IC or microcomputer, are then sent to the decoder IC.

Features

(1) Low power consumption due to CMOS process
(2) Accurate caption signal extraction using a built-in peak hold circuit and digital technology.
(3) Power Requirement : 5V± 10%
(4) Package LC7455A : DIP16
LC7455M : MFP18

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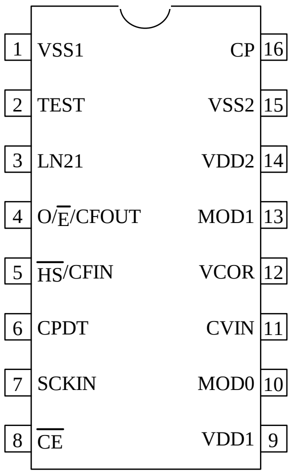
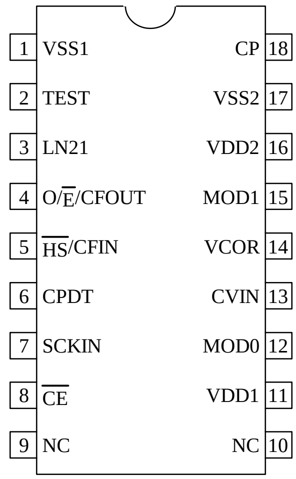
Pin Assignment

DIP16



LC7455A

MFP18

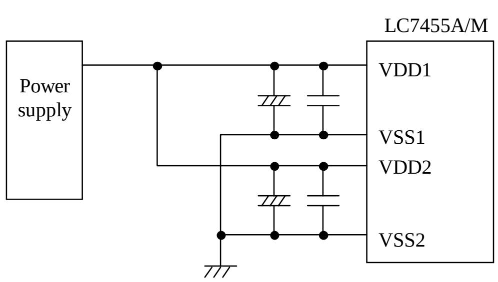


LC7455M

Pin Description

Terminal	Pin No		Function Description		
	DIP16	MFP18	MODE1	MODE2	MODE3
VSS1	1	1	Negative power supply for digital circuit		
TEST	2	2	Test pin, Leave open in operation		
LN21	3	3	Line 21H pulse output (Even field)		Line 21H pulse output (Both field)
O/$\overline{\text{E}}$ /CFOUT	4	4	Field determination output	CF oscillation output terminal	Field determination output
$\overline{\text{HS}}$ /CFIN	5	5	$\overline{\text{Hsync}}$ output	CF oscillation input terminal	$\overline{\text{Hsync}}$ input
CPDT	6	6	Caption data output (Nch open drain)		
SCKIN	7	7	Input for Caption-data-transmission clock		
$\overline{\text{CE}}$	8	8	Chip select input		
VDD1	9	11	Positive power supply for digital circuit		
MOD0	10	12	leave open	connect to VDD1	leave open
CVIN	11	13	Composite video input		
VCOR	12	14	Built-in VCO frequency control		
MOD1	13	15	leave open	leave open	connect to VDD1
VDD2	14	16	Positive power supply for analog circuit		
VSS2	15	17	Negative power supply for analog circuit		
CP	16	18	Built-in PLL filter pin		

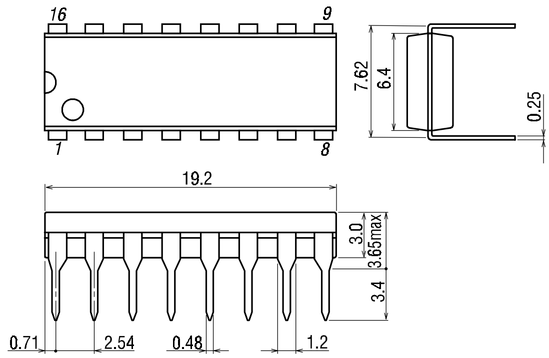
* VDD1,VSS1are the power supply terminals for built-in digital circuit. And VDD2,VSS2 are the power supply terminals for built-in analog circuit. Connect like following figure to reduce the noise influence.



Package Dimension

(unit : mm)

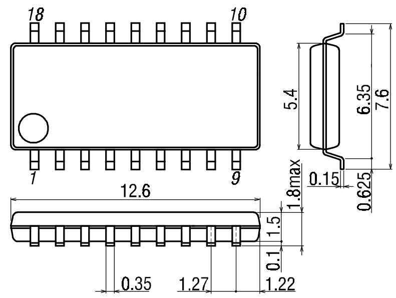
3006B



SANYO : DIP-16

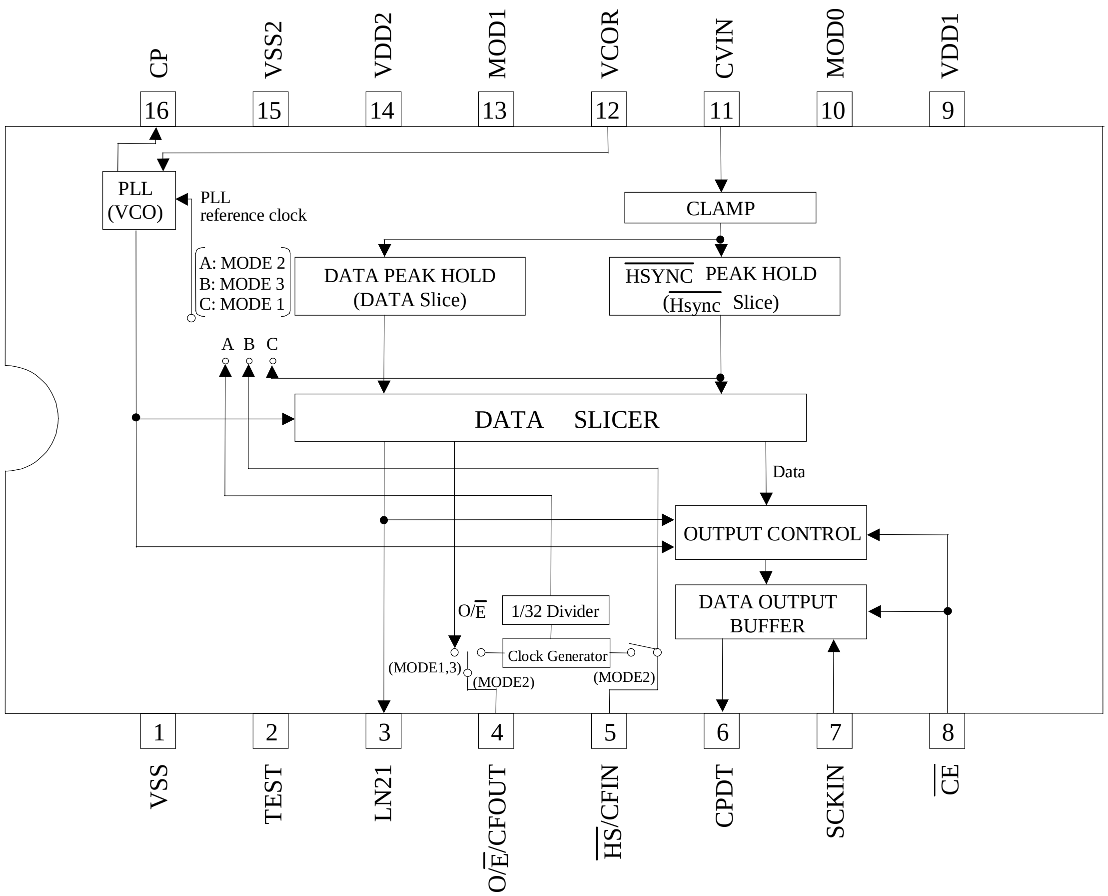
(unit : mm)

3095



SANYO : MFP-18

System Block Diagram (DIP16)



Mode Description

Terminal		MODE	Applications	Operation
MOD1	MOD0			
Leave open	Leave open	MOD1	VTR	•Extraction of Line-21 data of the even field Built-in PLL circuit uses the horizontal synchronized signal separated from C-Video signal as the reference of PLL operation.
Leave open	Connect to VDD1	MOD2	VTR	•Extraction of Line-21 data of the even field Built-in PLL circuit uses the 1/32-divided signal from 508KHz oscilla- tion as the reference of the PLL operation. Note that the 508KHz oscillation requires 508KHz-ceramic resonator externally.
Connect to VDD1	Leave open	MOD3	NTSC-TV	•Extraction of Line-21 data of the even/Odd field Built-in PLL circuit uses the horizontal synchronized signal generated from external Fly-Back circuit as the reference of the PLL operation.

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min.	typ.	max.	
Supply voltage	VDDMAX	VDD1,VDD2	VDD1=VDD2	-0.3	-	+7.0	V
Input voltage	VI	$\overline{HS}$ /CFIN,CVIN,SCKIN, $\overline{CE}$		-0.3	-	VDD+0.3	
Output voltage	VIO	LN21,CPDT, O/ $\overline{E}$ /CFOUT, $\overline{HS}$ /CFIN		-0.3	-	VDD+0.3	
Maximum power dissipation	Pdmax	DIP16				300	mW
		MFP18				150	
Operating temperature range	Topr			-30	-	+70	°C
Storage temperature range	Tstg			-55	-	+150	

* VSS1 and VSS2 are same level.
VDD1 and VDD2 are also same level.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating Supply voltage	VDD	VDD1,VDD2	VDD1=VDD2		4.5		5.5	V
Input high voltage	VIH	$\overline{HS}$ /CFIN, SCKIN, $\overline{CE}$	Output disable	4.5 to 5.5	0.75VDD		VDD	
Input low voltage	VIL	$\overline{HS}$ /CFIN, SCKIN, $\overline{CE}$	Output disable	4.5 to 5.5	VSS		0.2VDD	
CVIN input amplitude	CVSYNC	CVIN	SYNC-WHITE=1.0V	4.5 to 5.5	1Vp-p+ 3dB	1V p-p	1V p-p+3dB	
$\overline{HS}$ input frequency range	fH	$\overline{HS}$ /CFIN	MODE3	4.5 to 5.5	15.23	15.73	16.23	kHz
Oscillation frequency range (Note 1)	FmCF	$\overline{HS}$ /CFIN, O/ $\overline{E}$ /CFOUT	•MODE2 •Refer to figure 1	4.5 to 5.5	503	508	513	
Oscillation stabilizing time period (Note 2)	tmsCF	$\overline{HS}$ /CFIN, O/ $\overline{E}$ /CFOUT	•MODE2 •Refer to figure 2	4.5 to 5.5		0.5	5	ms

(Note 1) The oscillation constant is shown on table 1.
(Note 2) The oscillation stable time period means the time to oscillate stably after supplyng voltage.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Input high current	IIH	$\overline{HS}$/CFIN, SCKIN, $\overline{CE}$	VIN=VDD	4.5 to 5.5			1	µA
Input low current	IIL	$\overline{HS}$/CFIN, SCKIN, $\overline{CE}$	VIN=VSS	4.5 to 5.5	-1			
Output high voltage	VOH	LN21,CPDT, O/$\overline{E}$/CFOUT, $\overline{HS}$/CFIN	IOH=-4mA	4.5 to 5.5	VDD-1.2			V
Output low voltage	VOL	LN21,CPDT, O/$\overline{E}$/CFIN, $\overline{HS}$/CFIN	IOL=10mA	4.5 to 5.5			1	
Input clamp voltage	VCLMP	CVIN		5.0	2.3	2.5	2.7	
Clamp input current	CII	CVIN	CVIN=3V	5.0	5	10	18	µA
Clamp output current	COI	CVIN	CVIN=2V	5.0	-120	-70	-30	
Current dissipation	IDD	VDD1,VDD2		4.5 to 5.5		6	15.0	mA

4. Serial Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions		Ratings			unit
						VDD[V]	min.	typ.	max.	
Serial clock	Input clock	Cycle	tCKCY	SCKIN	Refer to figure 3	4.5 to 5.5	1			µs
		Low Level pulse width	tCKL			4.5 to 5.5	0.5			
		High Level pulse width	tCKH			4.5 to 5.5	0.5			
	Set-up time		tICK			4.5 to 5.5	1			
Serial output	Output delay time		tCKO	CPDT	•Use test load. •Refer to figure 3	4.5 to 5.5			0.5	

Table 1. Ceramic resonator oscillation recommended constant

A kind of an oscillation	Producer	Oscillator	C1	C2
508KHz ceramic resonator oscillation	Murata	CSB 508E	150pF	150pF

* Both C1 and C2 must be use K rank (±10%) and SL characteristics.

(Notes)
- Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
- If you use other oscillators herein, we provide no guarantee for the characteristics.

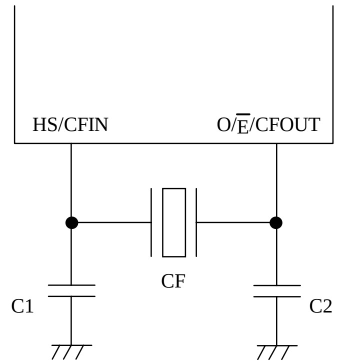


Figure 1 Ceramic resonator oscillation

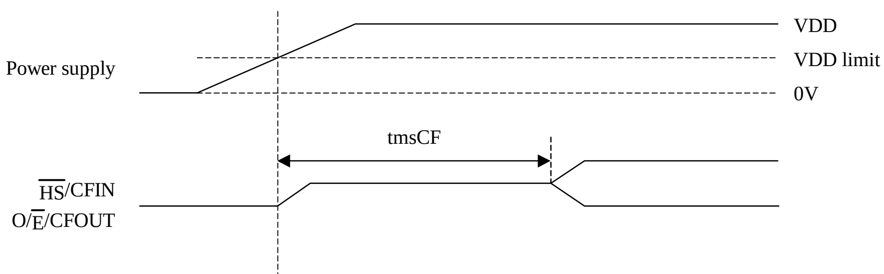
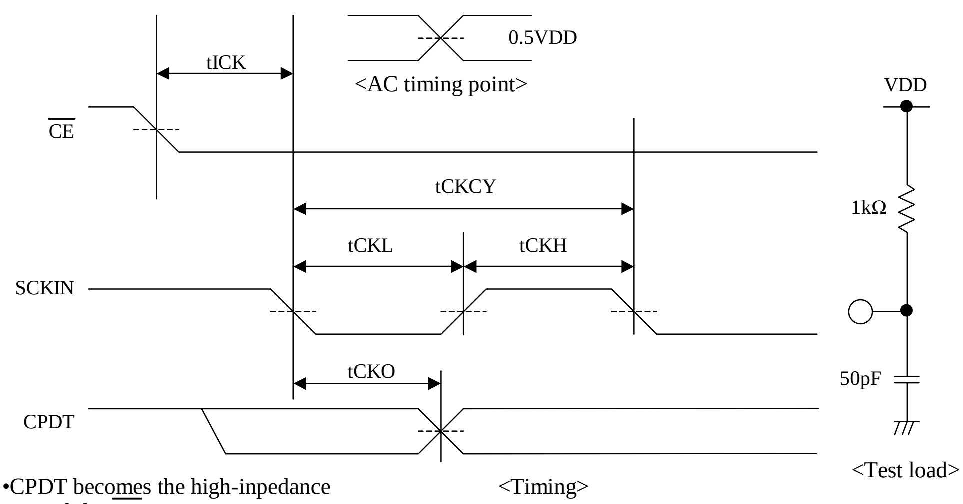


Figure 2 Oscillation stable time period

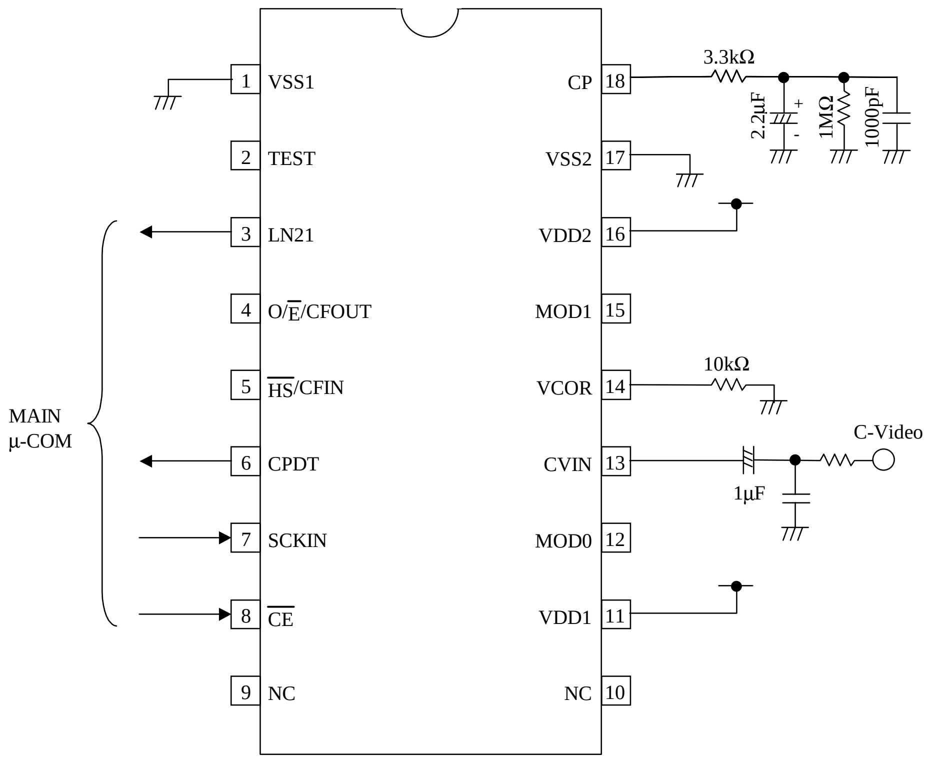


•CPDT becomes the high-inpedance state while $\overline{\text{CE}}$=H

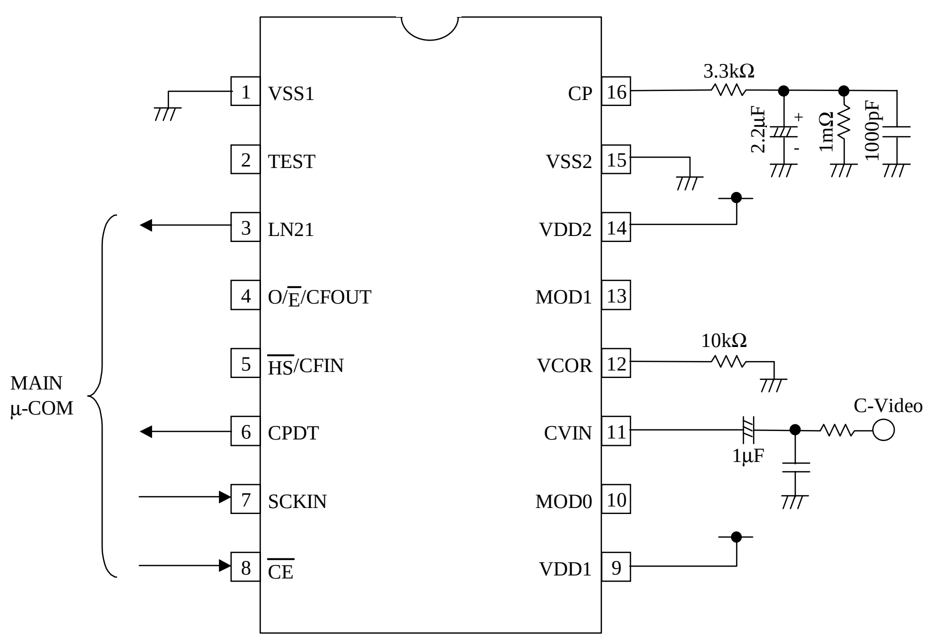
Figure 3 Serial output test condition

Applications (Mode 1)

MFP18

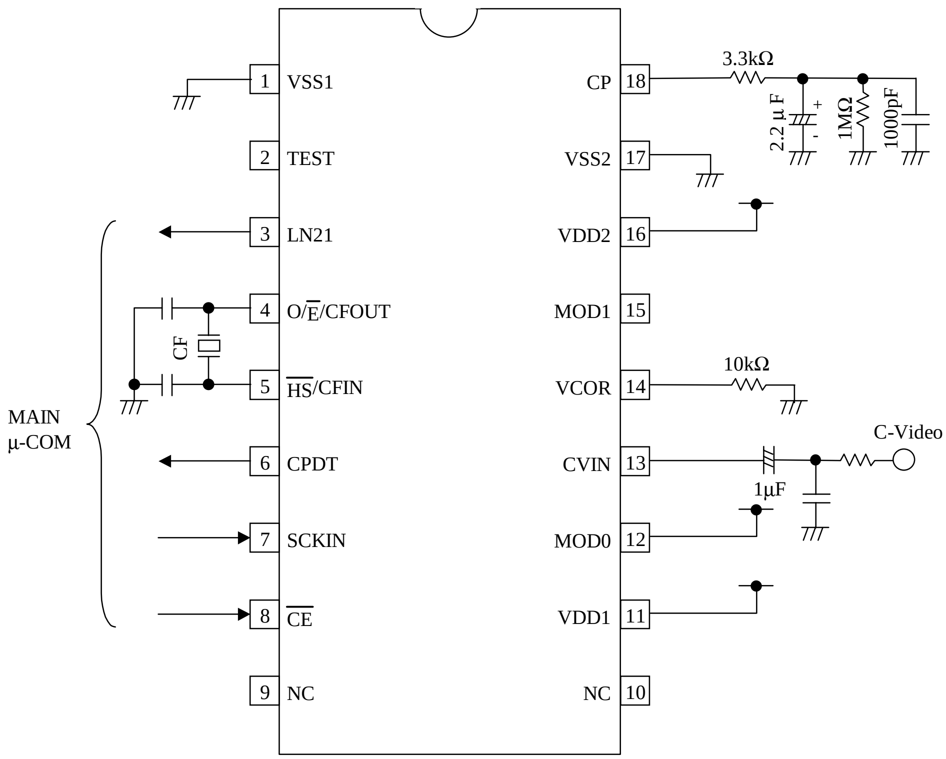


DIP16

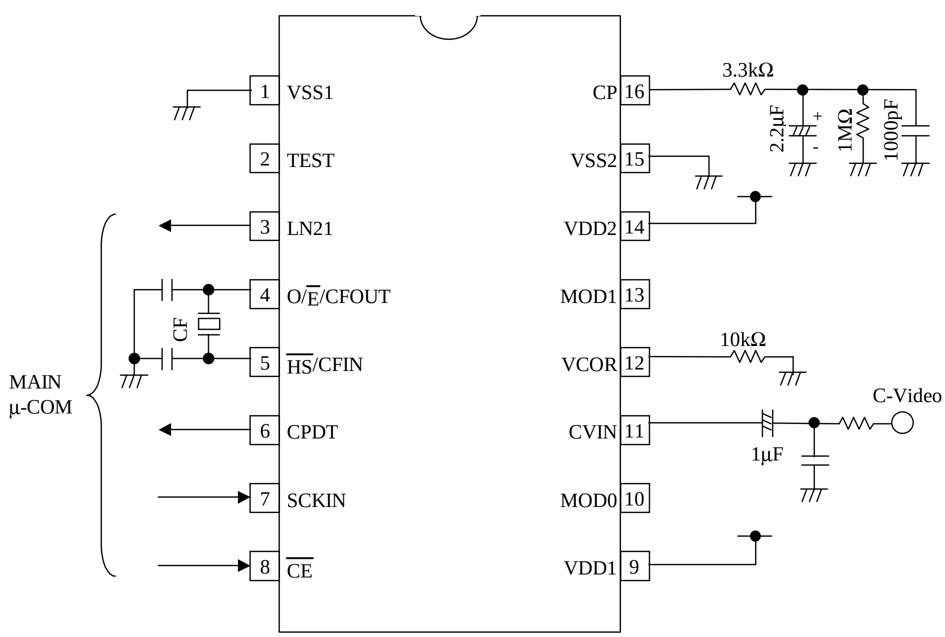


Applications (Mode 2)

MFP18

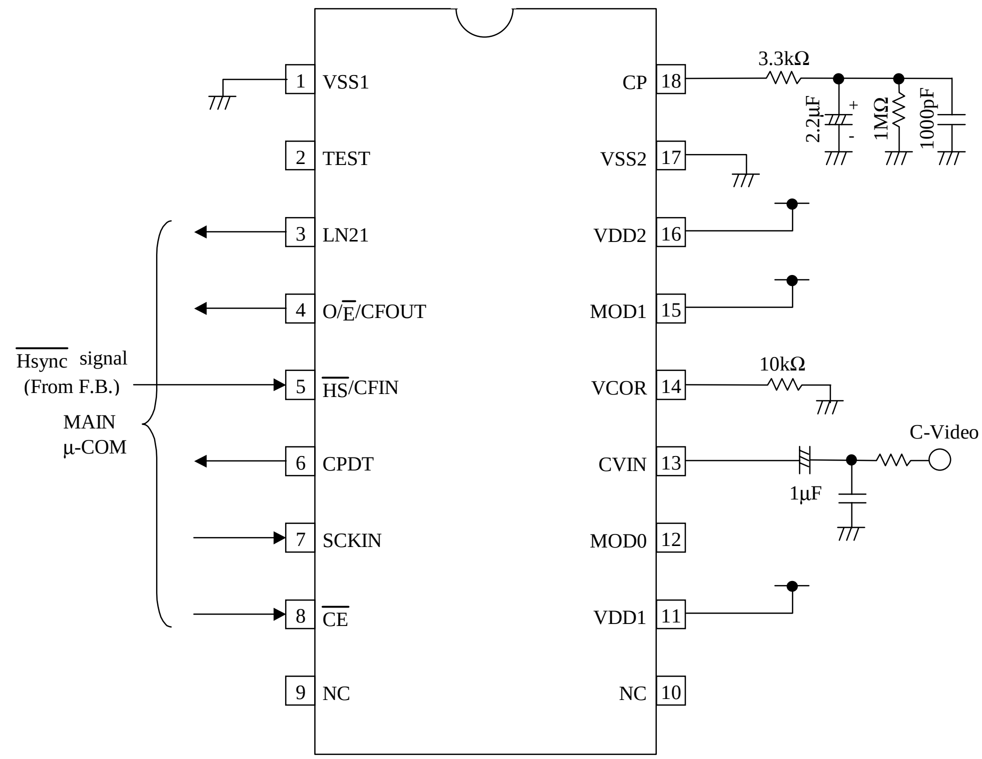


DIP16

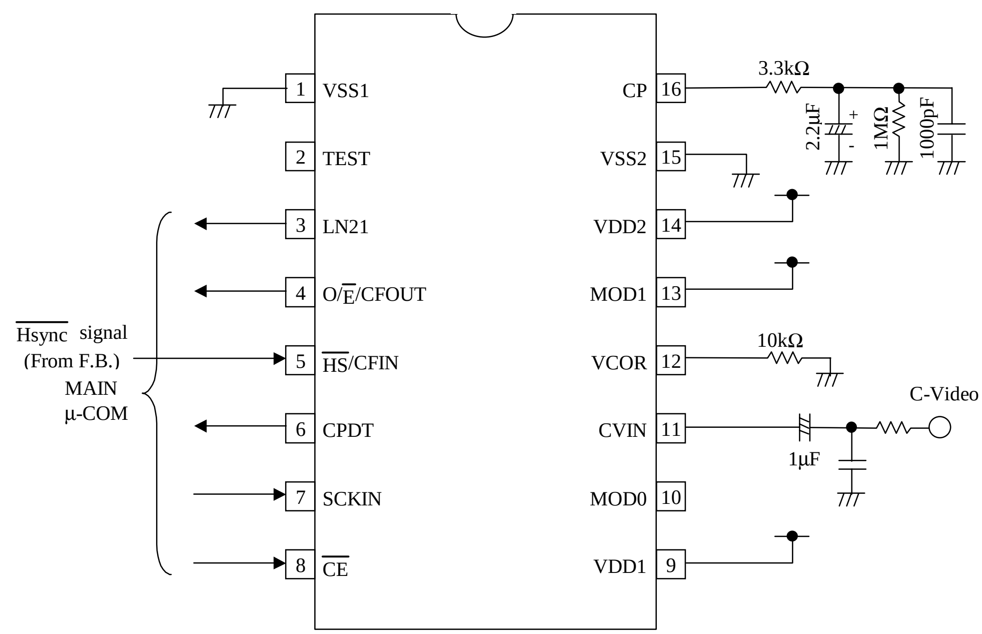


Applications (Mode 3)

MFP18



DIP16



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