Ordering number : ENN*6853

CMOS IC

LC73101C

LCD Driver IC

Preliminary

Overview

The LC73101C is a dot matrix LCD driver IC that includes an on-chip display data RAM with a one-to-one correspondence between bits in RAM and display pixels on the LCD panel. The LC73101C provides display data RAM that can store 80 × 132 bits of data and can implement a large-screen display system with a single chip.

The LC73101C provides 80 common output circuits and 132 segment output circuits, and can display up to 80 × 132 dots (8 characters × 4 lines of kanji text using a 16 × 16-dot kanji font) with a single chip. The LC73101C also provides a master/slave function that allows two LC73101C chips to be combined to implement twice the display area: 160 × 132 dots.

The LC73101C provides a partial display function that allows the number of lines displayed to be set to 8, 16, 24, 32, 40, 48, 56, 64, 72, or 80 lines by commands sent from the system microcontroller. This allows the current drain to be reduced significantly when only a smaller number of lines needs to be displayed.

This device includes built-in voltage step-up circuits with factors of 3×, 4×, 5×, and 6× to provide high-quality display even when a high duty cycle is required. The number of step-up circuit stages used can be set by commands from the system microcontroller.

Since the display RAM read and write operations do not require the external operating clock, the LC73101C can operate at low power. Furthermore, since the LC73101C provides built-in LCD drive power supply, LCD drive power supply voltage adjustment, temperature-compensated reference voltage, and display contrast adjustment electronic potentiometers circuits, the LC73101C can implement portable display systems with low power consumption and a minimal number of external components.

Features

- 132 × 80-dot display
- Microcontroller interface (for both Intel and Motorola microcontrollers)
- On-chip display RAM (80 × 132 = 10,560 bits)
- Low power
- Low-voltage operation: V_{DD} = 1.8 to 3.6 V
- High-precision reference voltage circuit (Variable temperature compensation coefficients)
- LCD drive 6× voltage step-up circuit (3×, 4×, 5×, or 6× can be selected by commands from the microcontroller.)
- Built-in high-precision RC oscillator circuit
- Contrast adjustment electronic potentiometer circuit
- Partial display function (Allows 8, 16, 24, 32, 40, 48, 56, 64, 72, or 80 lines to be displayed under the control of commands sent from the microcontroller.)
- Supports synchronous operation using master/slave connection.

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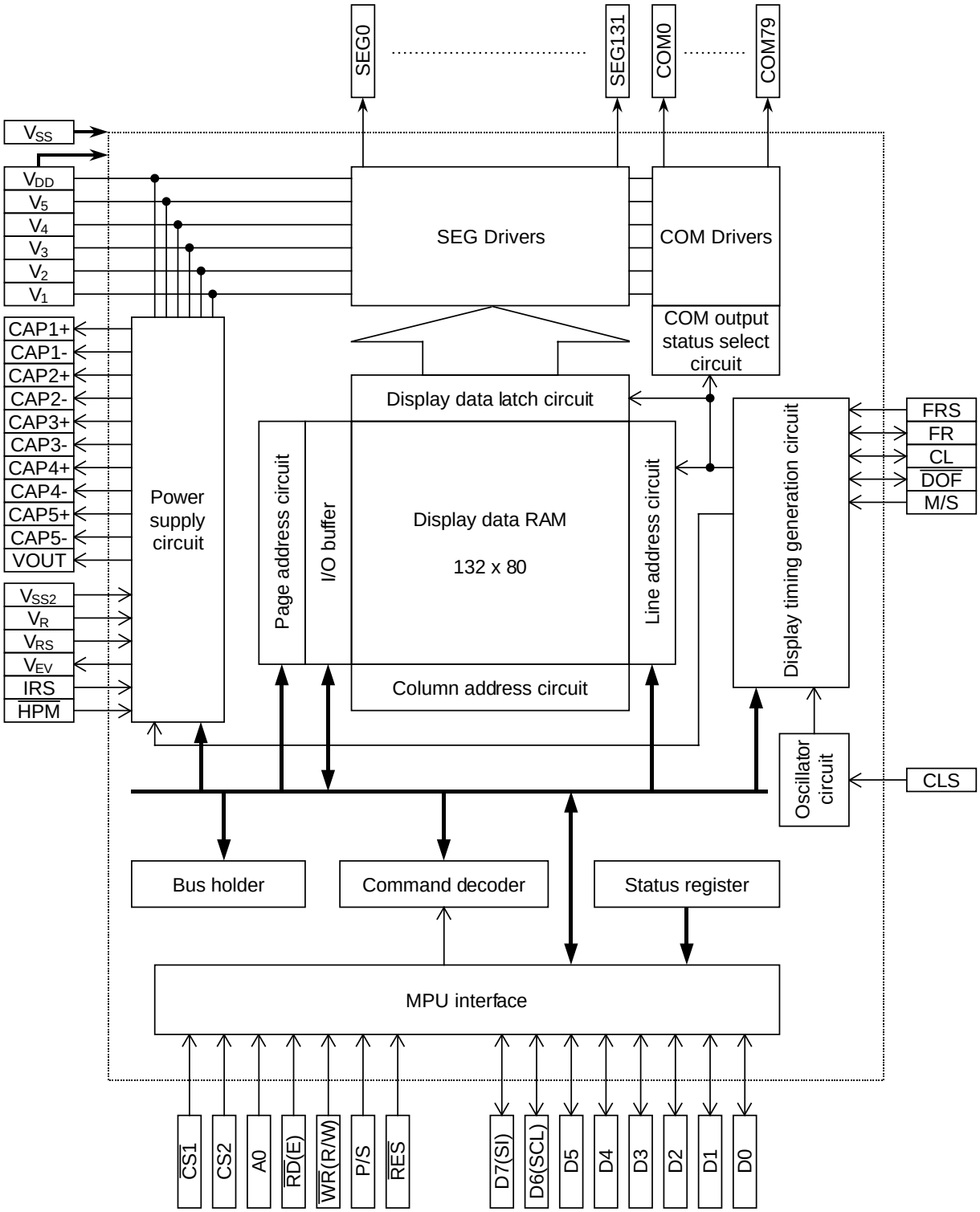
Block Diagram



Pin Functions

Power supply

Pin	I/O	Function	Number of pins
V_{DD}	Power supply	Microcontroller power supply. The same power supply system must be used for V_{CC}.	Undetermined
V_{SS}	Power supply	Connect to the system ground. These pins are 0 V pins.	Undetermined
V_{SS2}	Power supply	LCD drive step-up voltage circuit reference voltage	Undetermined
V_{RS}	Power supply	LCD power supply voltage adjustment circuit external input V_{REG} power supply. When the internally generated V_{REG} is used, this pin outputs that V_{REG} voltage.	Undetermined
V_1, V_2, V_3, V_4, V_5	Power supply	Multi-level power supply system used as the LCD power supply. The voltages stipulated for each LCD cell are created by resistor divider circuits or by operational amplifier based impedance conversion. The potentials are determined referenced to V_{SS}, and must obey the following inequalities. $V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{SS}$ When the built-in power supply circuit that operates in master mode is turned on, the voltage determined by the voltage adjustment circuit is applied to V_1, and the voltages determined by LCD Bias Set commands are applied to V_2 through V_5.	Undetermined

LCD Power Supply Circuit Pins

Pin	I/O	Function	Number of pins
CAP1+	O	Step-up circuit capacitor positive connection Insert a capacitor between this pin and the CAP1– pin.	Undetermined
CAP1–	O	Step-up circuit capacitor negative connection Insert a capacitor between this pin and the CAP1+ pin.	Undetermined
CAP2+	O	Step-up circuit capacitor positive connection Insert a capacitor between this pin and the CAP2– pin.	Undetermined
CAP2–	O	Step-up circuit capacitor negative connection Insert a capacitor between this pin and the CAP2+ pin.	Undetermined
CAP3+	O	Step-up circuit capacitor positive connection Insert a capacitor between this pin and the CAP3– pin.	Undetermined
CAP3–	O	Step-up circuit capacitor negative connection Insert a capacitor between this pin and the CAP3+ pin.	Undetermined
CAP4+	O	Step-up circuit capacitor positive connection Insert a capacitor between this pin and the CAP4– pin.	Undetermined
CAP4–	O	Step-up circuit capacitor negative connection Insert a capacitor between this pin and the CAP4+ pin.	Undetermined
CAP5+	O	Step-up circuit capacitor positive connection Insert a capacitor between this pin and the CAP5– pin.	Undetermined
CAP5–	O	Step-up circuit capacitor negative connection Insert a capacitor between this pin and the CAP5+ pin.	Undetermined
V_{OUT}	O	Post-step-up circuit voltage output. Insert a capacitor between this pin and V_{SS}.	Undetermined
V_R	I	Voltage adjustment. Apply a voltage in the range V_1 to V_{SS} by using a resistor divider circuit. Use of this pin is only valid when the built-in V_1 voltage adjustment resistor is not used (IRS = low). Do not use this pin if the built-in V_1 voltage adjustment resistor is used (IRS = high).	Undetermined

System Bus Connection Pins

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>D0 to D7</td><td>I/O</td><td>Bidirectional 8-bit data bus connected to the microcontroller data bus.
When the serial interface is selected (P/S is low):
D7: Serial data input (SI)
D6: Serial clock input (SCL)
In this mode, D0 to D5 go to the high-impedance state. When the chip select line is inactive, D0 to D7 go to the high-impedance state.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>A0 is normally connected to the low order bit of the microcontroller address bus and discriminates between data and commands.
A0 = high: Indicates that D0 to D7 are used for data display.
A0 = low: Indicates that D0 to D7 are used for control data.</td><td>1</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>The LC73101C is initialized when $\overline{\text{RES}}$ is set low.
The reset operation is performed by the $\overline{\text{RES}}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{\text{CS1}}$
CS2</td><td>I</td><td>Chip select signals. The LC73101C becomes active when $\overline{\text{CS1}}$ is low and CS2 is high. Input and output of data and commands is possible in this state.</td><td>2</td></tr>
<tr><td>$\overline{\text{RD}}$
(E)</td><td>I</td><td>This pin is active-low when an Intel-type microcontroller is used.
The Intel-type microcontroller $\overline{\text{RD}}$ signal should be connected to this pin. The LC73101C data bus goes to the output state when this signal is low.
This pin is active-high when a Motorola-type microcontroller is used.
This pin functions as the enable clock input pin when a Motorola-type microcontroller is used.</td><td>1</td></tr>
<tr><td>$\overline{\text{WR}}$
(R/$\overline{\text{W}}$)</td><td>I</td><td>This pin is active-low when an Intel-type microcontroller is used.
The Intel-type microcontroller $\overline{\text{WR}}$ signal should be connected to this pin. The data bus signals are latched on the rising edge of the WR signal.
When a Motorola-type microcontroller is used:
This pin functions as the read/write control signal input.
R/$\overline{\text{W}}$ = high: Read, R/$\overline{\text{W}}$ = low: Write.</td><td></td></tr>
<tr><td>C86</td><td>I</td><td>C86 is the Microcontroller interface switching input.
C86 = high: Motorola-type interface
C86 = low: Intel-type interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/serial data input mode switch
P/S = high: Parallel input
P/S = low: Serial input
The table below lists the effects of this pin.
<table>
<tr><th>P/S</th><th>Data/command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>$\overline{\text{RD}}$, $\overline{\text{WR}}$</td><td>—</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S is low, D0 to D5 go to the high-impedance state.
D0 to D5 may be left high, low, or open in this mode.
RD (E) and WR (R/W) must be held either high or low.
In serial data input mode, the RAM display data and the device status cannot be read.</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Selects enabled/disabled for the internal oscillator circuit for display clock
CLS = high: Internal oscillator circuit enabled.
CLS = low: Internal oscillator circuit disabled. (External input)
If CLS is low, input the display clock signal to the CL pin.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Selects master or slave mode operation for the LC73101C itself.
In slave mode operation, synchronization with the display system is acquired by input of the timing signals required for LCD display.
M/S = high: Master operation
M/S = low: Slave operation
The M/S and CLS pins determine the operating state as shown in the table below.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>$\overline{\text{DOF}}$</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
<tr><td>“L”</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td><td>1</td></tr>
</table>

Continued from preceding page.

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input or output.
The M/S and CLS pins determine the operating state as shown in the table below.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Input</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table>
When two LC73101C chips are used together in master/slave mode, their CL pins must be connected together.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD alternation signal input or output.
M/S = high: Output
M/S = Low: Input
When two LC73101C chips are used together in master/slave mode, their FR pins must be connected together.</td><td>1</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>Indicates the on/off state of the LCD display.
M/S = high: Output
M/S = Low: Input
When two LC73101C chips are used together in master/slave mode, their $\overline{\text{DOF}}$ pins must be connected together.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>V1 voltage adjustment resistor selection.
IRS = high: Internal resistor used.
IRS = low: Internal resistor not used. In this case, the V_1 voltage is adjusted by the VR pin and the external divider resistor circuit.
This pin is only valid in master mode. This pin must be held either low or high for slave mode operation.</td><td>1</td></tr>
<tr><td>$\overline{\text{HPM}}$</td><td>I</td><td>LCD drive power supply circuit power control.
$\overline{\text{HPM}}$ = high: Normal mode
$\overline{\text{HPM}}$ = low: High power mode
This pin is only valid in master mode. This pin must be held either low or high for slave mode operation.</td><td>1</td></tr>
</table>

LCD Drive Pins

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>SEG0 to SEG131</td><td>O</td><td>LCD segment drive outputs.
One of the V_1, V_3, V_4, and V_{SS} levels is selected by the combination of the contents of display RAM and the FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display positive level</th><th>Display inverted level</th></tr>
<tr><td>H</td><td>H</td><td>V_1</td><td>V_3</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_4</td></tr>
<tr><td>L</td><td>H</td><td>V_3</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td><td>V_{SS}</td></tr>
<tr><td>Power saving mode</td><td>—</td><td colspan="2">V_{SS}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0 to COM80</td><td>O</td><td>LCD common drive outputs.
One of the V_1, V_2, V_5, and V_{SS} levels is selected by the combination of the scan data and the FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td>V_1</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td></tr>
<tr><td>L</td><td>L</td><td>V_5</td></tr>
<tr><td>Power saving mode</td><td>—</td><td>V_{SS}</td></tr>
</table></td><td>80</td></tr>
</table>

Test Pins

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of pins</th></tr>
<tr><td>TEST0 to 7</td><td>O</td><td>IC test pins. These pins must be left open.</td><td>8</td></tr>
<tr><td>TEST8</td><td>I</td><td>IC test pin. This pin must be left open.</td><td>1</td></tr>
</table>

Functional Description

Microcontroller Interface

- Interface type selection
  The LC73101C transfers data over either an 8-bit bidirectional data bus (D0 to D7) or a serial data input system (SI). Applications can select either 8-bit parallel data input or serial data input as shown in table 1 by setting the P/S pin either high or low.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
High: Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
Low: Serial input	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	High impedance

- Parallel interface
  When the parallel interface is selected (P/S = high), the bus of either an Intel-type or a Motorola-type microcontroller can be directly connected to the LC73101C parallel interface by setting the C86 pin either high or low as shown in table 2.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
High: Mptorola-type MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
Low: Intel-type MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

- Serial interface
  When the serial interface is selected (P/S = low), data can be written to the LC73101C using the serial input (SI) and serial clock (SCL) pins with the chip in the active state (CS1 = low, CS2 = high). The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is acquired from the serial data input pin in the order D7 to D0 on the rising edge of the serial clock signal. The serial data is converted to 8 bits of parallel data on the eighth rising edge of the serial clock and processed by the LC73101C.

  Whether the serial data input is display data or a command is determined by the state of the A0 input. When A0 is high, the data is display data, and when A0 is low, it is taken to be a command. The A0 input is acquired and interpreted once every eight rising edges (that is, on the 8×th rising edge) of the serial clock signal after the chip goes to the active state.

  Figure 1 shows the timing chart for the serial interface.

  When the chip is in a non-active state due to the $\overline{CS1}$ and CS2 inputs, the shift register and the counter are reset. The serial interface does not support readout. Be sure to prevent termination reflections and noise from appearing on the SCL signal. We recommend testing in an actual end product.

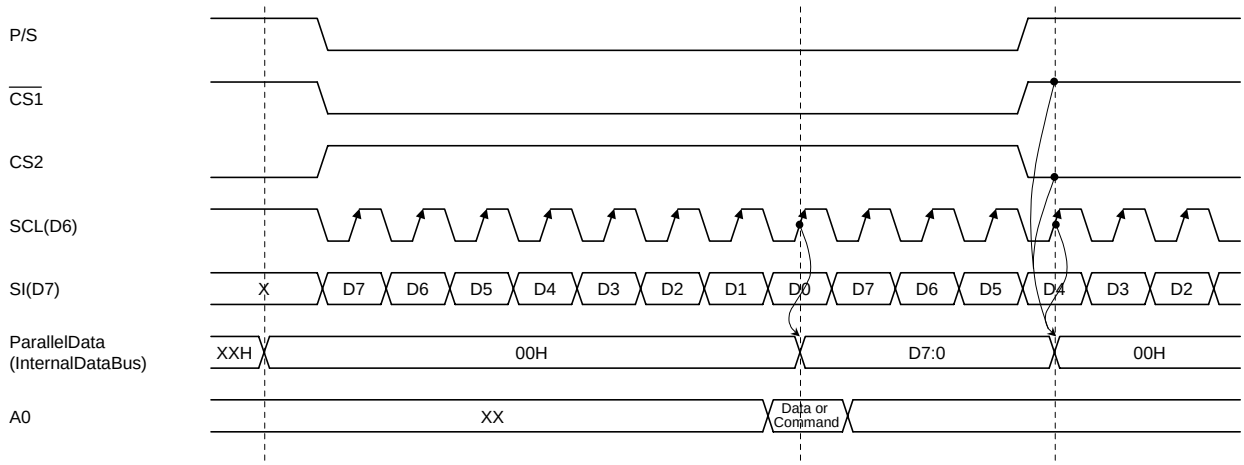


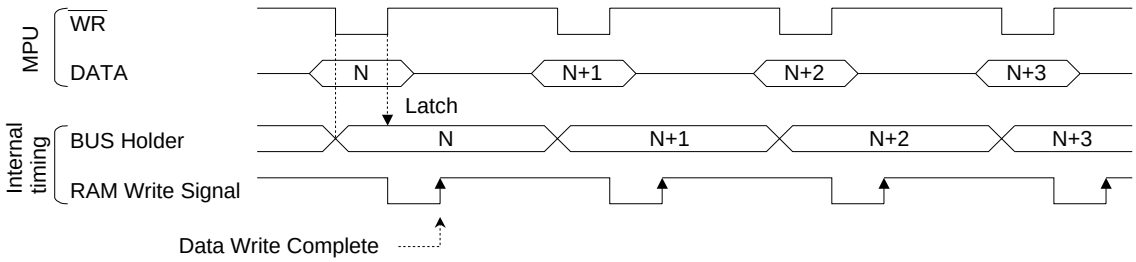
Figure 1

• Chip select
The LC73101C has two chip select inputs: $\overline{CS1}$ and CS2. The microcontroller and the serial interface can only be used when $\overline{CS1}$ is low and CS2 is high. When the chip select inputs select a non-active state, the D0 to D7 pins go to the high-impedance state and the A0, $\overline{RD}$, and $\overline{WR}$ inputs are disabled. The serial interface shift register and counter are reset.

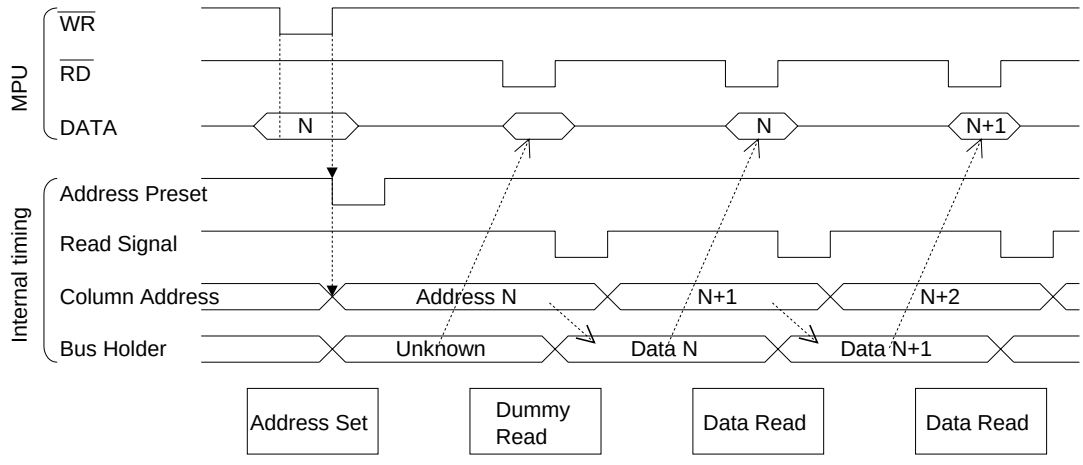
• Access to display data RAM and internal registers
The LC73101C supports high-speed data transfers that require no wait time as long as the LC73101C access cycle time constraints are met by the microcontroller. The LC73101C uses an internal “bus holder” circuit on its internal data bus to receive or send data during data transfers with the microcontroller.

For example, when the microcontroller writes to LC73101C display data RAM, the data is temporarily held by the bus holder and written to the display data RAM before the next write cycle. When the microcontroller reads out the contents of the display data RAM, data read out on the first (dummy) read cycle is stored in the bus holder, and then that data is read out onto the system bus on the next data read cycle. When reading display data RAM, after setting the address, the immediately following read instruction does not read out the data at the address specified, but rather reads out the data from the address specified by the second preceding data read operation. Thus care is required when using this function. This means that one dummy read operation is always required after setting the address or after a write cycle. Figure 2 (a) and figure 2 (b) show this timing.

(a) Write



(a) Read



• Busy flag
When the busy flag is high, it indicates that an LC73101C internal operation is in progress.

The busy flag is output from the D7 pin by a Status Read command. If the cycle time (t_{CYC}) conditions are met, there is no need to check this flag before each command. This can significantly increase the available processing power of the microcontroller.

Display Data RAM

- Display data RAM
  The display data RAM holds the dot data to be displayed, and has an 80 (10-page × 8-bit) × 132-bit organization. This memory is accessed by specifying a page address and a column address to access data in 8-bit units. Since the display data D7 to D0 from the microcontroller corresponds to the direction of the LCD common pins as shown in figure 3, when two LC73101C chips are used together, there are few constraints or limitations when transferring data, and highly flexible display structures can be implemented easily. Read and write operations to this display data RAM are performed through an I/O buffer, and thus these operations are independent of signal reads for LCD drive. This means that flicker and other problems do not occur when the display RAM is accessed asynchronously during display on the LCD panel.

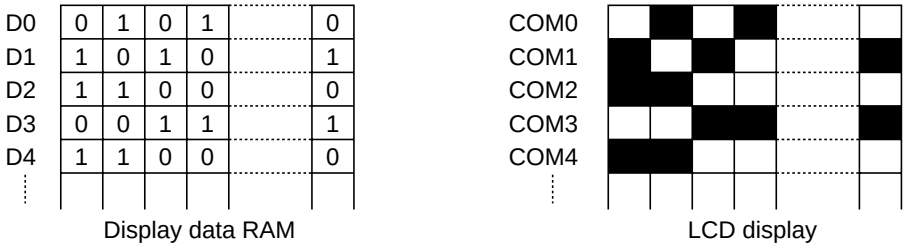


Figure 3 Noninverting LCD Display

- Page address circuit
  The display data RAM page address shown in figure 4 is specified using the Page Address Set command. The page address must be specified again to access a different page.

- Column address circuit
  The display data RAM column address shown in figure 4 is specified using the Column Address Set command. Since the specified column address is incremented each time a display data read or write command is input, the microcontroller can access the display data consecutively. Note that this column address incrementing stops when the column address reaches 83H. Since the column address and the page address are mutually independent, the column address and the page address must both be specified again to access a different column on a different page. Additionally, the correspondence between the display data RAM column address and segment output can be inverted with the CSS command (Column Address/Segment Output Correspondence Selection command) as shown in table 3. This reduces constraints on IC positioning when assembling LCD modules.

Table 3

CSS setting (D0)	Column address		Segment output
0	0H	→	SEG0
	83H	→	SEG131
1	0H	→	SEG131
	83H	→	SEG0

- Line address circuit

  The line address circuit specifies the line address corresponding to the COM output when the contents of display data RAM are displayed as shown in figure 4. Normally, the Display Start Line Address Set command specifies the uppermost line of the display (which depends on the common output state: in normal mode: COM0 output; in the inverted state: COM79 output). The maximum display area is 80 lines in the direction of increasing line address values from the specified display start line address.

  The data for the line address set by the Display Start Line Address Set command is passed to the common output driver specified by the Common Output State Selection command and the address set by the Display Start Common Address Set command in the common address circuit.

  Operations such as scrolling the screen and switching pages can be implemented by changing display start line address with this Display Start Line Address Set command.

- Common address circuit

  The line address circuit passes the display data for the line address determined by the line address circuit to the common output driver offset by the number of lines set by the Display Start Common Address Set command. Additionally, at this time the correspondence (figure 4) between the common output driver and the common address specified by the Common Output State Selection command is take into consideration.

  During partial display, the display position on the screen can be changed by changing this address without rewriting the contents of display RAM.

- Display data latch circuit

  The display data latch circuit is a latch that temporarily holds the display data output to the LCD drive circuit from data display RAM. Since the display normal/inverted and display on/off commands control this latched data, the data in display data RAM is not changed by these functions.

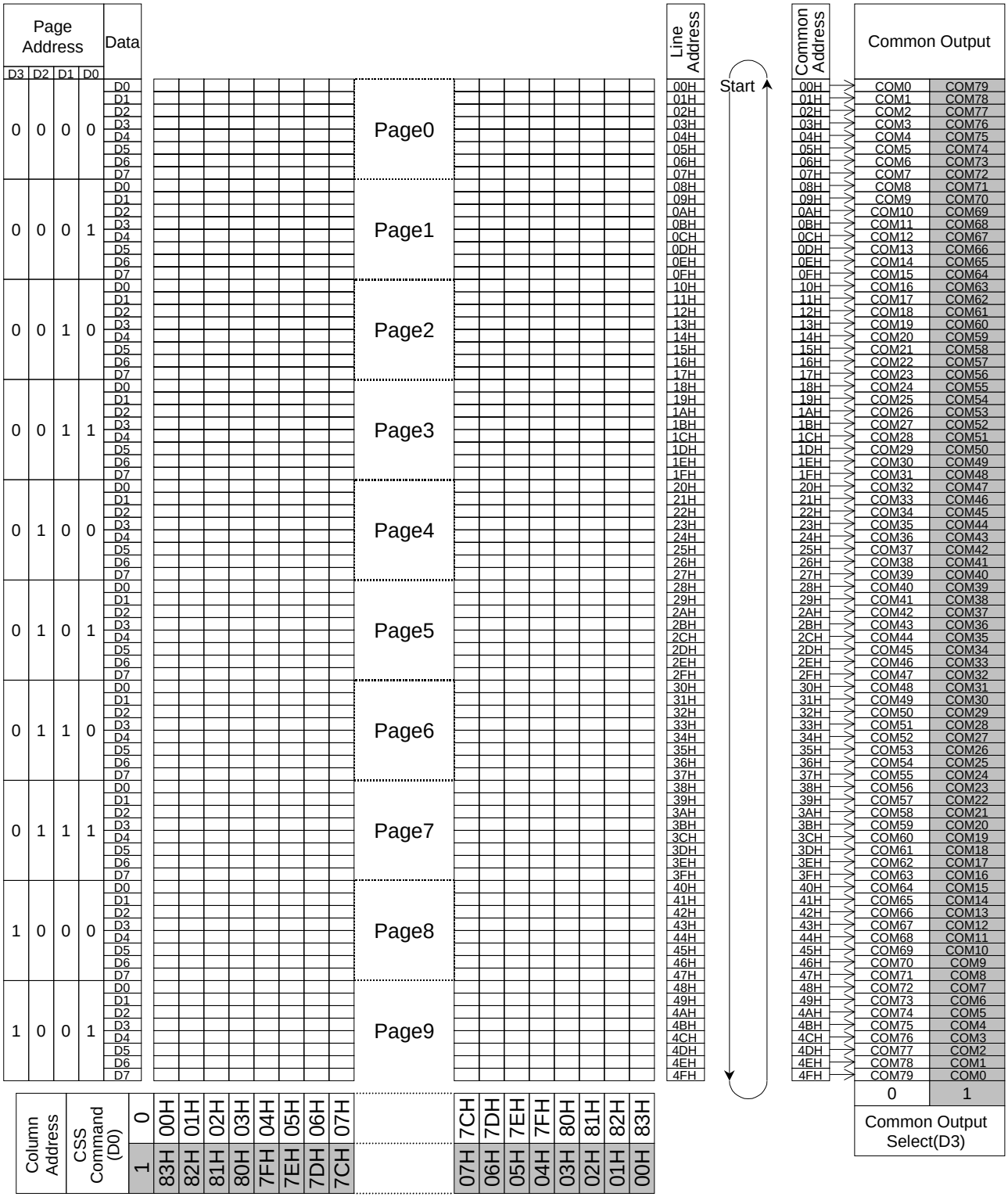


Figure 4 Display RAM Address Map

Partial Display Function

- Partial display function
  The LC73101C provides commands that control the following settings: the LCD drive duty setting, the LCD drive bias selection, the number of stages of voltage step-up, the display start line address, and the display start common address. These settings can be used to only display part of the screen.

  The number of lines displayed by the partial display function can be selected to be 8, 16, 24, 32, 40, 48, 56, 64, 72, or 80 lines. This is set by setting the LCD duty. The start of the frame is the display start line, and by setting this line to be the display start common address, it is possible to select any of the COM0 to COM79 lines.

  In general, as the LCD drive duty is reduced, the optimal values of the LCD drive voltage and LCD drive bias also become smaller. Since this allows the number of step-up stages in the voltage step-up circuit to be reduced, power consumption can be reduced significantly.

- Duty and frame frequency
  Table 4 shows the relationship between the duty setting, the number of lines, the display clock frequency f_{CL}, and the frame frequency f_{FR}.

Table 4

Duty	Number of lines displayed	f_{CL} [kHz]	f_{FR} [Hz]
80	80	6.40	80.0
72	72	5.12	71.1
64	64	5.12	80.0
56	56	4.27	76.2
48	48	3.66	76.2
40	40	3.20	80.0
32	32	2.56	80.0
24	24	1.97	82.1
16	16	1.28	80.0
8	8	0.640	80.0

Oscillator Circuit

This circuit is an RC circuit that generates the display clock. The oscillator circuit is only enabled when M/S is high and CLS is high. When CLS is low, the oscillator circuit is stopped and the display clock is input to the CL pin.

Display Timing Generator

This circuit generates the timing signals for the line address circuit and the display data latch circuit from the display clock. The display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment drive output pins. Readout of the display data to the LCD drive circuit is completely independent of microcontroller access to the display data RAM. This means that flicker or other problems never occur due to the display RAM being accessed asynchronously during display on the LCD panel. This circuit also generates the internal common timing and the LCD alternation signal (FR) from the display clock. The two-frame alternation drive waveforms shown in figure 5 are generated for the LCD drive circuit.

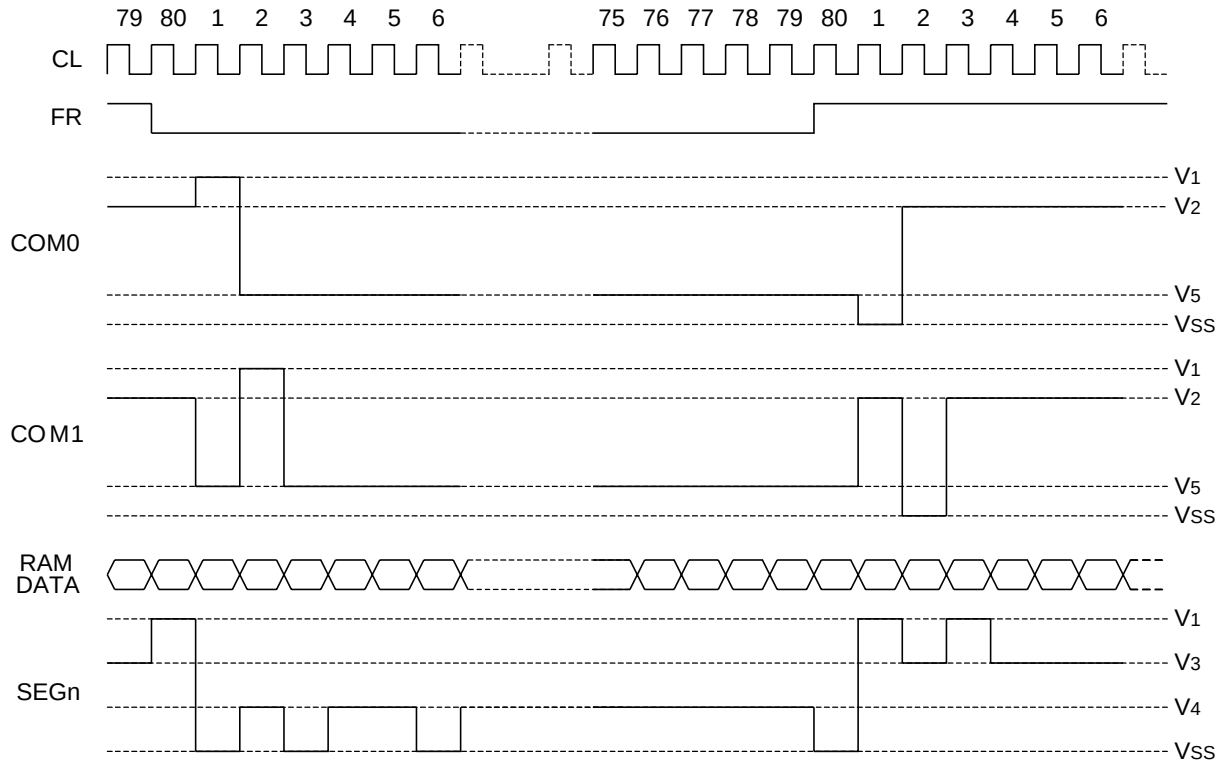


Figure 5 Frame Alternation Drive Waveforms

When the LC73101C is used in a multi-chip configuration, the display timing signals (FR, CL, and DOF) must be provided to the slave by the master.

Table 5 shows the states of the FR, CL, and $\overline{\text{DOF}}$ pins.

Table 5

Setting		FR	CL	$\overline{\text{DOF}}$
M/S	CLS			
"H"	"H"	Output	Output	Output
	"L"	Output	Input	Output
"L"	"H" or "L"	Input	Input	Input
	"H" or "L"	Input	Input	Input

Common Output State Selection Circuit

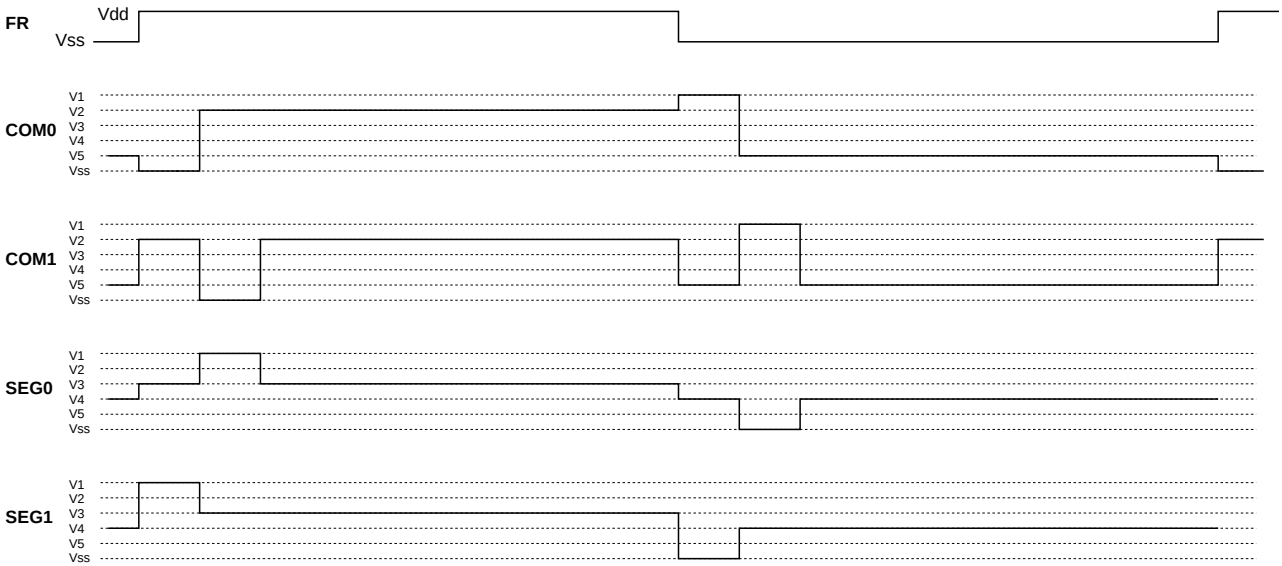
The LC73101C allows the scan direction of the COM outputs to be set with the common output state selection circuit. This reduces constraints on IC positioning when assembling LCD modules. (See table 6.)

Table 6

Common Output State Selection command (D3)	Selected state
0	Normal: COM0 → COM79
1	Inverted: COM79 → COM0

LCD Drive Circuit

The LCD drive voltages are output according to the combination of the display data, the COM scan signal, and the FR signal. Figure 6 shows the SEG and COM output waveform examples for the frame alternation drive technique used.



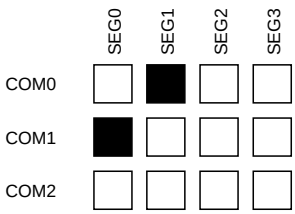


Figure 6

Power Supply Circuit

This circuit is a low power consumption power supply circuit that creates the voltages required for LCD drive. It can only be used when the LC73101C is in master mode. It consists of a voltage step-up circuit, a voltage adjustment circuit, and a voltage follower circuit. The on/off states of the voltage step-up circuit and the voltage adjustment circuit in the power supply can be controlled individually with the Power Control Set command. This allows external power supply levels to be used in combination with certain of the functions of the internal power supply circuit. Table 7 lists the functions controlled by the 3 bits of data in the Power Control Set command, and table 8 presents examples of possible combinations of functions.

Table 7 Power Control Set Command Bit Functions

Bit	Item set	Bit value	
		1	0
D2	Voltage step-up circuit	ON	OFF
D1	Voltage adjustment circuit (V adjustment circuit)	ON	OFF
D0	Voltage follower circuit (V/F circuit)	ON	OFF

Table 8 Sample Combinations

		D2	D1	D0	Step-up circuit	V adjustment circuit	V/F circuit	External voltage input	Step-up system pins
1.	Only the internal power supply used	1	1	1	○	○	○	V_{SS2}	Used
2.	Only the V adjustment and V/F circuits used	0	1	1	×	○	○	V_{OUT}, V_{SS2}	Open
3.	Only the V/F circuit used	0	0	1	×	×	○	V_5, V_{SS2}	Open
4.	External power supply only	0	0	0	×	×	×	V_1 to V_5	Open

Note: The step-up system pins are the CAP1+, CAP1–, CAP2+, CAP2–, CAP3+, CAP3–, CAP4+, CAP4–, CAP5+, and CAP5– pins.
While combinations other than the above are possible, these other combinations are impractical and are not recommended.

- Voltage step-up circuit
  The LC73101C's built-in voltage step-up circuit can generate potentials that are 3×, 4×, 5×, and 6× that of the potential between V_{SS2} and V_{DD}. Figure 7 shows the relationships between these potentials.

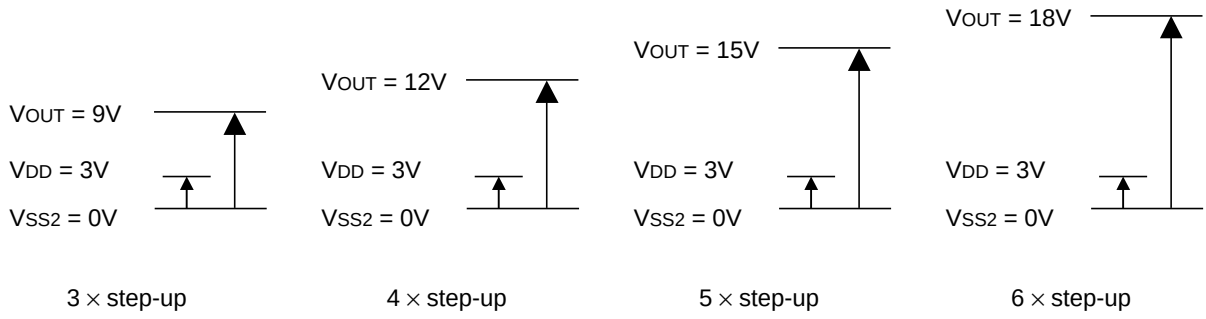


Figure 7 The relationships between these potentials

• Voltage adjustment circuit
The stepped-up voltage generated at the V_{OUT} pin is output as the V_1 LCD drive voltage through the power supply adjustment circuit. Since the LC73101C provides a reference voltage based on a high-precision constant-voltage source, an electronic potentiometer with 64 levels, and furthermore, a voltage adjustment resistor built in to the V_1 pin, a high-precision voltage adjustment circuit can be implemented with a minimal number of external components. Figure 8 shows this voltage adjustment circuit.

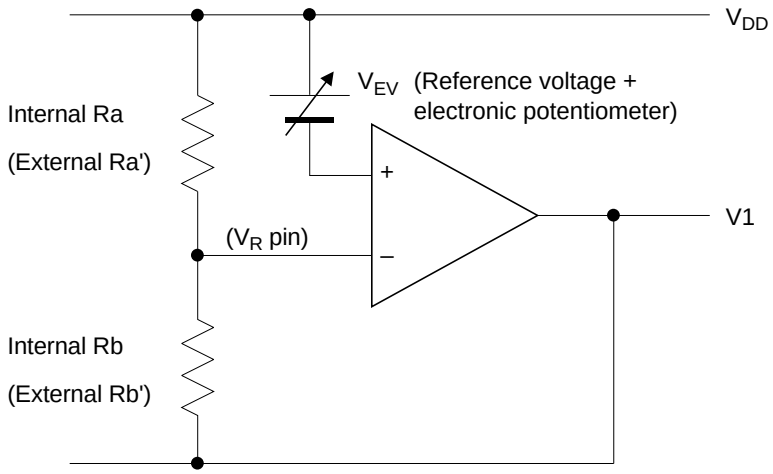


Figure 8 Voltage Adjustment Circuit

The formulas below show the relationship between Ra, Rb, V_{REG}, V_{EV}, and V_1. The term α is the set value of the electronic potentiometer.

$$V_{EV} = \left(1 - \frac{\alpha}{162}\right) \times V_{REG}$$

$$V_1 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV}$$

(1) Reference voltage

The LC73101C includes a constant-voltage supply that features a selectable temperature correction coefficient: one of three slopes can be selected. The Reference Supply Selection command is used to select the slope. This command can also be used to isolate (disconnect) the internal low-voltage supply so that the reference voltage can be supplied from the external V_{RS} pin. The bits D0 and D1 in the Reference Supply Selection command control these settings. Table 9 lists the reference voltage V_{REG} values that correspond to the D0 and D1 settings.

Table 9

D1	D0	Setting	V_{REG}
0	0	Internal reference voltage: Off	Input from the V_{RS} pin
0	1	Temperature coefficient: –0.05%	–2.5 V
1	0	Temperature coefficient: –0.1%	–2.5 V
1	1	Temperature coefficient: –0.2%	–2.5 V

(2) Electronic potentiometer

The electronic potentiometer function can be used when the voltage adjustment circuit is activated by the Power Control Set command.

The electronic potentiometer adjusts the reference voltage using a resistor divider. This adjustment is set using the Electronic Potentiometer Mode Set command and the Electronic Potentiometer Register Set 2-Byte command. Table 10 lists the correspondence between the 6 bits of setting data specified by these commands and the value of the α parameter.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		↓				↓
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

(3) Voltage adjustment using the internal resistor

The internal voltage adjustment resistor can be used when the IRS pin is high. Here, the VR pin should be left open. The internal resistor ratio (1 + Rb/Ra) can be set with the V_1 Adjustment Internal Resistor Ratio Set command.

Table 11 lists the correspondence between the 4 bits of data specified by this command and the value of the ratio (1 + Rb/Ra) set by that command. See the section "V_1 voltage Adjustment Internal Resistor Ratio Set Command" in the command descriptions for details on using this command.

Table 11

V_3	V_2	V_1	V_0	1 + Rb/Ra
0	0	0	0	1.5
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5

(4) Voltage adjustment using external resistors

When the IRS pin is low, the built-in voltage adjustment resistor is disconnected and the voltage can be adjusted using external resistors. Divide the voltage between V_{DD} and V_5 with the external resistors Ra' and Rb' and apply that voltage to the V_R pin.

LCD Voltage Generation Circuit

The V_1, V_2, V_3, and V_4 potentials required for LCD drive are generated by resistor division of the V_1 voltage internally to the IC. The voltage followers are used to convert the impedance of the V_1, V_2, V_3, and V_4 potentials and supply those levels to the LCD drive circuit. The bias ratio can be set with the LCD Bias Set command. Table 12 shows the correspondence between the 6 bits of data specified by this command and value of the bias setting set by that data.

Table 12

D2	D1	D0	Bias setting
0	0	0	1/10
0	0	1	1/9
0	1	0	1/8
0	1	1	1/7
1	0	0	1/6
1	0	1	1/5
1	1	0	1/4

High Power Mode

The power supply circuit built into the LC73101C is an extremely low power consumption circuit in normal mode (when $\overline{\text{HPM}}$ is high). As a result, the display quality with panels or LCDs that present a relatively large load may be compromised. In such cases, the display quality can be improved by setting the $\overline{\text{HPM}}$ pin low to switch the LC73101C to high power mode. We recommend testing in an actual system to decide whether or not to use this mode. Note that it may be necessary to use an external power supply for LCD drive if high power mode cannot provide adequate display quality.

Reset Circuit

The LC73101C is reset to the initialized state by a low level applied to the $\overline{RES}$ input. The following describes the initialized state.

(1) Display: off

(2) Display normal

(3) ADC selection: Normal (ADC command D0 = 0)

(4) Power control register (D2, D1, D0) = (0, 0, 0)

(5) Serial interface internal register data: cleared

(6) LCD power supply bias ratio: 1/10

(7) Display: all dots off.

(8) Power saving function: disabled

(9) V_1 voltage adjustment internal resistors Ra and Rb: Disconnected.

(10) The SEG and COM outputs go to the V_{SS} level while $\overline{RES}$ is low.

(11) Read-modify-write: off

(12) Display start line address: 00H

(13) Display start common address: 00H

(10) Column address: 00H

(11) Page address: page 0

(12) Common output state: Normal order

(13) V_1 voltage adjustment internal resistor ratio: 1.5

(14) Electronic potentiometer register set mode: cleared
Electronic potentiometer register (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)

(15) LCD bias register set mode: cleared
LCD bias register (D2, D1, D0) = (0, 0, 0)

When the Reset command is used, only items (7) to (15) in the above initialization items are reset as shown.

The $\overline{RES}$ pin can be connected to the microcontroller reset pin so that both the LC73101C and the microcontroller are reset at the same time. The LC73101C must be initialized with the $\overline{RES}$ pin when power is first applied. Note that overcurrents may flow in this IC if the control signals from the microcontroller are in the high-impedance state. Applications must be designed so that the input pins are not connected to high-impedance lines when power is first applied. If the internal LCD power supply circuit is not used, the $\overline{RES}$ pin must be at the low level when the external LCD power supply is turned on.

Commands

1. Display On/Off

Controls the on/off state of the LCD panel. The D0 bit sets the on/off state of the LCD display.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	0	Display off
										1	Display on

When a Display Off command is issued in the display fully on (all lit by All Display Pixels Lit On command) state, the device goes to the power saving state.

2. Display Start Line Set

Sets the line address for the start of display from display data RAM. This address is set in two operations: first the upper 3 bits and then the lower 4 bits. Both the upper and lower bits can be set independently.

At reset, the display start line address is reset to 00H. The display can be scrolled by periodically changing the display start line address with this command. In partial display mode, the content displayed can be changed without changing the contents of display RAM by changing the address with this command.

See the functional description in the “Line Address Circuit” section for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	X	L6	L5	L4
			0	1	0	1	L3	L2	L1	L0

L6	L5	L4	L3	L2	L1	L0	Display start line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
			↓				↓
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

3. Display Start Common Set

Sets the common address for the start of display from display data RAM. This address is set in two operations: first the upper 3 bits and then the lower 4 bits. Both the upper and lower bits can be set independently.

At reset, the display start common address is reset to 00H. In partial display mode, the content displayed position can be changed without changing the contents of display RAM by changing the address with this command.

See the functional description in the “Common Address Circuit” section for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	0	X	C6	C5	C4
			0	1	1	1	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Display Start Common Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
			↓				↓
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79

4. Page Address Set

Sets the page address used when the display data RAM is accessed from the microcontroller.

The display data RAM is accessed in 8-bit units using a page address and a column address.

At reset, the page address is reset to 0.

See the functional description in the "Page Address Circuit" section for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							1	0	0	0	8
							1	0	0	1	9

5. Column Address Set

Sets the column address for display data RAM. This address is set in two operations: first the upper 4 bits and then the lower 4 bits. The column address is automatically incremented (+1) each time display data RAM is accessed. Thus there is no need to issue this command each time this RAM is read or written, and the microcontroller can read or write display data consecutively.

Automatic increment of the column address stops when it reaches 83H.

See the functional description in the "Column Address Circuit" section for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	M7	M6	M5	M4
			0	0	0	0	M3	M2	M1	M0

M6	M5	M4	M3	M2	M1	M0	Column Start Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
			↓				↓
1	0	0	0	0	1	0	130
1	0	0	0	0	1	1	131

6. Status Read

Allows the microcontroller to read out the IC state from the status data.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	ST4	ST3	ST2	ST1	1	1	1	1

ST1	Busy flag When ST1 is 1, indicates that either a read operation or an internal operation is in progress. This command can be issued until ST1 becomes 0. However, there is no need to check this flag if the cycle time conditions are met.
ST2	Indicates the correspondence between column addresses and segment drivers. 0: Inverted (Column addresses 0H → 83H: SEG0 → SEG131) 1: Normal (Column addresses 0H → 83H: SEG131 → SEG0)
ST3	Indicates the on/off state of the display. (This value has the reverse polarity of the Display On/Off command.) 0: Display on 1: Display off
ST4	Indicates that an initialization operation due to either the $\overline{RES}$ signal or a Reset command. 0: Operating state 1: Reset in progress

7. Display Data Write

Writes 8 bits of data to the address specified for display data RAM. After the write, the column address is automatically incremented to allow the microcontroller to write display data continuously.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

8. Display Data Read

Reads 8 bits of data from the address specified for display data RAM. After the read, the column address is automatically incremented to allow the microcontroller to read display data continuously.

Note that one dummy read is required immediately after the column address is set. It is not possible to read out display data using the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

9. Column Address/Segment Output Correspondence Selection

Allows the correspondence between the display RAM data column address and the segment driver outputs to be inverted.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal: Column address 0 → SEG0
											Column address 131 → SEG131
										1	Inverted: Column address 0 → SEG131
											Column address 131 → SEG0

10. Display Normal/Inverted

Allows pixel on/off states to be inverted without rewriting the contents of display data RAM.

The contents of display data RAM are retained unchanged by this operation.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data high → LCD pixel on
										1	RAM data low → LCD pixel on

11. All Display Pixels Lit On/Off

Allows all the pixels in the display to be forcibly set to the on state regardless of the contents of display data RAM.

The contents of display data RAM are retained unchanged by this operation.

This command takes priority over the Display Normal/Inverted command.

When a Display All Pixels Lit On command is issued with the device in the display off state, the device goes to the power saving state.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	All pixels lit state.

12. LCD Bias

These commands select the bias ratio for the voltages required for LCD drive.

These commands form a 2-byte command pair: the Electronic Potentiometer Mode Set command and the Electronic Potentiometer Register Set command. These two commands must be issued consecutively.

LCD Bias Mode Set

When this command is issued, the LCD Bias Register Set command is enabled. Once the electronic potentiometer mode is set, no command other than the LCD Bias Register Set command can be used. This state is cleared after data is stored into the register with the LCD Bias Register Set command.

This command is cleared when a reset input occurs or when a reset command is issued.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	0

LCD Bias Register Set

Stores 3 bits of data into the LCD bias register to select one of 6 bias values.

LCD bias mode is cleared after the LCD bias register is set by issuing this command.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	0	0	0	0	0	0	1/10
								0	0	1	1/9
								0	1	0	1/8
								0	1	1	1/7
								1	0	0	1/6
								1	0	1	1/5

The bias is set to 1/10 if a value other than those listed above is used for D2 to D0.

13. Read/Modify/Write

Used as a pair with the End command. Once this command has been issued, the column address is not changed by the Display Data Read command, but is only incremented by the Display Data Write command. This state remains in effect until an End command is issued. When an End command is issued, the column address returns to the address it held at the point the Read/Modify/Write command was issued.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

14. End

Clears read/modify/write mode and returns the column address to its address at the start of this mode.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

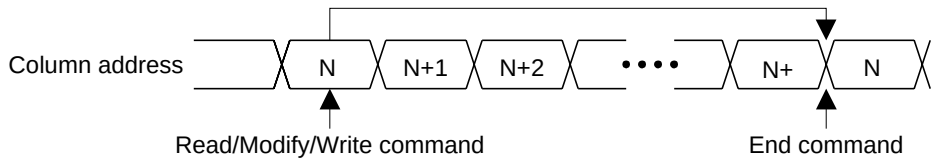


Figure 9

15. Reset

Initializes the display start line, column address, page address, common output state, V_1 voltage adjustment internal resistor ratio, and electronic potentiometer and clears read/modify/write mode and test mode. A reset has no effect on the contents of display data RAM. The reset operation is performed after the reset command is issued.

Apply a reset signal to the $\overline{RES}$ pin for initialization when power is first applied.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The reset state is cleared by issuing a NOP command. A NOP command must be issued after a reset.

16. Common Output State Selection

Selects the scan direction for the COM output pins.

The common signals are output sequentially in the scan direction selected with this command from the selected frame start position for the specified display start common setting.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	1	1	0	0	0	×	×	×	Normal: COM0 → COM79
							1				Inverted: COM79 → COM0

17. Power Control Set

Specifies the functions of the power supply circuit. See the functional description in the “Power Supply Circuit” section for details.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Step-up circuit: Off
								1			Step-up circuit: On
									0		V adjustment circuit: Off
									1		V adjustment circuit: On
										0	V/F circuit: Off
										1	V/F circuit: On

(V/F circuits: Voltage follower circuit; V adjustment circuit: voltage adjustment circuit)

18. V_1 Voltage Adjustment Internal Resistor Ratio Set

Sets the V_1 voltage adjustment internal resistor ratio. The four bits of this setting are specified using two consecutive commands: one to set the upper 2 bits, and the other to set the lower 2 bits.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	V3	V2
			0	0	1	0	0	0	V1	V0

V3	V2	V1	V0	1 + Rb/Ra
0	0	0	0	1.5
0	0	0	1	2.0
0	0	1	0	2.5
0	0	1	1	3.0
0	1	0	0	3.5
0	1	0	1	4.0
0	1	1	0	4.5
0	1	1	1	5.0
1	0	0	0	5.5
1	0	0	1	6.0
1	0	1	0	6.5

19. Electronic Potentiometer

Controls the LCD drive voltage V_1 output from the internal LCD power supply voltage adjustment circuit and adjusts the contrast of the LCD display.

These commands form a 2-byte command pair: the Electronic Potentiometer Mode Set command and the Electronic Potentiometer Register Set command. These two commands must be issued consecutively.

19-1. Electronic Potentiometer Mode Set

When this command is issued, the electronic Potentiometer Register Set command is enabled. Once the electronic potentiometer mode is set, no command other than the Electronic Potentiometer Register Set command can be used. This state is cleared after data is stored into the register with the Electronic Potentiometer Register Set command.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

19-2. Electronic Potentiometer Register Set

This command sets the LCD drive voltage V_1 to one of 64 voltage levels by writing 6 bits of data to the electronic potentiometer register.

Electronic potentiometer mode is cleared after this command is issued and the electronic potentiometer register has been set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	α
0	1	0	×	×	0	0	0	0	0	0	63
					0	0	0	0	0	1	62
					0	0	0	0	1	0	61
							↓				↓
					1	1	1	1	0	1	2
					1	1	1	1	1	0	1
					1	1	1	1	1	1	0

This register is set to (X, X, 1, 0, 0, 0, 0, 0) when the electronic potentiometer function is not used.

20. Power Save

The LC73101C can be set to its power saving mode by issuing the Display Off command and the All Display Pixels Lit On command. Power consumption can be reduced significantly by setting the LC73101C to power saving mode.

Display On/Off	All Display Pixels Lit	Setting
On	Off	Power saving mode cleared (normal operating state)
On	On	
Off	Off	
Off	On	Power saving mode

In power saving mode, the states of the display data and the operating mode prior to power saving mode are retained, and the microcontroller can access the display data RAM.

Power saving mode is cleared using the All Display Pixels Lit Off command.

In power saving mode, all LCD display system operations are stopped and current can be reduced to a value close to the quiescent current even when RAM is not accessed by the microcontroller. The internal states in this mode are as follows.

(1) The oscillator circuit and the LCD power supply circuit are stopped.

(2) All LCD drive circuits are stopped and the segment and common driver outputs go to the V_{SS} level.

21. NOP

This command is the no-op (no operation) command.

Issuing this command has no effects on the IC internal circuits.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Reference Supply Selection

This command sets the internal reference voltage temperature coefficient and the circuit's on/off state.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	1	0	×	0	0	Internal reference voltage: Off
									0	1	Temperature coefficient: –0.05%
									1	0	Temperature coefficient: –0.1%
									1	1	Temperature coefficient: –0.2%

23. Step-up Stages Count Set

This command sets the number of stages and the on/off state of the internal voltage step-up circuit.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	1	1	1	×	0	0	3× step-up
									0	1	4× step-up
									1	0	5× step-up
									1	1	6× step-up

24. Partial Drive Setup

This command sets the duty used during partial drive.

The line address starts at the display start line address and is incremented by the duty value set using this command. It then returns to the original display start line address.

The common address starts at the display start common address and is incremented by the duty value set using this command. It then returns to the original display start common address.

On the display screen, display starts from the common output selected by the display start common address, and only the number of lines given by the value of the specified duty are displayed in the direction that the address is incremented in.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Duty setting
0	1	0	1	0	0	1	0	0	0	0	80
							0	0	0	1	72
							0	0	1	0	64
							0	0	1	1	56
							0	1	0	0	48
							0	1	0	1	40
							0	1	1	0	32
							0	1	1	1	24
							1	0	0	0	16
							1	0	0	1	8

25. Test

This command is used for IC testing. It should not be used in end applications.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1		Test item.		

Command Table

Table 13

No.	Command	Command code											Function
		A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
1	Display On/Off	0	1	0	1	0	1	0	1	1	1	0 1	Controls the LCD display on/off state. 0: Off, 1: On
2	Display Start Line Set Upper bits	0	1	0	0	1	0	0	×	Upper address			Sets the upper 4 bits of the display RAM display start line address.
	Display Start Line Set Lower bits	0	1	0	0	1	0	1	Lower address				Sets the lower 4 bits of the display RAM display start line address.
3	Display Start Common Set Upper bits	0	1	0	0	1	1	0	×	Upper address			Sets the upper 4 bits of the display RAM display start common address.
	Display Start Common Set Lower bits	0	1	0	0	1	1	1	Lower address				Sets the lower 4 bits of the display RAM display start common address.
4	Page Address Set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address.
5	Column Address Set Upper bits	0	1	0	0	0	0	1	Upper column address				Sets the upper 4 bits of the display RAM display column address.
	Column Address Set Lower bits	0	1	0	0	0	0	0	Upper column address				Sets the lower 4 bits of the display RAM display column address.
6	Status Read	0	0	1	0	Status			0	0	0	0	Reads out the status information.
7	Display Data Write	1	1	0		Write data							Writes display data to display RAM.
8	Display Data Read	1	0	1		Read data							Reads display data from display RAM.
9	Column Address/Segment Output Correspondence Selection	0	1	0	1	0	1	0	0	0	0	0 1	Selects the correspondence between column addresses and segment outputs. 0: Column address 0 -> SEG0 1: Column address 0 -> SEG131
10	Display Normal/Inverted	0	1	0	1	0	1	0	0	1	1	0 1	Selects normal or inverted display on the LCD 0: Normal, 1: Inverted
11	All Display Pixels Lit On/Off	0	1	0	1	0	1	0	0	1	0	0 1	Turns on all the pixels on the LCD display. 0: Normal operation, 1: All pixels lit
12	LCD Bias Mode Set	0	1	0	1	0	1	0	0	0	1	0	Two-byte command Sets the LCD drive voltage bias ratio.
	LCD Bias Register Set	0	1	0	0	0	0	0	0	Bias value			
13	Read/Modify/Write	0	1	0	1	1	1	0	0	0	0	0	Sets up the read/modify/write state.
14	End	0	1	0	1	1	1	0	1	1	1	0	Clears the read/modify/write state.
15	Reset	0	1	0	1	1	1	0	0	0	1	0	Command-based reset function. Only resets a subset of the internal circuits.
16	Common Output State Selection	0	1	0	1	1	0	0	0 1	×	×	×	Selects the COM output scan direction. 0: Normal, 1: Reversed
17	Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the operating state of the internal power supply.
18	V_1 Voltage Adjustment Internal Resistor Ratio Set Upper bits	0	1	0	0	0	1	0	0	1	Upper bits		Sets the upper 2 bits of the 4-bit value that selects the internal resistor ratio (Rb/Ra).
	V_1 Voltage Adjustment Internal Resistor Ratio Set Lower bits	0	1	0	0	0	1	0	0	0	Lower bits		Sets the lower 2 bits of the 4-bit value that selects the internal resistor ratio (Rb/Ra).
19	Electronic Potentiometer Mode Set	0	1	0	1	0	0	0	0	0	0	1	Two-byte command Sets the electronic potentiometer.
	Electronic Potentiometer Register Set	0	1	0	0	0	Electronic potentiometer value						
20	Power Save	Display Off + All Display Pixels Lit On											This combination of commands sets and clears power saving mode.
21	NOP	0	1	0	1	1	1	0	0	0	1	1	Has no influence on IC operations.
22	Reference Supply Selection	0	1	0	0	0	1	1	0	×	Coefficient		Sets the coefficient for the internal reference voltage.
23	Step-up Stages Count Set	0	1	0	0	0	1	1	1	×	Number of stages		Sets the number of stages in the internal voltage step-up circuit.
24	Partial Drive Setup	0	1	0	1	0	0	1	Duty value				Sets the duty value.
25	Test	0	1	0	1	1	1	1	Test item				IC testing command. This command must not be used.

Note: ×: Don't care.

Electrical Characteristics

DC Characteristics

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum supply voltage	V_{DDMAX}		–0.3		+4.0	V
Bias voltage	V_1, V_{OUT}	$V_{SS} \le V_5 \le V_4 \le V_3 \le V_2 \le V_1$	–0.3		+20	V
Bias voltage	V_2, V_3, V_4, V_5		–0.3		V_1	V
Input voltage	V_{IN}		–0.3		V_{DD} + 0.3	V
Output voltage	V_O		–0.3		V_{DD} + 0.3	V
Operating temperature	Topr		–40		+85	°C
Storage temperature	Tstg		–50		125	°C

Recommended Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit	Applicable pins
			min	typ	max		
Supply voltage	V_{DD}		1.8		3.6	V	V_{DD}, V_{SS}
Bias voltage	V_{BI}		1.8		+18	V	V_{OUT}, V_1, V_2, V_3, V_4, V_5
Step-up circuit output voltage	V_{OUT}		1.8		+18	V	V_{OUT}
Operating temperature	Topr		–40		+85	°C	

DC Electrical Characteristics at Ta = –40 to 85°C, V_{SS} = 0 V

Parameter		Symbol	Conditions	Ratings			Unit	Applicable pins
				min	typ	max		
High-level input voltage		V_{IH}		0.8 V_{DD}		V_{DD}	V	*1
Low-level input voltage		V_{IL}		V_{SS}		0.2 V_{DD}	V	*1
High-level output voltage		V_{OH}	I_{OH} = –0.5 mA	0.8 V_{DD}		V_{DD}	V	*2
Low-level output voltage		V_{OL}	I_{OL} = 0.5 mA	V_{SS}		0.2 V_{DD}	V	*2
High-level input current		I_{IH}	V_{IH} = V_{DD}	–1.0		+1.0	µA	*3, 4
Low-level input current		I_{IL}	V_{IL} = V_{SS}	–1.0		+1.0	µA	*3, 4
LCD driver on resistance		R_{ON}	V_1 = 14.0 V, Ta = 25°C		2.0	3.5	kΩ	SEGn
			V_1 = 8.0 V, Ta = 25°C		3.2	5.4		COMn
Current drain (normal mode)		I_{OP1}	f_{OSC} = 25.6 kHz, 1/80 duty Data that specifies all display pixels off, Ta = 25°C, V_{DD} = 3.0 V, 4 × step-up circuit used.		Not fixed	Not fixed	µA	V_{DD}
Current drain (high-power mode)		I_{OP2}	f_{OSC} = 25.6 kHz, 1/80 duty Data that specifies all display pixels off, Ta = 25°C, V_{DD} = 3.0 V, 3 × step-up circuit used.		Not fixed	Not fixed	µA	V_{DD}
Current drain (sleep mode)		I_{DDS}	V_{DD} = 3.0 V, Ta = 25°C		Not fixed	Not fixed	µA	V_{DD}
Input pin capacitance		C_{IN}	f = 1 MHz, Ta = 25°C		5.0	8.0	pF	
Oscillator frequency	Internal oscillator	f_{OSC}	Ta = 25°C	21.0	25.6	30.2	kHz	CL
	External input	f_{CL}		21.0	25.6	30.2	kHz	CL

Notes: 1. A0, D0 to D7, $\overline{RD}$, $\overline{WR}$, $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$
2. D0 to D7, FR, CL, and $\overline{DOF}$
3. A0, $\overline{RD}$, $\overline{WR}$, $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, IRS, and $\overline{HPM}$
4. All input pins. However, applies when D0 to D7, CL, FR, and $\overline{DOF}$ are in the high-impedance state.

AC Characteristics

• System Bus Read/Write Characteristics (1) (Intel-type microcontrollers)

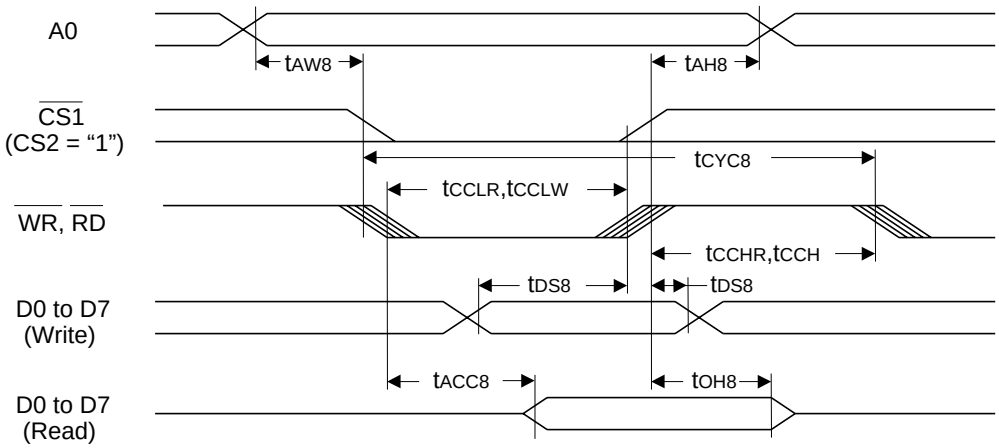


Figure 10

V_{DD} = 2.7 to 3.6 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings		Unit
				min	max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		T_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		300	—	ns
Control low-level pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control low-level pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	
Control high-level pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	
Control high-level pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	

V_{DD} = 1.8 to 2.7 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings		Unit
				min	max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		T_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		1000	—	ns
Control low-level pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control low-level pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	
Control high-level pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	
Control high-level pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Address hold time		t_{DH8}		30	—	
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	

Notes: 1. The input signal rise and fall times (t_r, t_f) are stipulated to be under 15 ns. When using a short system cycle time for high-speed operation, these are stipulated as follows: $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$

2. All timings are stipulated to be referenced to 20% and 80% of V_{DD}.

3. t_{CCLW} and t_{CCLR} are stipulated to be the overlap time when $\overline{CS1}$ is low (CS2 is high) and $\overline{WR}$ and $\overline{RD}$ are low.

• System Bus Read/Write Characteristics (2) (Motorola-type microcontrollers)

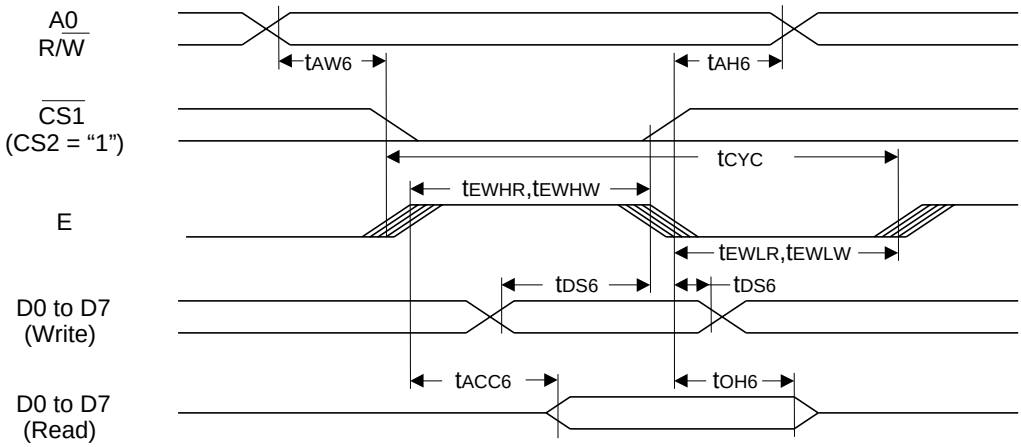


Figure 11

V_{DD} = 2.7 to 3.6 V, Ta = –40 to 85°C

Parameter		Signal	Symbol	Conditions	Ratings		Unit
					min	max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			T_{AW6}		0	—	
System cycle time		A0	t_{CYC6}		300	—	ns
Data setup time		D0 to D7	t_{DS6}		40	—	ns
Address hold time			t_{DH6}		15	—	
Access time		D0 to D7	t_{ACC6}	C_L = 100 pF	—	140	ns
Output disable time			t_{OH6}		10	100	
Enable high-level pulse width	Read	E	t_{EWHR}		120	—	ns
	Write		t_{EWHW}		60	—	
Enable low-level pulse width	Read	E	t_{EWLR}		60	—	ns
	Write		t_{EWLW}		60	—	

V_{DD} = 1.8 to 2.7 V, Ta = –40 to 85°C

Parameter		Signal	Symbol	Conditions	Ratings		Unit
					min	max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			T_{AW6}		0	—	
System cycle time		A0	t_{CYC6}		1000	—	ns
Data setup time		D0 to D7	t_{DS6}		80	—	ns
Address hold time			t_{DH6}		30	—	
Access time		D0 to D7	t_{ACC6}	C_L = 100 pF	—	280	ns
Output disable time			t_{OH6}		10	200	
Enable high-level pulse width	Read	D0 to D7	t_{EWHR}		240	—	ns
	Write		t_{EWHW}		120	—	
Enable low-level pulse width	Read	D0 to D7	t_{EWLR}		120	—	ns
	Write		t_{EWLW}		120	—	

Notes: 1. The input signal rise and fall times (t_r, t_f) are stipulated to be under 15 ns. When using a short system cycle time for high-speed operation, these are stipulated as follows: $(t_r + t_f) \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $(t_r + t_f) \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$
2. All timings are stipulated to be referenced to 20% and 80% of V_{DD}.
3. t_{EWLW} and t_{EWLR} are stipulated to be the overlap time when $\overline{CS1}$ is low (CS2 is high) and E is low.

• Serial Interface

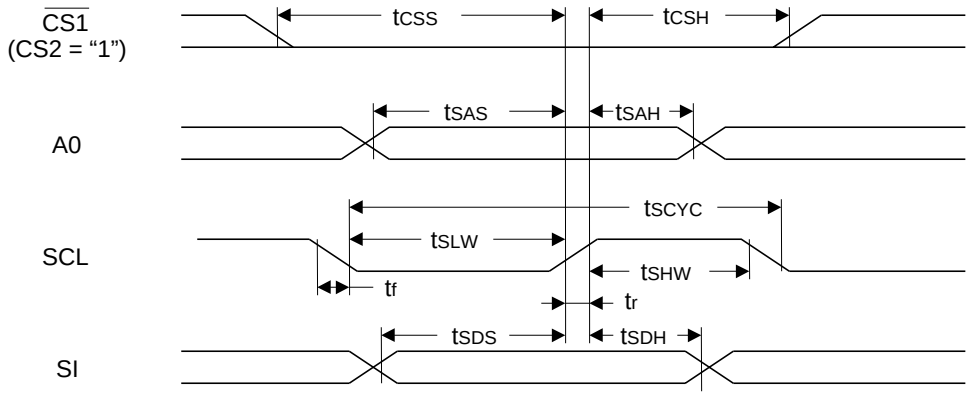


Figure 12

V_{DD} = 2.7 to 3.6 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings		Unit
				min	max	
Serial clock period	SCL	t_{SCYC}		250	—	ns
SCL high-level pulse width		t_{SHW}		100	—	
SCL low-level pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	ns
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	ns
Data hold time		t_{SDH}		100	—	
CS to CSL time	CS	t_{CSS}		150	—	ns
		t_{CSH}		150	—	

V_{DD} = 1.8 to 2.7 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings		Unit
				min	max	
Serial clock period	SCL	t_{SCYC}		400	—	ns
SCL high-level pulse width		t_{SHW}		150	—	
SCL low-level pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	
CS to CSL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	

Notes: 1. The input signal rise and fall times (t_r, t_f) are stipulated to be under 15 ns.
2. All timings are stipulated to be referenced to 20% and 80% of V_{DD}.

• Display Control Output Timing

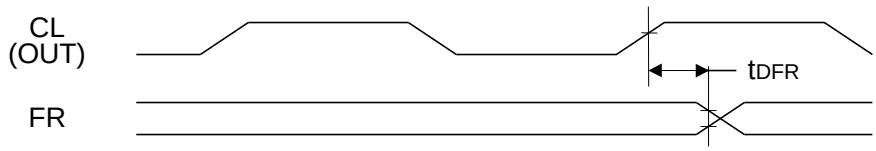


Figure 13

V_{DD} = 2.7 to 3.6 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings			Unit
				min	typ	max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	20	80	ns

V_{DD} = 1.8 to 2.7 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings			Unit
				min	typ	max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	50	200	ns

Notes: 1. Only valid in master operation mode.
2. All timings are stipulated to be referenced to 20% and 80% of V_{DD}.

• Reset

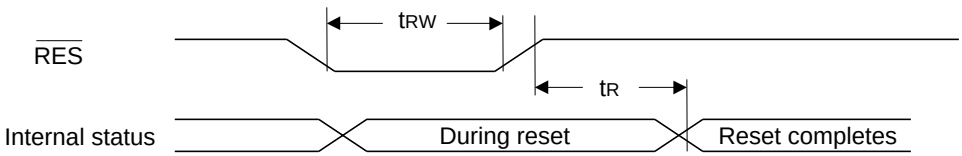


Figure 14

V_{DD} = 2.7 to 3.6 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings			Unit
				min	typ	max	
Reset time		t_R		—	—	1	µs
Reset low-level pulse width	RES	t_{RW}		1	—	—	µs

V_{DD} = 1.8 to 2.7 V, Ta = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Ratings			Unit
				min	typ	max	
Reset time		t_R		—	—	1.5	µs
Reset low-level pulse width	RES	t_{RW}		1.5	—	—	µs

Note: All timings are stipulated to be referenced to 20% and 80% of V_{DD}.

Connection Between LCD Drivers

Connection Between LCD Drivers (For reference purposes)

The LC73101C allows the LCD display area to be increased easily by using multiple LC73101C chips.

Connect the LC73101C chips as shown in figure 15.

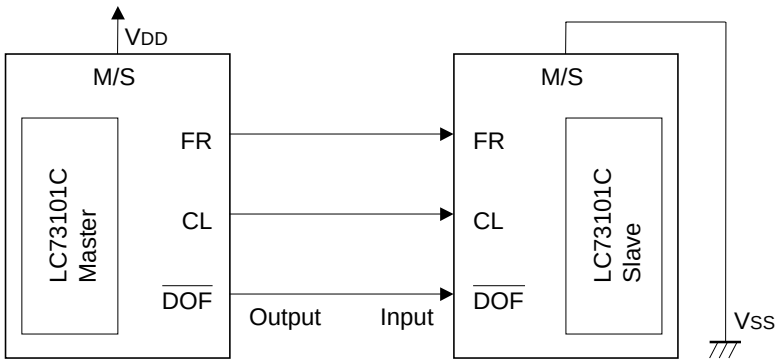


Figure 15