



# LC723732/40/48/56/64

## ETR Microcontrollers

### Overview

The LC723700 Series are large-capacity ETR microcontrollers that achieve an instruction execution time of 1.33  $\mu$ s and provide up to 64 KB of ROM and up to 2 KB of RAM. They include an on-chip high-performance PLL circuit that features an added high-speed lock circuit and can control the C/N characteristics of a local oscillator. They also provide a rich set of on-chip interface circuits, including a 3-channel serial I/O port, and an 8-input 8-bit A/D converter.

### Functions

- ROM
    - Up to 32K steps ( $32,767 \times 16$  bits)
    - The subroutine area holds 4 K steps ( $4,096 \times 16$  bits)
  - RAM
    - Up to 4 K  $\times$  4 bits (In banks 00 through 3F)
      - LC723732 – ROM: 32 KB, RAM 1 KB
      - LC723740 – ROM: 40 KB, RAM 2 KB
      - LC723748 – ROM: 48 KB, RAM 2 KB
      - LC723756 – ROM: 56 KB, RAM 2 KB
      - LC723764 – ROM: 64 KB, RAM 2 KB
  - Stack
    - 32 levels
  - Serial I/O
    - Three channels. These circuits can support both 2-wire and 3-wire 8-bit communication techniques, and can be switched between MSB first and LSB first operation.
    - One of six internally generated serial transfer clock rates can be selected: 12.5, 37.5, 187.5, 281.25, 375, and 450 kHz.
  - External interrupts
    - Seven interrupt inputs (pins INT0 through INT5, and the HOLD pin)
 

These interrupts can be set to switch between rising and falling edges, although the HOLD pin only supports falling edge detection.
  - Internal interrupts
    - Seven interrupts; four internal timer interrupts, and three serial I/O interrupts.
  - Interrupt nesting levels
    - 16 levels
    - Interrupt are prioritized in hardware as follows:
- HOLD pin > INT0 pin > INT1 pin > INT2 pin > INT3 pin > INT4 pin > INT5 pin > S-I/O0 > S-I/O1 > S-I/O2 > internal TMR0 > internal TMR1 > internal TMR2 > internal TMR3
- A/D converter
    - 8-bit resolution and 8 inputs
  - General-purpose ports
    - Input ports: 12
    - Output ports : 4
    - I/O ports: 62 (These pins can be switched between input and output in 1-bit units.)
  - PLL block
    - Includes a sub-charge pump for high-speed locking.
    - Supports dead zone control.
    - Built-in unlock detection circuit.
    - Twelve reference frequencies: 1, 3, 3.125, 5, 6.25, 9, 10, 12.5, 25, 30, 50, and 100 kHz.
    - A second PLL circuit is also included for use in AM up conversion.
  - Universal counter
    - This 20-bit counter can be used for either frequency or period measurement and supports four measurement (calculation) periods: 1, 4, 8, and 32 ms.
  - Timers
    - Two fixed timers and two programmable timers (8-bit counters)
      - TMR0: Supports four periods: 10  $\mu$ s, 100  $\mu$ s, 1 ms, and 5 ms
      - TMR1: Supports four periods: 10  $\mu$ s, 100  $\mu$ s, 1 ms, and 10 ms
      - TMR2 and TMR3: Programmable 8-bit counters. Input clocks with 10  $\mu$ s, 100  $\mu$ s, and 1 ms periods are provided.
    - One 125-ms timer flip-flop provided.
  - Beep circuit
    - Provides 12 fixed beep tones: 0.5, 1, 2, 2.08, 2.2, 2.5, 3.33, 3.75, 4.17, and 7.03 kHz.
    - Programmable 8-bit beep tone generator. Reference clocks with frequencies of 5 kHz, 15 kHz, and 50 kHz are provided.
  - Reset
    - Built-in voltage detection reset circuit
    - External reset pin

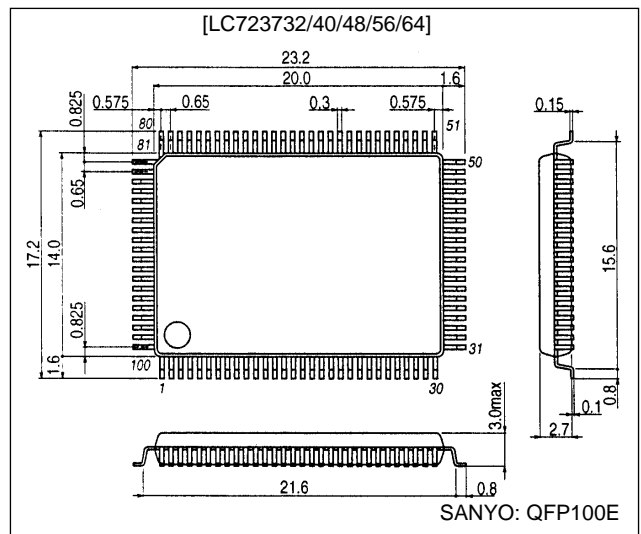
- Cycle time
  - 1.33  $\mu$ s (All instructions are one word.)
- Halt mode
  - The microcontroller operating clock is stopped in halt mode.

There are four conditions that can clear halt mode: an interrupt request, a timer flip-flop overflow, a PA port input, or a HOLD pin input.
- Operating supply voltage
  - 4.5 to 5.5 V (Microcontroller block only: 3.5 to 5.5 V)
- Package
  - QIP100E
- OTP version
  - LC72P3700
- Development tools
  - Emulator :RE32N
  - Evaluation chip: LC72EV3700
  - Evaluation chip board: EB-72EV3700

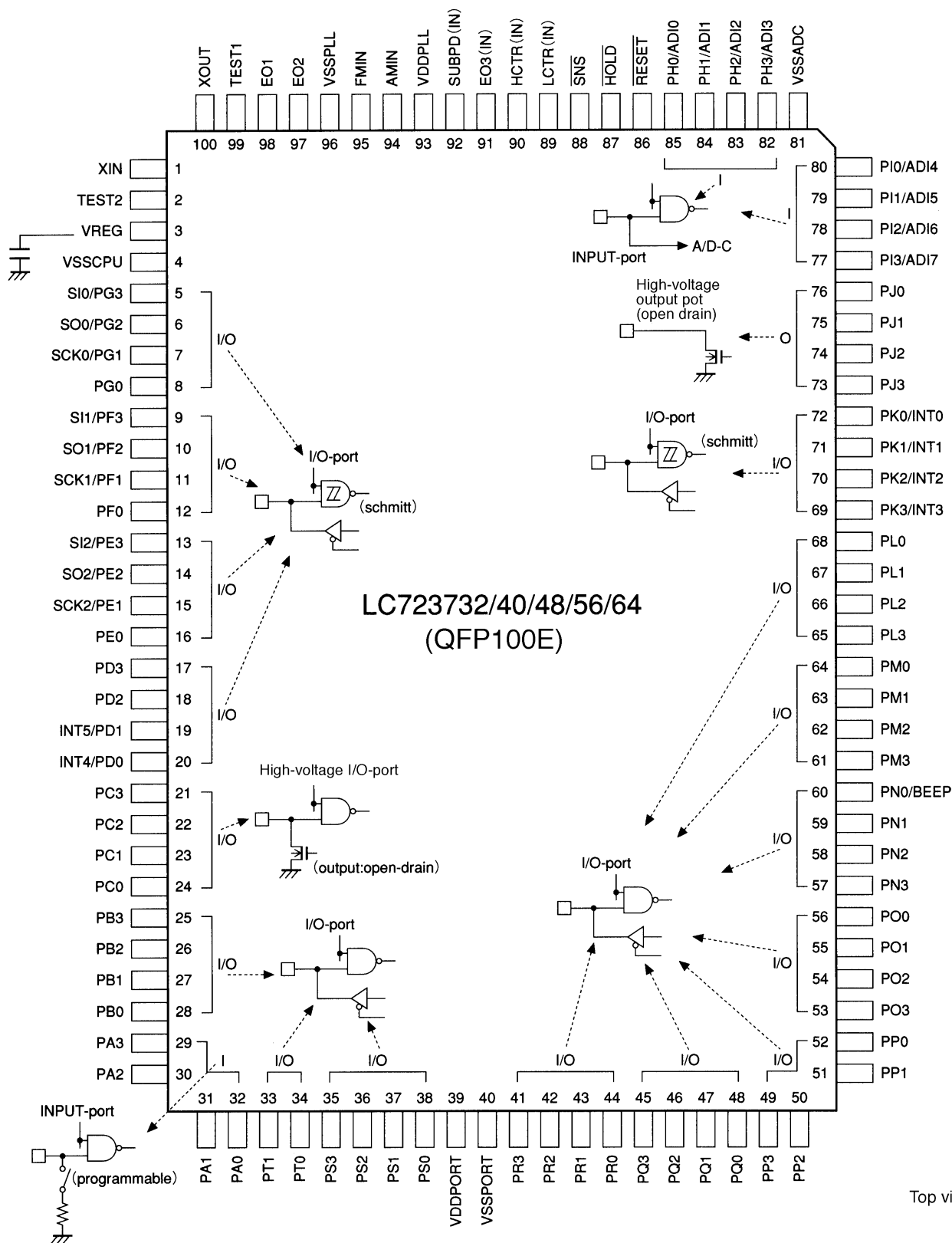
## Package Dimensions

unit: mm

### 3151-QFP100E



# Pin Assignment



A10892



## Specifications

### Electrical Characteristics

**Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$**

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	$V_{IN1}$	PC-PORT	-0.3 to +15	V
	$V_{IN2}$	All input pins other than $V_{IN1}$	-0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_{OUT1}$	PC, PJ-PORT	-0.3 to +15	V
	$V_{OUT2}$	All output pins other than $V_{OUT1}$	-0.3 to $V_{DD} + 0.3$	V
Output current	$I_{OUT1}$	PC, PJ-PORT	0 to +5	mA
	$I_{OUT2}$	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT, PT-PORT, EO1, EO2, EO3, SUBPD	0 to +3	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a = -40\text{ to }+85^\circ\text{C}$	400	mW
Operating temperature	Topg		-40 to +85	$^\circ\text{C}$
Storage temperature	Tstg		-45 to +125	$^\circ\text{C}$

**Allowable Operating Ranges at  $T_a = -40\text{ to }+85^\circ\text{C}$ ,  $V_{DD} = 3.5\text{ to }5.5\text{ V}$**

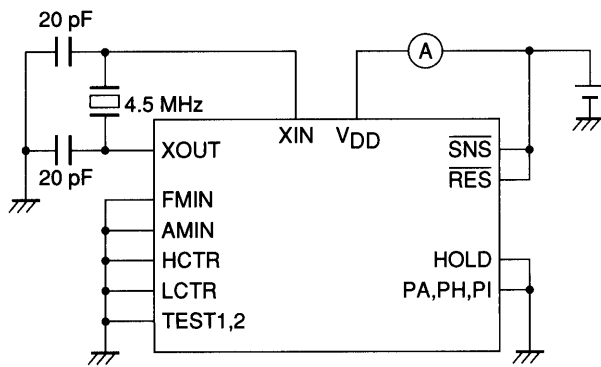
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD1}$	CPU and PLL operating	4.5	5.0	5.5	V
	$V_{DD2}$	CPU operating	3.5		5.5	V
	$V_{DD3}$	Memory retention	1.3		5.5	V
Input high-level voltage	$V_{IH1}$	PB, PC, PH, PI, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, HCTR, LCTR, EO3, SUBPD (with the I/O ports set to input mode.)	$0.7 V_{DD}$		$V_{DD}$	V
	$V_{IH2}$	PD, PE, PF, PG, PK-PORT, LCTR, _____ (in period measurement mode), HOLD, RESET	$0.8 V_{DD}$		$V_{DD}$	V
	$V_{IH3}$	$\overline{SNS}$	2.5		$V_{DD}$	V
	$V_{IH4}$	PA-PORT	$0.6 V_{DD}$		$V_{DD}$	V
Input low-level voltage	$V_{IL1}$	PB, PC, PH, PI, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, HCTR, LCTR, EO3, SUBPD (with the I/O ports set to input mode.)	0		$0.3 V_{DD}$	V
	$V_{IL2}$	PA, PD, PE, PF, PG, PK-PORT, LCTR (in period measurement mode), RESET	0		$0.2 V_{DD}$	V
	$V_{IL3}$	$\overline{SNS}$	0		1.3	V
	$V_{IL4}$	$\overline{HOLD}$	0		$0.4 V_{DD}$	V
Input frequency	$f_{IN1}$	XIN	4.0	4.5	5.0	MHz
	$f_{IN2}$	FMIN $V_{IN2}$ , $V_{DD1}$	10		150	MHz
	$f_{IN3}$	FMIN $V_{IN3}$ , $V_{DD1}$	10		130	MHz
	$f_{IN4}$	AMIN(H) $V_{IN3}$ , $V_{DD1}$	2.0		40	MHz
	$f_{IN5}$	AMIN(L) $V_{IN3}$ , $V_{DD1}$	0.5		10	MHz
	$f_{IN6}$	HCTR $V_{IN3}$ , $V_{DD1}$	0.4		12	MHz
	$f_{IN7}$	LCTR $V_{IN3}$ , $V_{DD1}$	100		500	kHz
	$f_{IN8}$	LCTR(period measurement) $V_{IH2}$ , $V_{IL2}$ , $V_{DD1}$	1		$20 \times 10^3$	Hz
Input amplitude	$V_{IN1}$	XIN	0.5		1.5	Vrms
	$V_{IN2}$	FMIN	0.07		1.5	Vrms
	$V_{IN3}$	FMIN, AMIN, HCTR, LCTR	0.04		1.5	Vrms
Input voltage range	$V_{IN4}$	ADI0 to ADI7	0		$V_{DD}$	V

# Electrical Characteristics in the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I <sub>IH1</sub>	XIN: V <sub>I</sub> = V <sub>DD</sub> = 5.0 V	2.0	5.0	15	μA
	I <sub>IH2</sub>	FMIN, AMIN, HCTR, LCTR: V <sub>I</sub> = V <sub>DD</sub> = 5.0 V	4.0	10	30	μA
	I <sub>IH3</sub>	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{\text{SNS}}$ , HOLD, $\overline{\text{RESET}}$ , HCTR, LCTR, E03, SUBPD: V <sub>I</sub> = V <sub>DD</sub> = 5.0 V (With the port PA pull-down resistors disabled, and PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT ports set to input mode.)			3.0	μA
	I <sub>IH4</sub>	Port PA (pull-down resistors enabled): V <sub>I</sub> = V <sub>DD</sub> = 5.0 V		50		μA
Input low-level current	I <sub>IL1</sub>	XIN: V <sub>I</sub> = V <sub>SS</sub>	2.0	5.0	15	μA
	I <sub>IL2</sub>	FMIN, AMIN, HCTR, LCTR: V <sub>I</sub> = V <sub>SS</sub>	4.0	10	30	μA
	I <sub>IL3</sub>	PA, PB, PC, PD, PE, PF, PG, PH, PI, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT, $\overline{\text{SNS}}$ , HOLD, $\overline{\text{RESET}}$ , HCTR, LCTR, E03, SUBPD: V <sub>I</sub> = V <sub>SS</sub> (With the port PA pull-down resistors disabled, and PB, PC, PD, PE, PF, PG, PK, PL, PM, PN, PP, PO, PQ, PR, PS, and PT ports set to input mode.)			3.0	μA
Input floating voltage	V <sub>IF</sub>	Port PA (pull-down resistors enabled)			0.05 V <sub>DD</sub>	V
Hysteresis	V <sub>H</sub>	PD, PE, PF, PG, PK-PORT, $\overline{\text{RESET}}$ , LCTR(in period measurement mode)	0.1 V <sub>DD</sub>	0.2 V <sub>DD</sub>		V
Output high-level voltage	V <sub>OH1</sub>	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT: I <sub>O</sub> = -1 mA	V <sub>DD</sub> - 1.0			V
	V <sub>OH2</sub>	E01, E02, E03, SUBPD: I <sub>O</sub> = -500 μA	V <sub>DD</sub> - 1.0			V
	V <sub>OH3</sub>	XOUT: I <sub>O</sub> = -200 μA	V <sub>DD</sub> - 1.0			V
Output low-level voltage	V <sub>OL1</sub>	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT: I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL2</sub>	E01, E02, E03, SUBPD: I <sub>O</sub> = 500 μA			1.0	V
	V <sub>OL3</sub>	XOUT: I <sub>O</sub> = 200 μA			1.5	V
	V <sub>OL4</sub>	PC, PJ-PORT: I <sub>O</sub> = 5 mA			2.0	V
Output off leakage current	I <sub>OFF1</sub>	PB, PD, PE, PF, PG, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT-PORT	-3.0		3.0	μA
	I <sub>OFF2</sub>	E01, E02, E03, SUBPD	-100		100	nA
	I <sub>OFF3</sub>	PC, PJ-PORT	-5.0		5.0	μA
A/D conversion error		ADI0 to ADI7 V <sub>DD1</sub>	-1.5		1.5	LSB
Rejected pulse width	P <sub>REJ</sub>	$\overline{\text{SNS}}$			50	μsec
Power down detection voltage	V <sub>DET</sub>		2.6	3.0	3.4	V
Pull-down resistance	R <sub>PD1</sub>	Port PA (pull-down resistors enabled): V <sub>DD</sub> = 5 V	75	100	200	kΩ
	R <sub>PD2</sub>	TEST1, TEST2		10		kΩ
Current drain	I <sub>DD1</sub>	During normal operation (PLL operating) V <sub>DD1</sub> , f <sub>IN2</sub> = 130 MHz Ta = 25°C		20	30	mA
	I <sub>DD2</sub>	Halt mode (CPU operation stopped, crystal oscillator operating) (See figure 1.) V <sub>DD2</sub> , Ta = 25°C*		0.45		mA
	I <sub>DD3</sub>	Backup mode (crystal oscillator stopped) (See figure 2.) V <sub>DD</sub> = 5.5 V, Ta = 25°C			5	μA
	I <sub>DD4</sub>	Backup mode (crystal oscillator stopped) (See figure 2.) V <sub>DD</sub> = 2.5 V, Ta = 25°C			1	μA

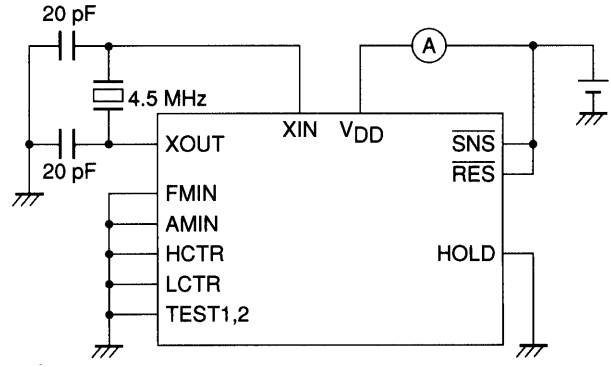
Note \*: Twenty instruction steps are executed every millisecond. The PLL, universal counter, and other functions are stopped.

## Test Circuits



A10894

Note: Ports PB through PG, and PJ through PT are all left open.  
However, ports PB through PG, PK through PT, EO3, and SUBPD are left open in output mode.



A10895

Note: Ports PA through PT are all left open.

Figure 1 IDD2 in Halt Mode

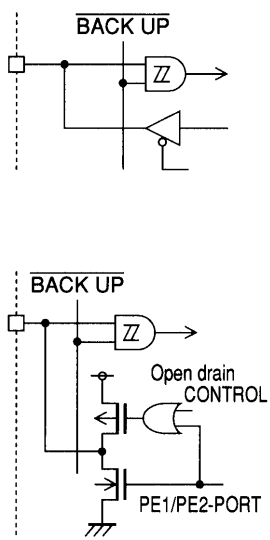
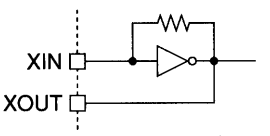
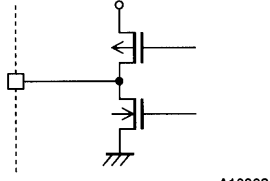
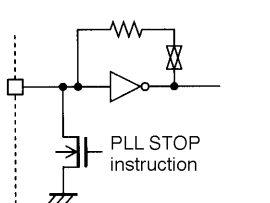
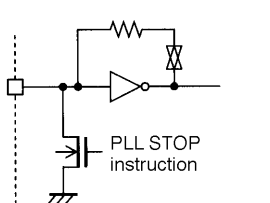
Figure 2 IDD3 and IDD4 in Backup Mode

## Pin Descriptions

Pin No.	Symbol	I/O	Function	Equivalent circuit
32 31 30 29	PA0 PA1 PA2 PA3	I	Dedicated input ports. These ports are designed with a low threshold voltage. The pull-down resistors for all four pins are set up together with an IOS1 instruction. The pull-down resistors cannot be set individually. Input is disabled in backup mode.	<p>BACK UP</p> <p>Programmable</p> <p>A10896</p>
28 27 26 25	PB0 PB1 PB2 PB3	I/O	General-purpose I/O ports The mode (input or output) is set using the IOS2 instruction. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	<p>BACK UP</p> <p>A10897</p>
24 23 22 21	PC0 PC1 PC2 PC3	I/O	General-purpose I/O ports (high-voltage input and output) The mode (input or output) is set using the IOS2 instruction. External pull-up resistors are required since the output circuits are open drain circuits. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	<p>BACK UP</p> <p>A10898</p>
20 19 18 17	PD0/INT4 PD1/INT5 PD2 PD3	I/O	General-purpose I/O and external interrupt shared function ports The input formats are Schmitt inputs. The external interrupt function is enabled when the external interrupt enable flag is set. • When used as general-purpose I/O ports: The mode (input or output) is set in 1-bit units using the IOS2 instruction. • When used as external interrupt pins: The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT4EN or INT5EN). Here, the pins must be set to input mode in advance. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	<p>BACK UP</p> <p>A10899</p>

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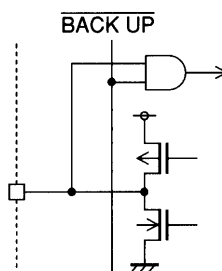
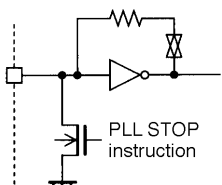
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Pin No.	Symbol	I/O	Function	Equivalent circuit									
16 15 14 13 12 11 10 9 8 7 6 5	PE0 PE1/SCK2 PE2/SO2 PE3/SI2 PF0 PF1/SCK1 PF2/SO1 PF3/SI1 PG0 PG1/SCK0 PG2/SO0 PG3/SI0	I/O	<p>General-purpose I/O ports with shared functions as serial I/O ports The input formats are Schmitt inputs. The PE1/SCK2 and PE2/SO2 pins can be switched to function as open drain outputs. The IOS1 instruction is used to switch between the general-purpose I/O port and serial I/O port functions.</p> <ul style="list-style-type: none"><li>When used as general-purpose I/O ports: The pins are set to the general-purpose I/O port function using the IOS1 instruction. The mode (input or output) is set in 1-bit units using the IOS1 instruction.</li><li>When used as serial I/O ports: The pins are set to the serial I/O port function using the IOS1 instruction. [Pin states when set to the serial I/O port function] PE0, PF0, PG0 ... General-purpose I/O PE1, PF1, PG1 ... SCK input or output PE2, PF2, PG2 ... SO output PE3, PF3, PG3 ... SI input</li></ul> <p>The PE1/SCK2 and PE2/SO2 pins can be switched to function as open drain outputs with the IOS2 instruction. When using this circuit type, the external pull-up resistors must be connected to the same power supply as that used by the IC. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.</p>	 <p>BACK UP</p> <p>Open drain CONTROL</p> <p>PE1/PE2-PORT</p> <p>A10900</p>									
1 100	XIN XOUT	I O	Connections for a 4.5-MHz crystal oscillator element	 <p>XIN</p> <p>XOUT</p> <p>A10901</p>									
98 97	E01 E02	O	<p>Main charge pump outputs These pins output a high level when the frequency of the local oscillator divided by n is higher than that of the reference frequency, and they output a low level when that frequency is lower. They go to the high-impedance state when the frequencies match. These pins go to the high-impedance state in backup mode, after a power on reset, and in the PLL stopped state.</p>	 <p>A10902</p>									
39 93 4 40 81 96	V <sub>DD</sub> PORT V <sub>DD</sub> PLL V <sub>SS</sub> CPU V <sub>SS</sub> PORT V <sub>SS</sub> ADC V <sub>SS</sub> PLL	—	<p>Power supply connections The V<sub>DD</sub>PORT and V<sub>SS</sub>PORT pins mainly supply power for the peripheral I/O blocks and the regulator. The V<sub>DD</sub>PLL and V<sub>SS</sub>PLL pins mainly for the PLL circuits. The V<sub>SS</sub>CPU pin is mainly used by the CPU block. The V<sub>SS</sub>ADC pin is mainly used by the A/D converter block. Since all the V<sub>DD</sub> and V<sub>SS</sub> pins are independent, all must be connected to the same power supply.</p>										
3	V <sub>REG</sub>	O	<p>Internal low voltage output Connect a bypass capacitor to this pin.</p>										
95	FM <sub>IN</sub>	I	<p>FM VCO (local oscillator) input This pin is selected with CW1 in the PLL instruction. The signal input to this pin must be capacitor coupled. Input is disabled in backup mode, after a power on reset, and in the PLL stopped state.</p>	 <p>PLL STOP instruction</p> <p>A10903</p>									
94	AM <sub>IN</sub>	I	<p>AM VCO (local oscillator) input This pin is selected and the band set with CW1 (b1, b0) in the PLL instruction.</p> <table border="1"><thead><tr><th>b1</th><th>b0</th><th>Band</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>2 to 40 MHz (SW)</td></tr><tr><td>1</td><td>1</td><td>0.5 to 10 MHz (MW, LW)</td></tr></tbody></table> <p>The signal input to this pin must be capacitor coupled. Input is disabled in backup mode, after a power on reset, and in the PLL stopped state.</p>	b1	b0	Band	1	0	2 to 40 MHz (SW)	1	1	0.5 to 10 MHz (MW, LW)	 <p>PLL STOP instruction</p> <p>A10903</p>
b1	b0	Band											
1	0	2 to 40 MHz (SW)											
1	1	0.5 to 10 MHz (MW, LW)											

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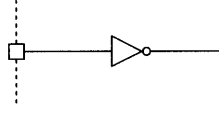
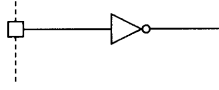
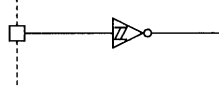
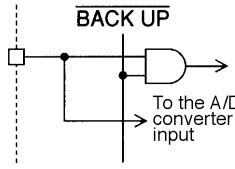
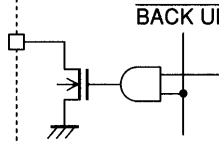
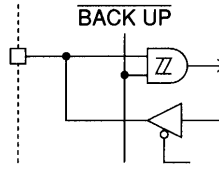


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Pin No.	Symbol	I/O	Function	Equivalent circuit															
92	SUBPD	I/O	<p>Sub-charge pump output and general-purpose input shared function port The IOS2 instruction is used for switching between the sub-charge pump output and general-purpose input functions.</p> <ul style="list-style-type: none"><li>When used as the sub-charge pump output: The sub-charge pump output function is set up with the IOS2 instruction. A high-speed locking circuit can be formed by using this pin in conjunction with the main charge pump. The sub-charge pump is controlled using the DZC instruction.</li></ul> <table><tr><th>b3</th><th>b2</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>High impedance</td></tr><tr><td>0</td><td>1</td><td>Only operates when the PLL is unlocked (450 kHz)</td></tr><tr><td>1</td><td>0</td><td>Only operates when the PLL is unlocked (900 kHz)</td></tr><tr><td>1</td><td>1</td><td>Normal operation</td></tr></table> <ul style="list-style-type: none"><li>When used as a general-purpose input: The general-purpose input function is set up with the IOS2 instruction. Data is read from the port using the INR instruction. This pin goes to the high-impedance state in backup mode, after a power on reset, and in the PLL stopped state.</li></ul>	b3	b2	Operation	0	0	High impedance	0	1	Only operates when the PLL is unlocked (450 kHz)	1	0	Only operates when the PLL is unlocked (900 kHz)	1	1	Normal operation	 <p>A10904</p>
b3	b2	Operation																	
0	0	High impedance																	
0	1	Only operates when the PLL is unlocked (450 kHz)																	
1	0	Only operates when the PLL is unlocked (900 kHz)																	
1	1	Normal operation																	
91	E03	I/O	<p>Second PLL charge pump output and general-purpose input shared function port The IOS2 instruction is used for switching between the second PLL charge pump output and general-purpose input functions.</p> <ul style="list-style-type: none"><li>When used as a charge pump output: The charge pump output function is set up with the IOS2 instruction. This pin outputs a low level when the frequency of the local oscillator divided by n is higher than that of the reference frequency, and it outputs a high level when that frequency is lower. It goes to the high-impedance state when the frequencies match. (Note that the logic of this pin is inverted from that of the EO1 and EO2 pins.)</li><li>When used as a general-purpose input: The general-purpose input function is set up with the IOS2 instruction. Data is read from the port using the INR instruction. This pin goes to the high-impedance state in backup mode, after a power on reset, and in the PLL stopped state.</li></ul>																
90	HCTR	I	<p>Universal counter and general-purpose input shared function input port The IOS1 instruction is used for switching between the universal counter and general-purpose input functions.</p> <ul style="list-style-type: none"><li>When used for frequency measurement: The universal counter function is set up with the IOS1 instruction. The counter is controlled using the UCS and UCC instructions. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling.</li><li>When used as a general-purpose input pin: The general-purpose input function is set up with the IOS1 instruction. Data is read from the port using the INR (b0) instruction. Input is disabled in backup mode. (The input pin will be pulled down.) The universal counter function is selected after a power on reset.</li></ul>																
89	LCTR	I	<p>Universal counter (frequency or period measurement) and general-purpose input shared function input port The IOS1 instruction is used for switching between the universal counter and general-purpose input functions.</p> <ul style="list-style-type: none"><li>When used for frequency measurement: The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since this pin functions as an AC amplifier in this mode, the input signal must be input with capacitor coupling.</li><li>When used for period measurement: The universal counter function is set up with the IOS1 instruction. Set up LCTR frequency measurement mode with the UCS instruction, and control operation with the UCC instruction. Since the bias feedback resistor is disconnected in this mode, the input signal must be input with DC coupling.</li><li>When used as a general-purpose input pin: The general-purpose input port function is set up with the IOS1 instruction. Data is read from the port using the INR (b1) instruction. Input is disabled in backup mode. (The input pin will be pulled down.) The universal counter function (HCTR frequency measurement mode) is selected after a power on reset.</li></ul>	 <p>A10905</p>															

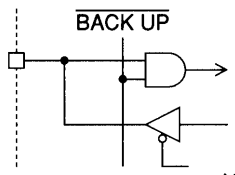
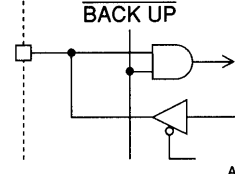
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Pin No.	Symbol	I/O	Function	Equivalent circuit
88	SNS	I	<p>Voltage sense and general-purpose input shared function port This input circuit is designed with a low input threshold voltage.</p> <ul style="list-style-type: none"> <li>When used as a voltage sense input: This pin is used to test for power failures on the return from backup mode. Application can test this condition using the internal SNS flip-flop. The SNS flip-flop can be tested with the TST instruction. (This usage requires external components (capacitors and resistors). See the sample application circuit in the user's manual.)</li> <li>When used as a general-purpose input port: When used as a general-purpose input port the pin state can be tested with the TST instruction.</li> </ul> <p>Unlike the other input ports, input to this pin is not disabled in backup mode and after a power on reset. As a result, through currents must be taken into account when designing applications that use this pin as a general-purpose input.</p>	 <p>A10906</p>
87	HOLD	I	<p>Power supply monitor (with interrupt function) This pin is designed with a high input threshold voltage.</p> <p>This pin is normally connected to the ACC line and used for power off detection. When a power off state is detected, the HOLDON flag and the hold interrupt request flag will be set. To enter backup mode, execute a CKSTP instruction when the HOLD pin is low. Set this pin high to clear backup mode.</p>	 <p>A10907</p>
86	RESET	I	<p>System reset pin When the CPU is operating or in halt mode, the system is reset when this pin is held low for at least one machine cycle. Execution starts with the PC pointing to location 0. At this time the SNS flip-flop is set. A low level must be applied for at least 50 ms when power is first applied.</p>	 <p>A10908</p>
85 84 83 82 81 80 79 78	PH0/ADI0 PH1/ADI1 PH2/ADI2 PH3/ADI3 PI0/ADI4 PI1/ADI5 PI2/ADI6 PI3/ADI7	I	<p>General-purpose input and A/D converter input shared function ports The IOS1 instruction is used to switch between the general-purpose input and the A/D converter input functions.</p> <ul style="list-style-type: none"> <li>When used as a general-purpose input ports: The general-purpose input port function is set up with the IOS1 instruction. (In bit units)</li> <li>When used as A/D converter input pins: The A/D converter input port function is set up with the IOS1 instruction. (In bit units)</li> </ul> <p>The pin whose voltage is to be converted is specified with the IOS1 instruction, and the conversion is started with the UCC instruction.</p> <p>Note: Since input is disabled for ports specified for the ADI function, executing an input instruction for such a port will always return a low level.</p> <p>Input is disabled in backup mode. These ports are set up as general-purpose input ports after a power on reset.</p>	 <p>A10909</p>
76 75 74 73	PJ0 PJ1 PJ2 PJ3	O	<p>General-purpose output ports Since these are open-drain output circuits, external pull-up resistors are required.</p> <p>The internal transistors are turned off (resulting in a high-level output) in backup mode and after a power on reset.</p>	 <p>A10910</p>
72 71 70 69	PK0/INT0 PK1/INT1 PK2/INT2 PK3/INT3	I/O	<p>General-purpose I/O and external interrupt shared function ports The input formats are Schmitt inputs.</p> <p>The external interrupt function is enabled when the external interrupt enable flag is set.</p> <ul style="list-style-type: none"> <li>When used as general-purpose I/O ports: The mode (input or output) is set in 1-bit units using the IOS1 instruction.</li> <li>When used as external interrupt pins: The external interrupt functions are enabled by setting the corresponding external interrupt enable flag (INT0EN through INT3EN). Here, the pins must be set to input mode in advance.</li> </ul> <p>Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.</p>	 <p>A10911</p>

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Pin No.	Symbol	I/O	Function	Equivalent circuit
68 to 61	PL0 to 3 PN0 to 3	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	 <p>A10912</p>
60 59 58 57	PN0/BEEP PN1 PN2 PN3	I/O	General-purpose I/O port and beep tone output shared function ports The IOS2 instruction is used to switch between the general-purpose I/O port and the beep tone output functions. <ul style="list-style-type: none"> <li>When used as a general-purpose input ports: The general-purpose I/O port function is set up with the IOS2 instruction. (Pins PN1 through PN3 are general-purpose I/O pins.)</li> <li>When used as the beep tone output pin: The beep tone output function is set up with the IOS2 instruction. The frequency is set with the BEEP instruction. When this pin is used as the beep tone output pin, executing an output instruction for this pin only sets the internal latch and has no influence on the output. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.</li> </ul>	
56 to 49	P00 to 3 PP0 to 3	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	
48 to 41 38 to 33	PQ0 to 3 PR0 to 3 PS0 to 3 PT0 to 1	I/O	General-purpose I/O ports The mode is switched between input and output with the IOS instruction, and data is input with the INR instruction and output with the OUTF instruction. The SPB, RPB, TPT, and TPF instruction cannot be used with these ports. Input is disabled and the pins go to the high-impedance state in backup mode. These ports are set up as general-purpose input ports after a power on reset.	 <p>A10913</p>
99 2	TEST1 TEST2		IC test pins These pins must be tied to ground.	

## LC723700 Instruction Set

## Abbreviations

ADDR:	Program memory address
b:	Borrow
c:	Carry
DH:	Data memory address High (Row address) [2 bits]
DL:	Data memory address Low (Column address) [4 bits]
I:	Immediate data [4 bits]
M:	Data memory address
N:	Bit position [4 bits]
M <sub>ADR</sub> :	M specified by address register
ROM <sub>ADR</sub> :	Program memory data specified by address register
P1n, P2n:	Port number [4 bits]
PW1n, PW2n:	Port control word number [4 bits]
PEn:	Peripheral register number [4 bits]
SR:	ADR/DTR
ADR:	Address register
DTR:	Data register
r:	General register (One of the address from 00H to 0FH of BANK0)
SWR:	Status write register
SRR:	Status read register
( ), [ ]:	Contents of register or memory
M(DH, DL):	Data memory specified by DH, DL

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format														
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1
Addition instructions	AD	r	M	Add M to r	$r \leftarrow (r) + (M)$	0	1	0	0	0	0	DH		DL						r
	ADS	r	M	ADD M to r, then skip if carry	$r \leftarrow (r) + (M)$ , skip carry	0	1	0	0	0	1	DH		DL						r
	AC	r	M	Add M to r with carry	$r \leftarrow (r) + (M) + C$	0	1	0	0	1	0	DH		DL					r	
	ACS	r	M	Add M to r with carry, then skip if carry	$r \leftarrow (r) + (M) + C$ skip if carry	0	1	0	0	1	1	DH		DL					r	
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	DH		DL					I	
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$ , skip if carry	0	1	0	1	0	1	DH		DL					I	
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	DH		DL					I	
	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$ , skip if carry	0	1	0	1	1	1	DH		DL					I	
Subtraction instructions	SU	r	M	Subtract M from r	$r \leftarrow (r) - (M)$	0	1	1	0	0	0	DH		DL					r	
	SUS	r	M	Subtract M from r, then skip if borrow	$r \leftarrow (r) - (M)$ , skip if borrow	0	1	1	0	0	1	DH		DL					r	
	SB	r	M	Subtract M from r with borrow	$r \leftarrow (r) - (M) - b$	0	1	1	0	1	0	DH		DL					r	
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$r \leftarrow (r) - (M) - b$ , skip if borrow	0	1	1	0	1	1	DH		DL					r	
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	DH		DL					I	
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$ , skip if borrow	0	1	1	1	0	1	DH		DL					I	
	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	DH		DL					I	
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$ , skip if borrow	0	1	1	1	1	1	DH		DL					I	
Comparison instructions	SEQ	r	M	Skip if r equal to M	$(r) - (M)$ , skip if zero	0	0	0	1	0	0	DH		DL					r	
	SEQI	M	I	Skip if M equal to I	$(M) - I$ , skip if zero	0	0	0	1	0	1	DH		DL					I	
	SNEI	M	I	Skip if M not equal to I	$(M) - I$ , skip if not zero	0	0	0	0	0	1	DH		DL					I	
	SGE	r	M	Skip if r is greater than or equal to M	$(r) - (M)$ , skip if not borrow	0	0	0	1	1	0	DH		DL					r	
	SLE	r	M	Skip if r is less than M	$(r) - M$ , skip if borrow	0	0	0	0	1	0	DH		DL					r	
	SGEI	M	I	Skip if M is greater than or equal to I	$(M) - I$ , skip if not borrow	0	0	0	1	1	1	DH		DL					I	
	SLEI	M	I	Skip if M is less than I	$(M) - I$ , skip if borrow	0	0	0	0	1	1	DH		DL					I	

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Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format																	
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0		
Logical operation instructions	AND	r	M	AND M with r	$r \leftarrow (r) \text{ AND } (M)$	0	0	1	0	0	0	DH		DL		r							
	ANDI	M	I	AND I with M	$M \leftarrow (M) \text{ AND } I$	0	0	1	0	0	1	DH		DL		I							
	OR	r	M	OR M with r	$r \leftarrow (r) \text{ OR } (M)$	0	0	1	0	1	0	DH		DL		r							
	ORI	M	I	OR I with M	$M \leftarrow (M) \text{ OR } I$	0	0	1	0	1	1	DH		DL		I							
	EXL	r	M	Exclusive OR M with r	$r \leftarrow (r) \text{ XOR } (M)$	0	0	1	1	0	0	DH		DL		r							
	EXLI	M	I	Exclusive OR M with M	$M \leftarrow (M) \text{ XOR } I$	0	0	1	1	0	1	DH		DL		I							
	SHMR	M		Shift M right with carry		1	1	1	1	1	1	1	1	1	0	DH		DL					
Transfer instructions	LD	r	M	Load M to r	$r \leftarrow (M)$	1	1	0	1	0	0	DH		DL		r							
	ST	M	r	Store r to M	$M \leftarrow (r)$	1	1	0	1	0	1	DH		DL		r							
	LDA	r		Load M specified by ADR to r	$r \leftarrow (M_{\text{ADR}})$	1	1	1	1	1	0	0	1	1	1	0	r						
	STA	r		Store r to M specified by ADR	$M_{\text{ADR}} \leftarrow (r)$	1	1	1	1	1	0	0	1	1	1	0	r						
	MVRD	r	M	Move M to destination M referring to r in the same row	$[\text{DH}, m] \leftarrow (M)$	1	1	0	1	1	0	DH		DL		r							
	MVRS	M	r	Move source M referring to r to M in the same row	$M \leftarrow (\text{DH}, m)$	1	1	0	1	1	1	DH		DL		r							
	MVSR	M1	M2	Move M to M in the same row	$[\text{DH}, \text{DL1}] \leftarrow [\text{DH}, \text{DL2}]$	1	1	1	0	0	0	DH		DL		DL2							
MVI	M	I	Move I to M	$M \leftarrow I$	1	1	1	0	0	1	DH		DL		I								
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if $M(N) = \text{all } 1$ , then skip	1	1	1	1	0	0	DH		DL		N							
	TMF	M	N	Test M bits, then skip if all bits specified are false	if $M(N) = \text{all } 0$ , then skip	1	1	1	1	0	1	DH		DL		N							
Jump and subroutine instructions	JMP	ADDR		Jump to the address	$\text{PC} \leftarrow \text{ADDR}$	1	0	ADDR(14 bits)															
	JMPA			Jump to the address specified by ADR	$\text{PC} \leftarrow (\text{ADR})$	0	0	0	0	0	0	0	0	1	1	1	0						
	JMPR	ADDR		Jump to the relative address	$\text{PC} \leftarrow (\text{PC}) + 1 + \text{ADDR}$	1	1	1	1	1	0	1	0	ADDR (8 bits)									
	CAL	ADDR		Call subroutine	$\text{PC} \leftarrow \text{ADDR}$ $\text{Stack} \leftarrow (\text{PC}) + 1$	1	1	0	0	ADDR(12 bits)													
	CALA			Call subroutine specified by ADR	$\text{PC} \leftarrow (\text{ADR})$ $\text{Stack} \leftarrow (\text{PC}) + 1$	0	0	0	0	0	0	0	0	1	1	1	1						
	RT			Return from subroutine	$\text{PC} \leftarrow \text{Stack}$	0	0	0	0	0	0	0	0	1	0	0	0						
	RTS			Return from subroutine and skip	$\text{PC} \leftarrow \text{Stack} + 1$	0	0	0	0	0	0	0	0	1	0	1	0						
	RTB			Return from subroutine with BANK data	$\text{PC} \leftarrow \text{Stack}$ , $\text{BANK} \leftarrow \text{Stack}$	1	1	1	1	1	1	1	1	1	1	1	0	0					
	RTBS			Return from subroutine with BANK data and skip	$\text{PC} \leftarrow \text{Stack} + 1$ , $\text{BANK} \leftarrow \text{Stack}$	1	1	1	1	1	1	1	1	1	1	1	0	1					
	RTI			Return from interrupt	$\text{PC} \leftarrow \text{Stack}$ , $\text{BANK} \leftarrow \text{Stack}$ , $\text{CARRY} \leftarrow \text{Stack}$ $\text{PAGE} \leftarrow \text{Stack}$	0	0	0	0	0	0	0	0	1	0	0	1						
Status register instructions	SS	SWR	N	Set status register	$(\text{Status W-reg})N \leftarrow 1$	1	1	1	1	1	1	1	1	0	0	SWR		N					
	RS	SWR	N	Reset status register	$(\text{Status W-reg})N \leftarrow 0$	1	1	1	1	1	1	1	1	0	1	SWR		N					
	TST	SRR	N	Test status register true	if $(\text{Status R-reg})N = \text{all } 1$ , then skip	1	1	1	1	1	0	0	0	0	SRR		N						
	TSF	SRR	N	Test status register false	if $(\text{Status R-reg})N = \text{all } 0$ , then skip	1	1	1	1	1	0	0	0	1	SRR		N						
Internal register transfer instructions	PLL	M		Load M to PLL register	$\text{PLL reg} \leftarrow \text{PLL data}$	1	1	1	1	1	0	0	1	0	1	DH		DL					
	PUT	PE <sub>n</sub>		Put data of DTR to peripheral register	$\text{PE}_n \leftarrow (\text{DTR})$	1	1	1	1	1	0	0	1	1	0	1	PE <sub>n</sub>						
	GET	PE <sub>n</sub>		Get peripheral data to DTR	$\text{DTR} \leftarrow (\text{PE}_n)$	1	1	1	1	1	0	0	1	1	0	1	PE <sub>n</sub>						
Hardware control instructions	SIO	I1	I2	Serial I/O control	$\text{SIO reg} \leftarrow I1, I2$	0	0	0	0	0	0	0	1	I1		I2							
	UCS	I		Set I to UCCW1	$\text{UCCW1} \leftarrow I$	0	0	0	0	0	0	0	0	0	0	0	I						
	UCC	I		Set I to UCCW2	$\text{UCCW2} \leftarrow I$	0	0	0	0	0	0	0	0	0	0	1	I						
	BEEP	I		Beep control	$\text{BEEP reg} \leftarrow I$	0	0	0	0	0	0	0	0	0	1	1	I						
	DZC	I		Dead zone control	$\text{DZC reg} \leftarrow I$	0	0	0	0	0	0	0	0	1	0	1	I						
	TMS	I		Set timer register	$\text{Timer reg} \leftarrow I$	0	0	0	0	0	0	0	0	1	1	0	I						
	IOS1	PW1 <sub>n</sub>	N	Set port control word1	$\text{IOS1 reg PW1}_n \leftarrow N$	1	1	1	1	1	1	1	0	PW1 <sub>n</sub>		N							
IOS2	PW2 <sub>n</sub>	N	Set port control word2	$\text{IOS2 reg PW2}_n \leftarrow N$	1	1	1	1	1	0	1	1	PW2 <sub>n</sub>		N								

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Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format															
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
I/O instructions	IN	M	P1n	Input port1 data to M	$M \leftarrow (P1n)$	1	1	1	0	1	0	DH					DL			P1n	
	OUT	M	P1n	Output contents of M to port 1	$P1n \leftarrow M$	1	1	1	0	1	1	DH					DL			P1n	
	INR	M	P2n	Input port 2 data to M	$M \leftarrow (P2n)$	0	0	1	1	1	0	DH					DL			P2n	
	OUTR	M	P2n	Output contents of M to port 2	$P2n \leftarrow (M)$	0	0	1	1	1	1	DH					DL			P2n	
	SPB	P1n	N	Set port 1 bits	$(P1n)N \leftarrow 1$	0	0	0	0	0	0	1	0				P1n			N	
	RPB	P1n	N	Reset port 1 bits	$(P1n)N \leftarrow 0$	0	0	0	0	0	0	1	1				P1n			N	
	TPT	P1n	N	Test port 1 bits, then skip if all bits specified are true	if $(P1n)N = \text{all } 1$ , then skip	1	1	1	1	1	1	0	0				P1n			N	
	TPF	P1n	N	Test port 1 bits, then skip if all bits specified are false	if $(P1n)N = \text{all } 0$ , then skip	1	1	1	1	1	1	0	1				P1n			N	
Bank switching instructions	BANK		I	Select Bank	$BANK \leftarrow I$	1	1	1	1	1	0	0	1	0	0				I		
Table reference instructions	MVTL			Move program memory data specified by ADR to DTR	$DTR \leftarrow (ROM_{ADR})$	0	0	0	0	0	0	0	0	0	0	1					
Stack manipulation instructions	PUSH		SR	Move ADR/DTR to stack	$Stack \leftarrow (ADR/DTR)$	1	1	1	1	1	0	0	1	1	0	0			SR		
	POP		SR	Move stack to ADR/DTR	$ADR/DTR \leftarrow Stack$	1	1	1	1	1	0	0	1	1	0	0			SR		
Other instructions	PAGE		I	Set page flag	$PAGE \text{ flag} \leftarrow I$	0	0	0	0	0	0	0	0	0	1	1			I		
	HALT		I	Halt mode control	$HALT \text{ reg} \leftarrow I$ , then CPU clock stop	0	0	0	0	0	0	0	0	0	1	0			I		
	CKSTP			Clock stop	Stop xtal OSC if HOLD = 0	0	0	0	0	0	0	0	0	0	1	0					
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0					

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