Ordering number : ENN*6651

CMOS IC

LC72346W, 72347W

Ultralow-Voltage ETR Controller with On-Chip LCD Driver

Preliminary

Overview

The LC72346W and LC72347W are ultralow-voltage electronic tuning microcontrollers that include a PLL that operates up to 250 MHz and a 1/4 duty 1/2 bias LCD driver on chip. This IC includes an on-chip DC-DC converter that can easily create the power supply voltages needed for electronic tuning and contribute to reducing end product costs. This IC is optimal for portable audio equipment that must operate from a single battery.

Function

- Program memory (ROM):
  — 4096 × 16 bits (8K bytes) : LC72346
  — 6144 × 16 bits (12K bytes): LC72347
- Data memory (RAM):
  — 256 × 4 bits: LC72346
  — 512 × 4 bits: LC72347
- Cycle time:
  40 µs (all 1-word instructions) at 75kHz crystal oscillation
- Stack: 8 levels
- LCD driver: 48 to 80 segments (1/4 duty, 1/2 bias drive)
- Interrupts: Two external interrupts
  Timer interrupts (1, 5, 10, and 50 ms)
- A/D converter:
  Four input channels (6-bit successive approximation conversion)
- Input ports: 7 ports (of which three can be switched for use as A/D converter inputs)
- Output ports: 6 ports (of which 1 can be switched for use as the beep tone output and 2 are open-drain ports)
- I/O ports: 20 ports (of which 8 can be switched for use as LCD ports and as mask options, of which 3 can be switched for use as serial I/O ports)
- Serial I/O: One system (LC72347)
- PLL: Reference frequencies:
  1, 3, 3.125, 5, 6.25, 12.5, and 25 kHz
- Input frequencies: FM band: 10 to 250 MHz
  AM band (high): 2 to 20 MHz
  AM band (low): 0.5 to 10 MHz
- Input sensitivity:
  FM band: 35 mVrms (50 mVrms at 130 MHz or higher frequency)
  AM band (high, low): 35 mVrms
- External reset input: During CPU and PLL operations, instruction execution is started from location 0.
- Built-in power-on reset circuit:
  The CPU starts execution from location 0 when power is first applied.
- Halt mode: The controller-operating clock is stopped.

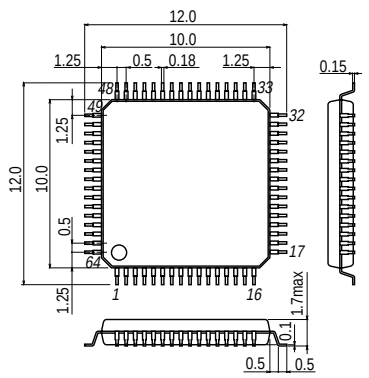
Continued on next page.

Package Dimensions

unit: mm

3190-SQFP64

[LC72346W, 72347W]



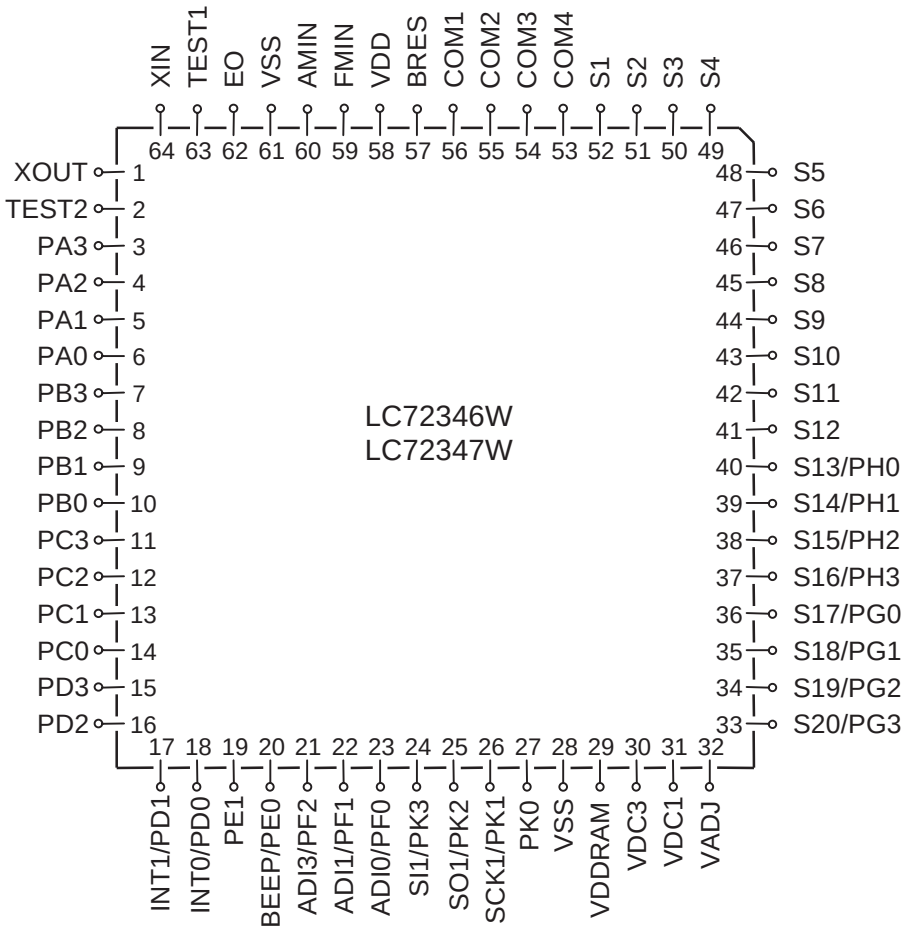
SANYO: SQFP64

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

- Backup mode: The crystal oscillator is stopped.
- Static power-on function:
  Backup state is cleared with the PF port
- Beep tone: 1.5 and 3.1 kHz
- Built-in DC-DC converter:
  For LCD and A/D converter use (3 V)
  Can also be used for TU + B creation by using a secondary coil.
- Built-in remaining battery life verification function:
  Converts the V_{DD} pin level to digital.
- Memory retention voltage: 0.5 V or higher
- Dedicated memory power supply: The RAM retention time has been increased by the provision of a dedicated memory power supply.
- Package: SQFP-64 (0.5-mm pitch)
- V_{DD} power supply: 0.9 to 1.8 V

Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}1$ max	V_{DD}	–0.3 to +3.0	V
	$V_{DD}3$ max	V_{DD}RAM	–0.3 to +4.0	V
	$V_{DD}4$ max	VDC3	–0.3 to +4.0	V
Input voltage	$V_{IN}1$	FMIN, AMIN	–0.3 to $V_{DD}1$ +0.3	V
	$V_{IN}2$	PA, PC, PD, PF, PK, PG, PH, BRES	–0.3 to $V_{DD}1$ +0.3	V
Output voltage	$V_{OUT}1$	PE	–0.3 to +7	V
	$V_{OUT}2$	PB, PC, PD, PG, PH	–0.3 to $V_{DD}1$ +0.3	V
	$V_{OUT}3$	VDC1, EO	–0.3 to $V_{DD}4$ +0.3	V
	$V_{OUT}4$	COM1 to COM4, S1 to S20	–0.3 to $V_{DD}4$ +0.3	V
Output current	$I_{OUT}1$	PC, PD, PG, PH, EO	0 to 3	mA
	$I_{OUT}2$	PB	0 to 1	mA
	$I_{OUT}3$	PE	0 to 2	mA
	$I_{OUT}4$	S1 to S20	300	µA
	$I_{OUT}5$	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –10 to +60°C	100	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –10 to +60°C, V_{DD} = 0.9 to 1.8 V

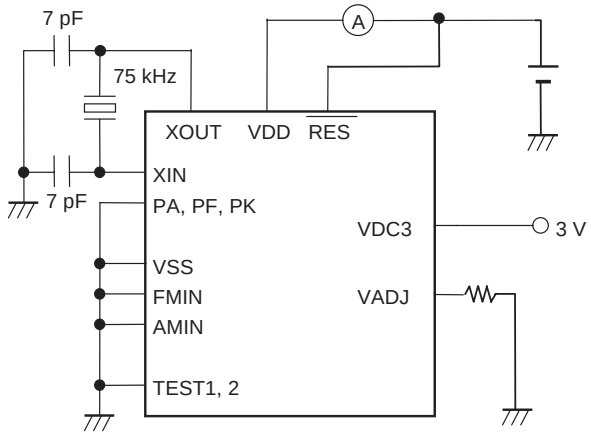
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	Voltage applied to the V_{DD} pin	0.9	1.3	1.8	V
	$V_{DD}3$	Voltage applied to the V_{DD}RAM pin	2.7	3.0	3.3	
	$V_{DD}4$	Voltage applied to the VDC3 pin	2.7	3.0	3.3	
	$V_{DD}5$	Memory retention voltage	0.5			
Input high-level voltage	$V_{IH}1$	Ports PC, PD, PG, PH, and PK	0.7 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}2$	Port PA	0.8 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}3$	Port PF	0.8 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}4$	Port BRES	0.6 $V_{DD}1$		$V_{DD}1$	V
Input low-level voltage	$V_{IL}1$	Ports PC, PD, PG, PH, and PK	0		0.3 $V_{DD}1$	V
	$V_{IL}2$	Port PA	0		0.2 $V_{DD}1$	V
	$V_{IL}3$	Port PF	0		0.2 $V_{DD}1$	V
	$V_{IL}4$	Port BRES	0		0.2 $V_{DD}1$	V
Input amplitude	$V_{IN}1$	XIN	0.5		0.6	Vrms
	$V_{IN}2$	FMIN, AMIN: $V_{DD}1$ = 0.9 to 1.8 V	0.035		0.35	Vrms
	$V_{IN}3$	FMIN: $V_{DD}1$ = 0.9 to 1.8 V	0.05		0.35	Vrms
Input voltage range	$V_{IN}4$	ADI0, ADI1, ADI3, $V_{DD}1$	0		$V_{DD}4$	V
Input frequency	$F_{IN}1$	XIN: CI ≤ 35 kΩ	70	75	80	kHz
	$F_{IN}2$	FMIN: $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	10		130	MHz
	$F_{IN}3$	FMIN: $V_{IN}3$, $V_{DD}1$ = 0.9 to 1.8 V	130		250	MHz
	$F_{IN}4$	AMIN(L): $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	0.5		10	MHz
	$F_{IN}5$	AMIN(H): $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	2.0		20	MHz

Electrical Characteristics under allowable operating conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}1$	XIN: $V_{DD}1$ = 1.3 V			3	µA
	$I_{IH}2$	FMIN, AMIN: $V_{DD}1$ = 1.3 V	3	8	20	µA
	$I_{IH}3$	Port PF: $V_{DD}1$ = 1.3 V			4	µA
	$I_{IH}4$	PA (without pull-down resistors), the PC, PD, PG, and PH ports, and BRES, PK: $V_{DD}1$ = 1.3 V			3	µA
Input low-level current	$I_{IL}1$	XIN: $V_{DD}1 = V_{SS}$			–3	µA
	$I_{IL}2$	FMIN, AMIN: $V_{DD}1 = V_{SS}$	–3	–8	–20	µA
	$I_{IL}3$	Port PF: $V_{DD}1 = V_{SS}$			–4	µA
	$I_{IL}4$	PA (without pull-down resistors), the PC, PD, PG, and PH ports, and BRES, PK: $V_{DD}1 = V_{SS}$			–3	µA
Input floating voltage	V_{IF}	PA (with pull-down resistors)			0.05 $V_{DD}1$	V
Pull-down resistor values	$R_{PD}1$	PA/PF (with pull-down resistors), $V_{DD}1$ = 1.3 V	75	100	200	kΩ
	$R_{PD}2$	TEST1, TEST2 (with pull-down resistors), $V_{DD}1$ = 1.3 V		10		kΩ
Hysteresis	V_H	BRES	0.1 $V_{DD}1$	0.2 $V_{DD}1$		V
Output high-level voltage	$V_{OH}1$	PB: I_O = 1 mA	$V_{DD}1$ – 0.3 V_{DD}			V
	$V_{OH}2$	PC, PD, PG, PH and PK: I_O = 1 mA	$V_{DD}1$ – 0.3 $V_{DD}1$			V
	$V_{OH}3$	EO: I_O = 500 µA	$V_{DD}4$ – 0.3 $V_{DD}4$			V
	$V_{OH}4$	XOUT: I_O = 1 µA	$V_{DD}1$ – 0.3 $V_{DD}1$			V
	$V_{OH}5$	S1 to S20: I_O = 20 µA	$V_{DD}4$ –1			V
	$V_{OH}6$	COM1, COM2, COM3, COM4: I_O = 100 µA	$V_{DD}4$ –1			V
	$V_{OH}7$	VDC1: I_O = 1 mA	$V_{DD}4$ –1			V
Output low-level voltage	$V_{OL}1$	PB: I_O = –50 µA			0.3 $V_{DD}1$	V
	$V_{OL}2$	PC, PD, PG, PH and PK: I_O = –1 mA			0.3 $V_{DD}1$	V
	$V_{OL}3$	EO: I_O = –500 µA			0.3 $V_{DD}4$	V
	$V_{OL}4$	XOUT: I_O = –1 µA			0.3 $V_{DD}1$	V
	$V_{OL}5$	S1 to S20: I_O = –20 µA			$V_{DD}4$ –2	V
	$V_{OL}6$	COM1, COM2, COM3, COM4: I_O = –100 µA			$V_{DD}4$ –2	V
	$V_{OL}7$	PE: I_O = 2 mA			0.6 $V_{DD}1$	V
Output off leakage current	$I_{OFF}1$	Ports PB, PC, PD, PG, PK, and EO	–3		+3	µA
	$I_{OFF}2$	Port PE	–100		+100	nA
A/D converter error		ADI0, ADI1, ADI3 $V_{DD}1$	–1/2		+1/2	LSB
Current drain	$I_{DD}1$	$V_{DD}1$ = 1.3 V: $F_{IN}2$ 130 MHz, Ta = 25°C		10	30	mA
	$I_{DD}2$	$V_{DD}1$ = 1.3 V: In PLL stop mode, Ta = 25°C		0.15		mA
	$I_{DD}3$	$V_{DD}1$ = 1.3 V: In HALT mode, Ta = 25°C *1		0.1		mA
	$I_{DD}4$	$V_{DD}1$ = 1.8 V, with the oscillator stopped, Ta = 25°C *2		1		µA

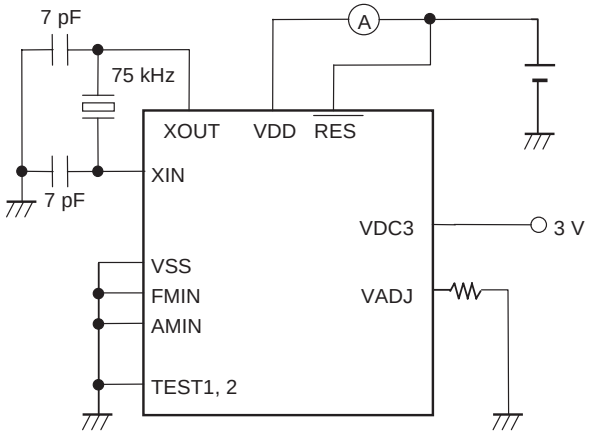
Note*: The halt mode current drain is due to 20 instructions being executed every 125 ms.

*1. Halt and PLL STOP mode current test circuit



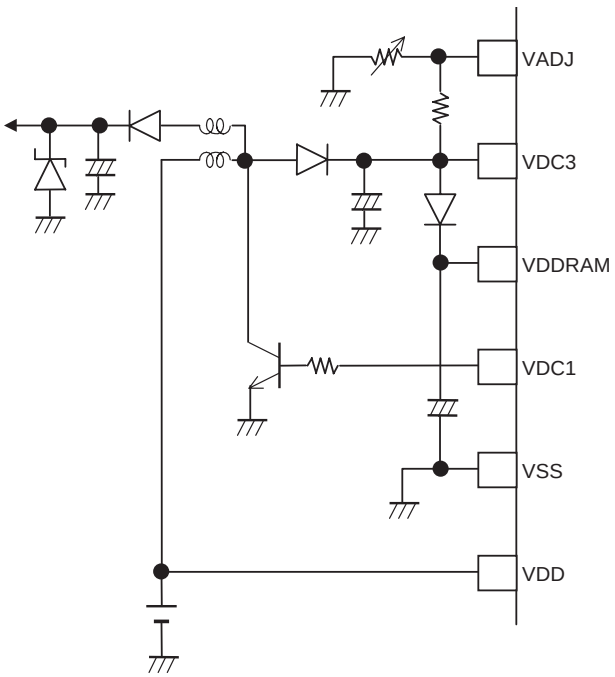
With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S20 selected.

*2. Backup mode current test circuit

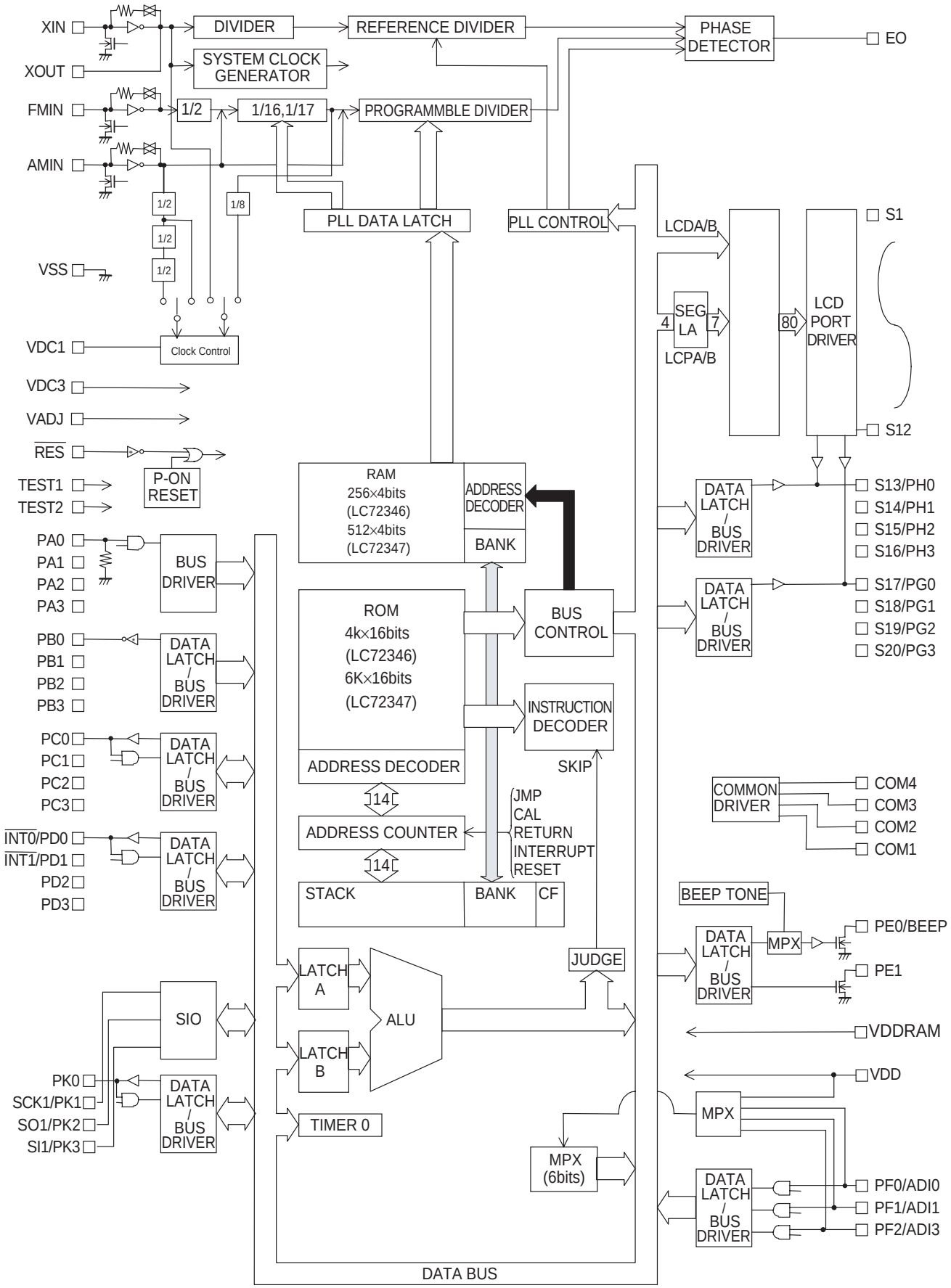


With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S20 selected.

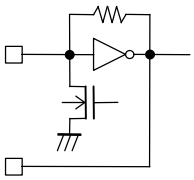
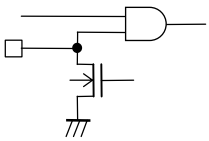
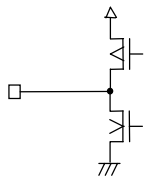
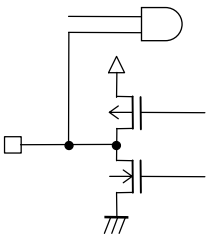
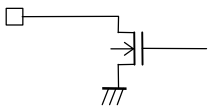
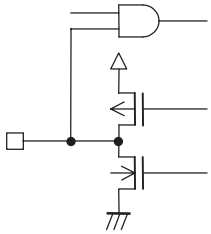
DC-DC Converter Application



Block Diagram



Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
64 1	XIN XOUT	I O	75 kHz oscillator connections	
63 2	TEST1 TEST2	I I	IC testing. These pins must be connected to ground.	—
6 5 4 3	PA0 PA1 PA2 PA3	I	Special-purpose ports for key return signal input designed with a low threshold voltage. When a key matrix is formed in combination with port PB, simultaneous multiple key presses with up to 3 keys can be detected. The pull-down resistors are set up for all four pins at the same time with the IOS instruction (PWn = 2.b1). This setting cannot be specified for individual pins. In backup mode, these pins go to the input disabled state, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor 
10 9 8 7	PB0 PB1 PB2 PB3	O	Unbalanced CMOS outputs. These outputs are switched with the IOS 0 instruction. Since these outputs are unbalanced, no diodes are required to prevent short circuits due to simultaneous multiple key presses. These outputs go to the high-impedance output state in backup mode. After a reset, they go to the high-impedance output state and remain in that state until an output instruction (OUT, SPB, or RPB) is executed.	Unbalanced CMOS push-pull 
14 13 12 11 18 17 16 15	PC0 PC1 PC2 PC3 $\overline{\text{INT1}}$/PD0 $\overline{\text{INT0}}$/PD1 PD2 PD3 *2	I/O	General-purpose I/O ports. PD0, PD1 can be used as an external interrupt port. The IOS instruction (Pwn = 4, 5) is used for switching the general-purpose I/O port function, and these ports can be set to input or output in 1-bit units. (0: input, 1: output) In backup mode they go to the input disabled high-impedance state. After a reset, they switch to the general-purpose input port function.	CMOS push-pull 
20 19	BEEP/PE0 PE1	O	General-purpose output and beep tone output shared function ports (PE0 only). The BEEP instruction is used to switch PE0 between the general-purpose output port and beep tone output functions. To use PE0 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use PE0 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. *: When PE0 is set up as the beep tone output, executing an output instruction to PE0 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only the PE0 pin can be switched between the general-purpose output function and the beep tone output function; the PE1 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V_{DD}. These ports are set to general-purpose output port function after a reset.	N-channel open-drain 
27 26 25 24	PK0 SCK1/PK1 SO1/PK2 SI1/PK3	I/O	Shared function pins used as either general-purpose I/O ports or a serial I/O port. When used as general-purpose I/O ports, the I/O direction can be switched in single pin units with the IOS instruction (with Pwn = C). The IOS instruction (with Pwn = 1, b2) is used to switch the function between the general-purpose I/O port and the serial I/O port function. (0: general-purpose I/O port, 1: serial I/O) In backup mode (low power mode) these pins go to the input disabled high-impedance state. After a reset, the general-purpose input port function is selected.	CMOS push-pull 

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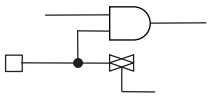
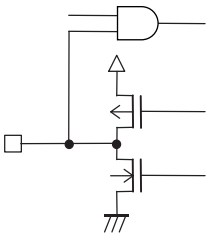
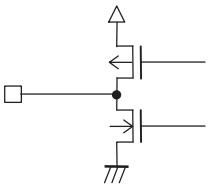
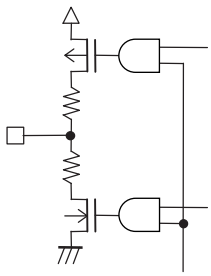
Pin No.	Pin	I/O	Function	I/O circuit
23 22 21	PF0/ADI0 PF1/ADI1 PF2/ADI3	I	General-purpose input and A/D converter input shared function ports. The IOS instruction (Pwn = FH) is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a units, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. *: If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 6-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (3FH) is (63/96) V_{DD}.	CMOS input/analog input 
33 34 35 36 37 38 39 40 *2	PG3/S20 PG2/S19 PG1/S18 PG0/S17 PH3/S16 PH2/S15 PH1/S14 PH0/S13	O	LCD driver segment output and general-purpose I/O shared function ports. The IOS instruction is used for switching between the segment output and general-purpose I/O functions and between input and output for the general-purpose I/O port function. • When used as segment output ports The general-purpose I/O port function is selected with the IOS instruction (Pwn = 8). b0 = S17 to 20/PG0 to 3 (0: Segment output, 1: PG0 to 3) The general-purpose I/O port function is selected with the IOS instruction (Pwn = 9). b0 = S13 to 16/PH0 to 3 (0: Segment output, 1: PH0 to 3) • When used as general-purpose I/O ports The IOS instruction (Pwn = 6,7) is used to select input or output. Note that the mode can be set in a bit units. b0 = PG0, b1 = PG1, b2 = PG2, b3 = PG3 ⟨0: Input, 1: Output⟩ b0 = PH0, b1 = PH1, b2 = PH2, b3 = PH3 ⟨0: Input, 1: Output⟩ In backup mode, these pins go to the input disabled high-impedance state if set up as general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset. Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function.	CMOS push-pull 
41 to 52	S12 to S1	O	LCD driver segment output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	CMOS push-pull 
53 54 55 56	COM4 COM3 COM2 COM1	O	LCD driver common output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	

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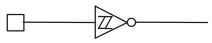
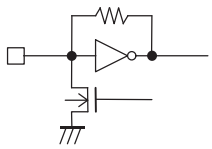
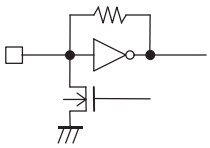
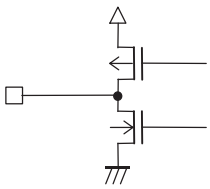
<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>I/O circuit</th></tr>
<tr><td>57</td><td>$\overline{\text{RES}}$</td><td>I</td><td>System reset input.
In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit.</td><td>  </td></tr>
<tr><td>31</td><td>VDC1</td><td>O</td><td>Output for the 3 V step-up circuit clock. Outputs 1/2 the AM local oscillator frequency in AM reception mode, and 1/256 the FM local oscillator or 75 kHz in FM reception mode.</td><td></td></tr>
<tr><td>30</td><td>VDC3</td><td>I</td><td>Voltage stepped up by the DC-DC converter (3 V)
May also be used to input an equivalent voltage.</td><td></td></tr>
<tr><td>29</td><td>VDDRAM</td><td>I</td><td>RAM backup power supply. Connected to the VDC3 voltage through a diode.</td><td></td></tr>
<tr><td>32</td><td>VADJ</td><td>O</td><td>VDC3 voltage adjustment pin. Insert a 10 kΩ trimmer between this pin and ground to adjust the VDC3 voltage.</td><td></td></tr>
<tr><td>59</td><td>FMIN</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected with the PLL instruction CW1.
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>60</td><td>AMIN</td><td>I</td><td>AM VCO (local oscillator) input.
This pin and the bandwidth are selected with the PLL instruction CW1.
<table>
<tr><th>CW1 b1, b0</th><th>Input pins</th><th>Bandwidth</th></tr>
<tr><td>1 0</td><td>AMIN (H)</td><td>2 to 20 MHz (SW)</td></tr>
<tr><td>1 1</td><td>FMIN (L)</td><td>0.5 to 10 MHz (MW, LW)</td></tr>
</table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>62</td><td>EO</td><td>O</td><td>Main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output,and the pin is set to the high-impedance state when the frequencies match.
This output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS push-pull
  </td></tr>
<tr><td>61
28
58</td><td>V_{SS}
V_{SS}
V_{DD}</td><td>—</td><td>Power supply pin. This pin must be connected to ground.
This pin must be connected to ground.
This pin must be connected to V_{DD}. Supports A/D converter.</td><td>—</td></tr>
</table>

Note*: When a pin in an I/O switching port is used as an output, applications must first set up the data with an OUT, SPB, or RPB instruction and then set up output mode with an IOS instruction.

LC72346/347 Series Instruction Set

Terminology

ADDR : Program memory address
b : Borrow
C : Carry
DH : Data memory address High (Row address) [2 bits]
DL : Data memory address Low (Column address) [4 bits]
I : Immediate data [4 bits]
M : Data memory address
N : Bit position [4 bits]
Rn : Resister number [4 bits]
Pn : Port number [4 bits]
PW : Port control word number [4 bits]
r : General register (One of the addresses from 00H to 0FH of BANK0)
( ), [ ] : Contents of register or memory
M (DH, DL) : Data memory specified by DH, DL

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format															
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
Addition instructions	AD	r	M	Add M to r	R ← (r) + (M)	0	1	0	0	0	0	DH		DL				r			
	ADS	r	M	Add M to r, then skip if carry	R ← (r) + (M), skip if carry	0	1	0	0	0	1	DH		DL				r			
	AC	r	M	Add M to r with carry	R ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				r			
	ACS	r	M	Add M to r with carry, then skip if carry	R ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I, skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C, skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	R ← (r) – (M)	0	1	1	0	0	0	DH		DL				r			
	SUS	r	M	Subtract M from r, then skip if borrow	R ← (r) – (M), skip if borrow	0	1	1	0	0	1	DH		DL				r			
	SB	r	M	Subtract M from r with borrow	R ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	R ← (r) – (M) – b, skip if borrow	0	1	1	0	1	1	DH		DL				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I, skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b, skip if borrow	0	1	1	1	1	1	DH		DL				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) – (M), skip if zero	0	0	0	1	0	0	DH		DL				r			
	SEQI	M	I	Skip if M equal to I	(M) – I, skip if zero	0	0	0	1	1	0	DH		DL				I			
	SNEI	M	I	Skip if M not equal to I	(M) – I, skip if not zero	0	0	0	0	0	1	DH		DL				I			
	SGE	r	M	Skip if r is greater than or equal to M	(r) – (M), skip if not borrow	0	0	0	1	1	0	DH		DL				r			
	SGEI	M	I	Skip if M is greater than equal to I	(M) – I, skip if not borrow	0	0	0	1	1	1	DH		DL				I			
	SLEI	M	I	Skip if M is less than I	(M) – I, skip if borrow	0	0	0	0	1	1	DH		DL				I			

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f e d c b a 9 8 7 6 5 4 3 2 1 0
Logic operation instructions	AND	r	M	AND M with r	R ← (r) AND (M)	0 0 1 0 0 0 DH DL r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0 0 1 DH DL I
	OR	r	M	OR M with r	R ← (r) OR (M)	0 0 1 0 1 0 DH DL r
	ORI	M	I	OR I with M	M ← (M) OR I	0 0 1 0 1 1 DH DL I
	EXL	r	M	Exclusive OR M with r	R ← (r) XOR (M)	0 0 1 1 0 0 DH DL r
	EXLI	M	I	Exclusive OR M with M	M ← (M) XOR I	0 0 1 1 1 0 DH DL I
	SHR	r		Shift r right with carry	carry (r)	0 0 0 0 0 0 0 0 1 1 1 0 r
Transfer instructions	LD	r	M	Load M to r	R ← (M)	1 1 0 1 0 0 DH DL r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1 0 1 DH DL r
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 1 0 1 1 0 DH DL r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 1 0 1 1 1 DH DL r
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 1 1 0 0 0 DH DL1 DL2
	MVI	M	I	Move I to M	M ← I	1 1 1 0 0 1 DH DL I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 1 1 1 0 0 DH DL N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 1 1 1 0 1 DH DL N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 0 ADDR (13 bits)
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + 1	1 0 1 ADDR (13 bits)
	RT			Return from subroutine	PC ← Stack	0 0 0 0 0 0 0 0 1 0 0 0
	RTI			Return from interrupt	PC ← Stack, BANK ← Stack, CARRY ← Stack	0 0 0 0 0 0 0 0 1 0 0 1
Status register instructions	SS	SWR	N	Set status register	(Status W-reg) N ← 1	1 1 1 1 1 1 1 1 0 0 0 SWR N
	RS	SWR	N	Reset status register	(Status W-reg) N ← 0	1 1 1 1 1 1 1 1 0 0 1 SWR N
	TST	SRR	N	Test status register true	If (Status R-reg) N = all 1, then skip	1 1 1 1 1 1 1 1 0 1 SRR N
	TSF	SRR	N	Test status register false	If (Status R-reg) N = all 0, then skip	1 1 1 1 1 1 1 1 1 0 SRR N
	TUL	N		Test Unlock F/F	If Unlock F/F (N) = All 0, then skip	0 0 0 0 0 0 0 0 1 1 0 1 N
Hardware control instructions	PLL	M		Load M to PLL register	PLL reg ← PLL data	1 1 1 1 1 0 DH DL r
	SIO	I1	I2	Serial I/O control	SIO reg ← I1, I2	0 0 0 0 0 0 0 1 I1 I2
	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0 0 0 0 0 0 0 0 1 I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0 0 0 0 0 0 0 1 0 I
	BEEP	I		Beep control	BEEP reg ← I	0 0 0 0 0 0 0 0 0 1 1 0 I
	DZC	I		Dead zone control	DZC reg ← I	0 0 0 0 0 0 0 0 1 0 1 1 I
	TMS	I		Set timer register	Timer reg ← I	0 0 0 0 0 0 0 0 1 1 0 0 I
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1 1 1 1 1 1 1 0 PWn N
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1 1 1 0 1 0 DH DL Pn
	OUT	M	Pn	Output contents of M to port	Pn ← M	1 1 1 0 1 1 DH DL Pn
	INR	M	Rn	Input register/port data to M	M ← (Pn reg)	0 0 1 1 1 0 DH DL Pn
	OUTR	M	Rn	Output contents of M to register/port	Rn reg ← (M)	0 0 1 1 1 1 DH DL Rn
	SPB		N	Set port1 bits	(Pn)N ← 1	0 0 0 0 0 0 1 0 Pn N
	RPB		N	Reset port1 bits	(Pn)N ← 0	0 0 0 0 0 0 1 1 Pn N
	TPT		N	Test port1 bits, then skip if all bits specified are true	If (Pn)N = all 1, then skip	1 1 1 1 1 1 0 0 Pn N
	TPF		N	Test port1 bits, then skip if all bits specified are false	If (Pn)N = all 0, then skip	1 1 1 1 1 1 0 1 Pn N
Bank switching instructions	BANK	I		Select Bank	BANK ← I	0 0 0 0 0 0 0 0 0 1 1 1 I

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
LCD instructions	LCDA	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1	1	0	0	0	0	DH		DL				DIGIT			
	LCDB	M	I			1	1	0	0	0	1	DH		DL				DIGIT			
	LCPA	M	I	Output segment pattern to LCD digit through LA	LCD (DIGIT) ← LA ← M	1	1	0	0	1	0	DH		DL				DIGIT			
	LCPB	M	I			1	1	0	0	1	1	DH		DL				DIGIT			
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0	0	0	0	0	0	0	0	0	1	0	0	I			
	CKSTP			Clock stop	Stop x'tal OSC	0	0	0	0	0	0	0	0	0	1	0	1				
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0	0				