Ordering number : ENN7022

CMOS IC

LC72317, 72318, 72319

Low-Voltage ETR-Controller

Overview

The LC72317, 72318 and 72319 are low-voltage electronic tuning radio microcontrollers that include a PLL that operates up to 250 MHz and a 1/4 duty 1/2 bias LCD driver on chip. These ICs include an on-chip DC-DC converter, making it is easy to create the supply voltages required for tuning and allowing cost reductions in end products.

These ICs are optimal for use in low-voltage portable audio equipment that includes a radio receiver.

Function

- Program memory (ROM):
  - — 6144 × 16 bits (12K bytes) LC72317
  - — 8192 × 16 bits (16K bytes) LC72318/319
- Data memory (RAM):
  - — 256 × 4 bits LC72317/318
  - — 512 × 4 bits LC72319
- Cycle time: 40 µs (all 1-word instructions) at 75kHz crystal oscillation
- Stack: 8 levels
- LCD driver: 48 to 112 segments (1/4 duty, 1/2 bias drive)
- Interrupts: Two external interrupts
  Timer interrupts (1, 5, 10, and 50 ms)
- A/D converter: Three input channels
  (5-bit successive approximation conversion)
- Input ports: 9 ports (of which three can be switched for use as A/D converter inputs)
- Output ports: 6 ports (of which 1 can be switched for use as the beep tone output and 2 are open-drain ports)

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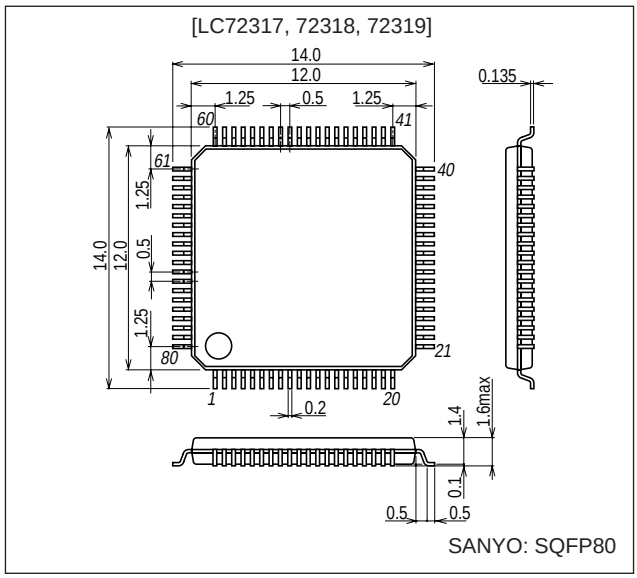
Package Dimensions

unit: mm

3220-SQFP80



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I/O ports: 29 pins (Of these 16 can be switched over to function as LCD ports as a mask options, and 3 ports can be switched over for use with serial I/O.)
- Serial I/O: One system
- Reference frequencies: 1, 3, 3.125, 5, 6.25, 12.5, and 25 kHz
- Input frequencies: FM band: 10 to 250 MHz
  AM band: 0.5 to 20 MHz
- Input sensitivity:
  FM band: 35 mVrms (50 mVrms at 130 MHz or higher frequency)
  AM band: 35 mVrms
- IF counting: Using the HCTR input pin for 0.4 to 12 MHz signals
- External reset input: During CPU and PLL operations, instruction execution is started from location 0.
- Built-in power-on reset circuit:
  The CPU starts execution from location 0 when power is first applied.
- Halt mode: The controller-operating clock is stopped.
- Backup mode: The crystal oscillator is stopped.
- Static power-on function: Backup state is cleared with the PF port
- Beep tone: 1.5 and 3.1 kHz
- Built-in tuner voltage generating circuit:
  Cost reduced in tuner-use power supply circuit
- Memory retention voltage: 0.9 V at least
- V_{DD} voltage
  — PLL: 1.8 to 3.6 V
  — CPU and ADC: 1.6 to 3.6 V
- Optional function switches:
  — PH0 to PH3 (open-drain output/general-purpose input and output/S13 to S16)
  — PG0 to PG3 (open-drain output/general-purpose input and output/S17 to S20)
  — PI0 to PI3 (open-drain output/general-purpose input and output/S21 to S24)
  — PJ0 to PJ3 (open-drain output/general-purpose input and output/S25 to S28)
  — VSENSE circuit (provided/not provided)
  — FM DC/DC clock (1/256, 75 kHz)
- Package: SQFP-80 (0.5-mm pitch)

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	VDD	–0.3 to +4.0	V
Input voltage	V_{IN}	All input pins	–0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}(1)	AOUT, PE	–0.3 to +15	V
	V_{OUT}(2)	All output pins except V_{OUT}(1)	–0.3 to V_{DD} + 0.3	V
Output current	I_{OUT}(1)	PC, PD, PG, PH, PI, PJ, PK, PL, EO	0 to 3	mA
	I_{OUT}(2)	PB	0 to 1	mA
	I_{OUT}(3)	AOUT, PE	0 to 2	mA
	I_{OUT}(4)	S1 to S28	300	µA
	I_{OUT}(5)	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –20 to +70°C	300	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –20 to +70°C, V_{DD} = 1.8 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}(1)$	PLL operating voltage	1.8	3.0	3.6	V
	$V_{DD}(2)$	Memory retention voltage	1.0			
	$V_{DD}(3)$	CPU operating voltage	1.4	3.0	3.6	
	$V_{DD}(4)$	A/D converter operating voltage	1.6	3.0	3.6	
Input high-level voltage	$V_{IH}(1)$	Input ports other than $V_{IH}(2)$, $V_{IH}(3)$, AMIN, FMIN, HCTR, and XIN	0.7 V_{DD}		V_{DD}	V
	$V_{IH}(2)$	BRES port	0.8 V_{DD}		V_{DD}	V
	$V_{IH}(3)$	Port PF	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	$V_{IL}(1)$	Input ports other than $V_{IL}(2)$, $V_{IL}(3)$, AMIN, FMIN, HCTR, and XIN	0		0.3 V_{DD}	V
	$V_{IL}(2)$	BRES port	0		0.2 V_{DD}	V
	$V_{IL}(3)$	Port PF	0		0.2 V_{DD}	V
Input amplitude	$V_{IN}(1)$	XIN	0.5		0.6	Vrms
	$V_{IN}(2)$	FMIN, AMIN	0.035		0.35	Vrms
	$V_{IN}(3)$	FMIN	0.05		0.35	Vrms
	$V_{IN}(4)$	HCTR	0.035		0.35	Vrms
Input voltage range	$V_{IN}(5)$	ADIO, ADI1, ADI3	0		V_{DD}	V
Input frequency	$F_{IN}(1)$	XIN: CI ≤ 35 kΩ	70	75	80	kHz
	$F_{IN}(2)$	FMIN: $V_{IN}(2)$, $V_{DD}(1)$	10		130	MHz
	$F_{IN}(3)$	FMIN: $V_{IN}(3)$, $V_{DD}(1)$	130		250	MHz
	$F_{IN}(4)$	AMIN(H): $V_{IN}(3)$, $V_{DD}(1)$	2		40	MHz
	$F_{IN}(5)$	AMIN(L): $V_{IN}(3)$, $V_{DD}(1)$	0.5		10	MHz
	$F_{IN}(6)$	HCTR: $V_{IN}(3)$, $V_{DD}(1)$	0.4		12	MHz

Electrical Characteristics within the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}(1)$	XIN: $V_I = V_{DD} = 3.0$ V			3	µA
	$I_{IH}(2)$	FMIN, AMIN, HCTR: $V_I = V_{DD} = 3.0$ V	3	8	20	µA
	$I_{IH}(3)$	PA/PF (without pull-down resistors), the PC, PD, PG, PH, PI, PJ, PK, and PL ports, and BRES: $V_I = V_{DD} = 3.0$ V			3	µA
Input low-level current	$I_{IL}(1)$	XIN: $V_{DD(1)} = V_{SS}$			–3	µA
	$I_{IL}(2)$	FMIN, AMIN, HCTR: $V_I = V_{DD} = V_{SS}$	–3	–8	–20	µA
	$I_{IL}(3)$	PA/PF (without pull-down resistors), the PC, PD, PG, PH, PI, PJ, PK, and PL ports, and BRES: $V_I = V_{DD} = V_{SS}$			–3	µA
Input floating voltage	V_{IF}	PA/PF (with pull-down resistors)			0.05 V_{DD}	V
Pull-down resistor values	$R_{PD}(1)$	PA/PF (with pull-down resistors), $V_{DD} = 3.0$ V	75	100	200	kΩ
	$R_{PD}(2)$	TEST1, TEST2 (with pull-down resistors)		10		kΩ
Hysteresis	V_H	BRES	0.1 V_{DD}	0.2 V_{DD}		V
Voltage doubler reference voltage	DBR4	Referenced to V_{DD}, C(3) = 0.47 µF, Ta = 25°C *1	1.3	1.5	1.7	V
Voltage doubler step-up voltage	DBR1, 2, 3	C(1) = 0.47 µF C(2) = 0.47 µF, without loading, Ta = 25°C *1	2.7	3.0	3.3	V
Output high-level voltage	$V_{OH}(1)$	PB: I_O = –1 mA	V_{DD} – 0.7 V_{DD}		V_{DD} – 0.3 V_{DD}	V
	$V_{OH}(2)$	PC, PD, PG, PH, PI, PJ, PK, PL: I_O = –1 mA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}(3)$	EO: I_O = –500 µA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}(4)$	XOUT: I_O = –1 µA	V_{DD} – 0.3 V_{DD}			V
	$V_{OH}(5)$	S1 to S28: I_O = –20 µA *1	2.0			V
	$V_{OH}(6)$	COM1, COM2, COM3, COM4: I_O = –100 µA *1	2.0			V

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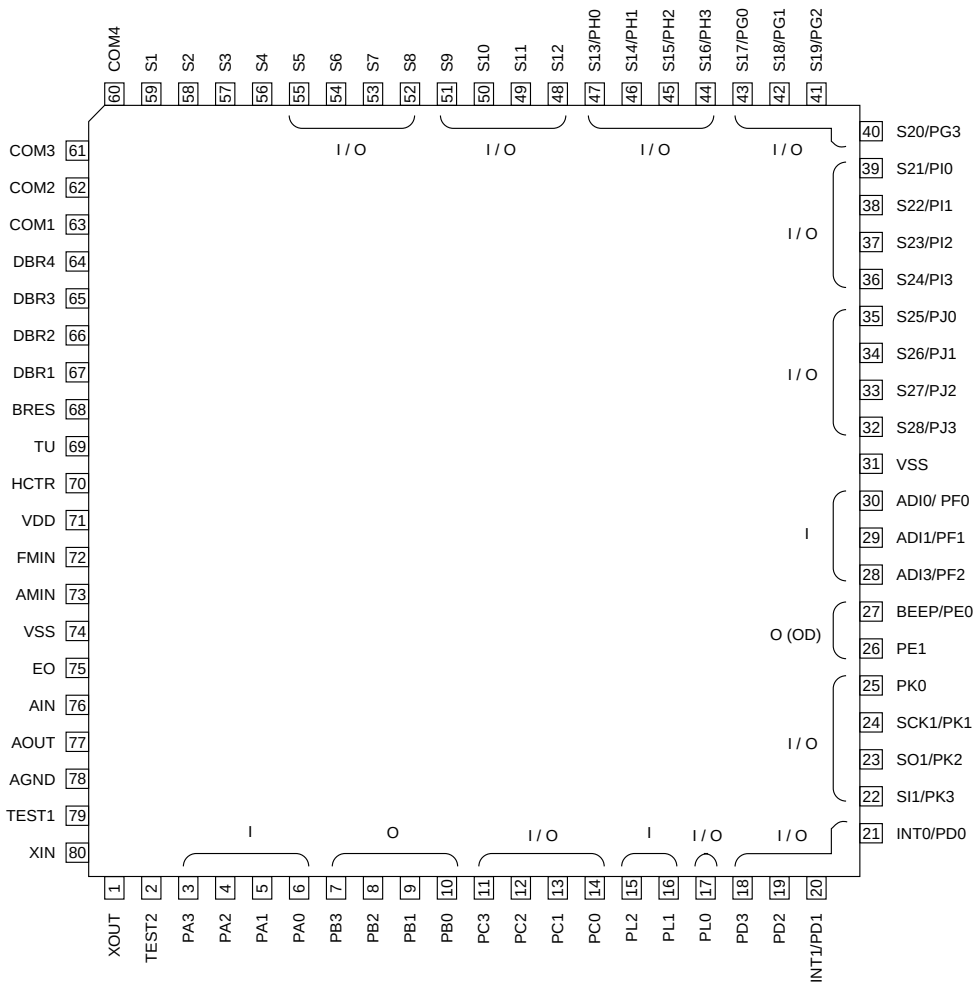
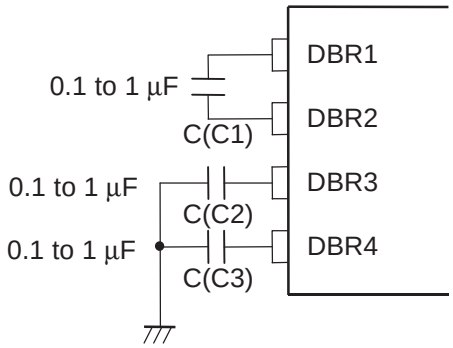
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output low-level voltage	V_{OL}(1)	PB: I_O = –1 mA	0.3 V_{DD}		0.7 V_{DD}	V
	V_{OL}(2)	PC, PD, PG, PH, PI, PJ, PK, PL: I_O = –1 mA			0.3 V_{DD}	V
	V_{OL}(3)	EO: I_O = –500 µA			0.3 V_{DD}	V
	V_{OL}(4)	XOUT: I_O = –1 µA			0.3 V_{DD}	V
	V_{OL}(5)	S1 to S28: I_O = –20 µA *1			1.0	V
	V_{OL}(6)	COM1, COM2, COM3, COM4: I_O = –100 µA *1			1.0	V
	V_{OL}(7)	PE: I_O = 2 mA			1.0	V
	V_{OL}(8)	AOUT, TU: I_O = 1 mA, AIN = 1.3 V (AOUT), V_{DD} = 3 V			0.5	V
Output off leakage current	I_{OFF}(1)	Ports PB, PC, PD, PG, PH, PI, PJ, PK, PL, and EO	–3		+3	µA
	I_{OFF}(2)	AOUT, TU and port PE	–100		+100	nA
A/D converter error		ADI0, ADI1, ADI3	–1/2		+1/2	LSB
Supply voltage drop detection voltage	V_{SENSE}(1)	Ta = 25°C *2	1.6	1.75	1.9	V
Supply voltage rise detection voltage	V_{SENSE}(2)	Ta = 25°C *2	(1)min +0.1		(1)max +0.2	V
Current drain	I_{DD}(1)	V_{DD}(1): F_{IN}(2) 130 MHz, Ta = 25°C		5	15	mA
	I_{DD}(2)	V_{DD}(1): In HALT mode, Ta = 25°C *3		0.1		mA
	I_{DD}(3)	V_{DD} = 3.6 V, with the oscillator stopped, Ta = 25°C *4		0.1		mA
	I_{DD}(4)	V_{DD} = 1.8 V, with the oscillator stopped, Ta = 25°C *4		1		µA

Note: The halt mode current is due to the CPU executing 20 instruction steps every 125 ms.

Pin Assignment



Note: * C(1), C(2), and C(3) must be connected even if an LCD is not used.

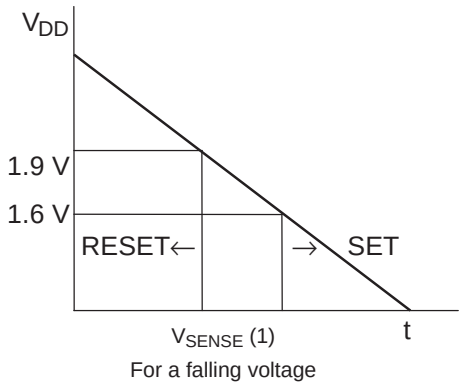


Notes: *1. The capacitors C(1), C(2), and C(3) must be connected to the DBR pins.

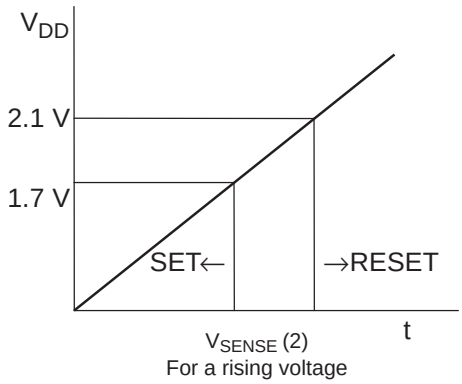
*2. V_{SENSE}

When the V_{DD} voltage drops, the V_{SENSE} flag is set when that voltage is 1.75 V (typical). Applications can check the V_{SENSE} flag using the TST instruction. Battery or other power source depletion can be easily measured by monitoring this flag.

Note that the voltage for V_{SENSE} detection differs for the falling and rising directions. Thus, after the V_{SENSE} flag has been set due to a voltage drop, it will not be reset if the voltage rises by under 0.1 V.

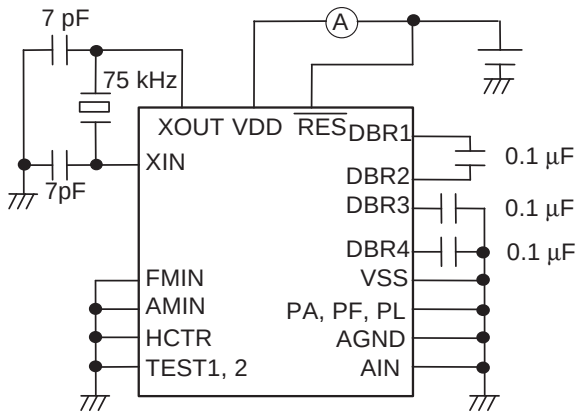


For a falling voltage



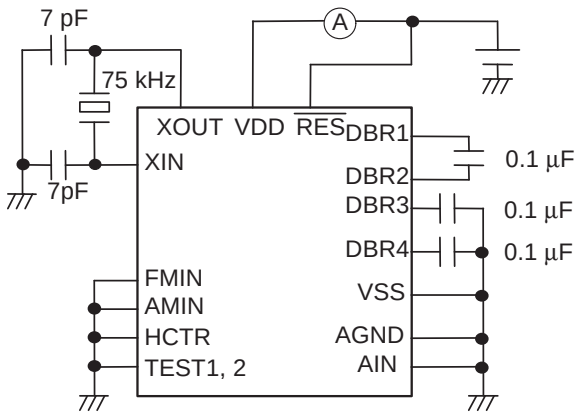
For a rising voltage

*3. Halt mode current measurement circuit



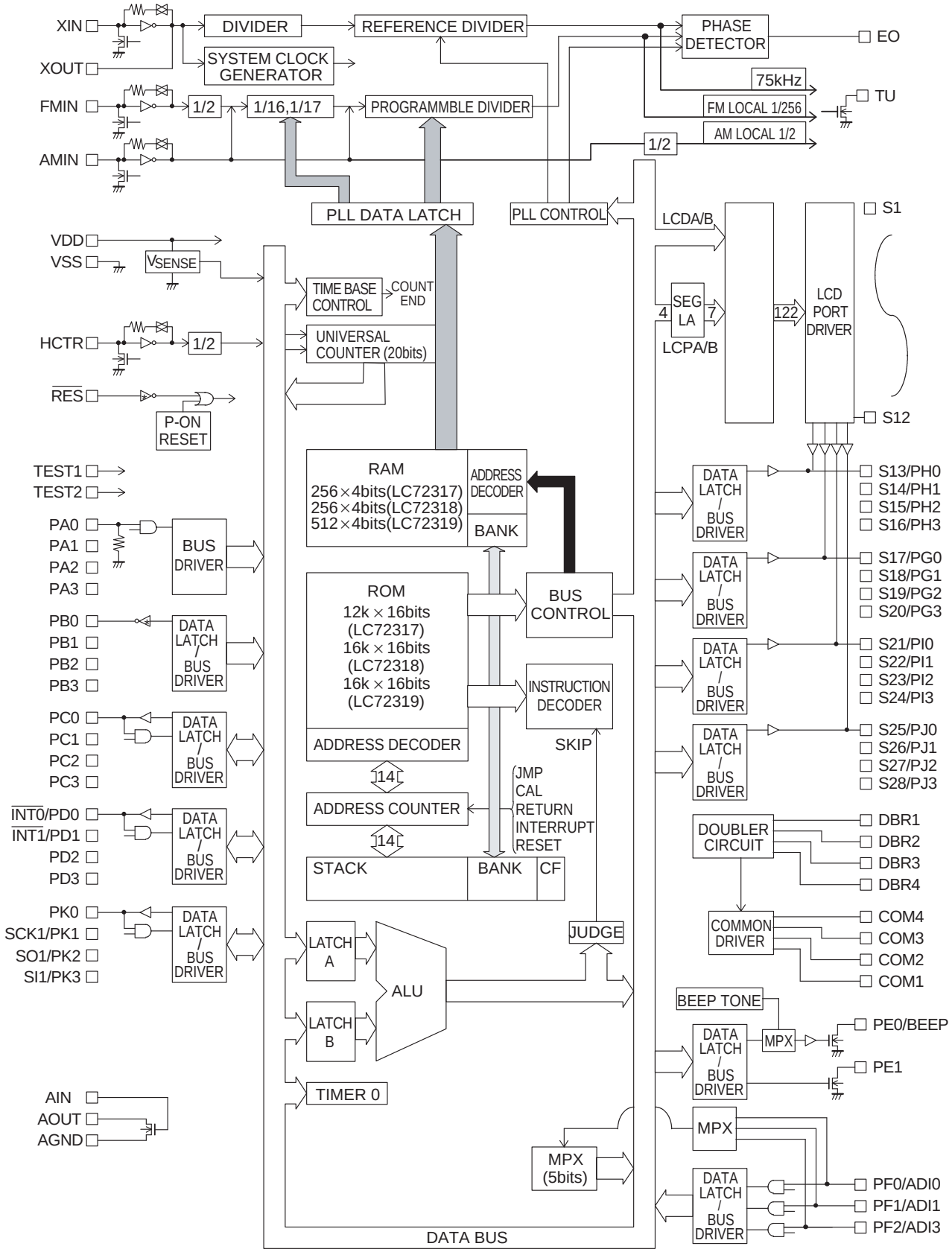
With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S28 selected.

*4. Backup mode current measurement circuit

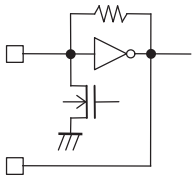
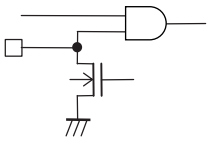
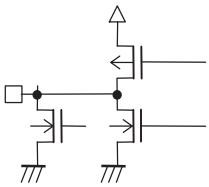
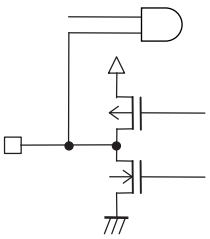
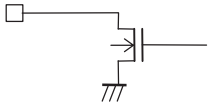


With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S28 selected.

Block Diagram



Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
80 1	XIN XOUT	I O	75 kHz oscillator connections	
79 2	TEST1 TEST2	I I	IC testing. These pins must be connected to ground during normal operation.	—
6 5 4 3	PA0 PA1 PA2 PA3	I	Special-purpose key return signal input ports designed with a low threshold voltage. When used in conjunction with port PB to form a key matrix, up to 3 simultaneous key presses can be detected. The four pull-down resistors are selected together in a single operation using the IOS instruction; they cannot be specified individually. Input is disabled in backup mode, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor 
10 9 8 7	PB0 PB1 PB2 PB3	O	General-purpose CMOS and n-channel open-drain output shared-function ports. The IOS instruction (Pwn = 2) is used for function switching. (b0: PB0, b2: PB1, b3: PB2, PB3) (0: general-purpose CMOS, 1: n-channel open-drain) Special-purpose key source signal output ports. Since unbalanced CMOS output transistor circuits are used, diodes to prevent short-circuits when multiple keys are pressed are not required. These ports go to the output high-impedance state in backup mode. These ports go to the output high-impedance state after a reset and remain in that state until an output instruction (OUT, SPB, or RPB) is executed. *: Verify the output impedance conditions carefully if these pins are used for functions other than key source outputs.	Unbalanced CMOS push-pull/n-channel open-drain 
14 13 12 11 21 20 19 18 17	PC0 PC1 PC2 PC3 $\overline{\text{INT0}}$/PD0 $\overline{\text{INT1}}$/PD1 PD2 PD3 PL0 *2	I/O	General-purpose I/O ports. PD0 and PD1 can be used as an external interrupt port. Input or output mode can be set individually using the IOS instruction by the bit . A value of 0 specifies input, and 1 specifies output. These ports go to the input disabled high-impedance state in backup mode. They are set to function as general-purpose input ports after a reset.	CMOS push-pull 
27 26	BEEP/PE0 PE1	O	General-purpose output ports with shared beep tone output function (pin 27 only). The BEEP instruction is used to switch pin 27 between the general-purpose output port and beep tone output functions. To use pin 27 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use pin 27 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. *: When pin 27 is set up as the beep tone output, executing an output instruction to pin 27 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only pin 27 can be switched between the general-purpose output function and the beep tone output function; the PE1 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V_{DD}. These ports are set to general-purpose output port function after a reset.	N-channel open-drain 

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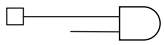
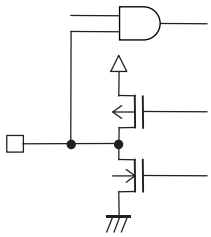
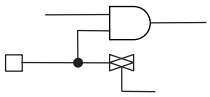
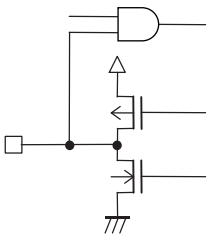
Pin No.	Pin	I/O	Function	I/O circuit
25 24 23 22	PK0 SCK1/PK1 SO1/PK2 SI1/PK3	I/O I/O I/O I/O	General-purpose input ports, general-purpose I/O ports, and serial I/O port. The general-purpose I/O port is switched using the IOS instruction; the direction (input or output) is set in a 1-bit unit. Switching between the general-purpose input port and the serial I/O port function is also performed with the IOS instruction. In backup mode, these ports go to the input disabled high-impedance state. After a reset, these pins are set to function as general-purpose input ports.	CMOS input  CMOS push-pull 
30 29 28	PF0/ADI0 PF1/ADI1 PF2/ADI3	I	General-purpose input and A/D converter input shared function ports. The IOS instruction is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched by the bit, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. *: If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 5-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (1FH) is (63/96) 3 V.	CMOS input/analog input 
32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 *2	PJ3/S28 PJ2/S27 PJ1/S26 PJ0/S25 PI3/S24 PI2/S23 PI1/S22 PI0/S21 PG3/S20 PG2/S19 PG1/S18 PG0/S17 PH3/S16 PH2/S15 PH1/S14 PH0/S13	O	Shared function ports that function either as LCD driver segment outputs or general-purpose I/O ports. The IOS instruction is used to switch between the segment output and the general-purpose I/O port functions. It is also used to switch the direction of pins functioning as general-purpose I/O ports. • When used as segment output ports The IOS (Pwn=8) instruction is used to set the following 4 pins to function as segment output ports. b0 to b3 correspond to S17 to S20/PG0 to PG3 (0: Segment output, 1: PG0 to PG3) The IOS (Pwn=9) instruction is used to set the following 4 pins to function as segment output ports. b0 to b3 correspond to S13 to S16/PH0 to PH3 (0: Segment output, 1: PH0 to PH3) The IOS (Pwn=D) instruction is used to set the following 4 pins to function as segment output ports. b0 to b3 correspond to S21 to S24/PI0 to PI3 (0: Segment output, 1: PG0 to PG3) The IOS (Pwn=E) instruction is used to set the following 4 pins to function as segment output ports. b0 to b3 correspond to S25 to S28/PJ0 to PJ3 (0: Segment output, 1: PH0 to PH3) • When used as general-purpose I/O ports The IOS instruction is used to switch the I/O direction. The directions of these pins can be set individually in 1-bit units. {b0 = PG0, b1 = PG1, b2 = PG2, b3 = PG3} {b0 = PH0, b1 = PH1, b2 = PH2, b3 = PH3} {b0 = PI0, b1 = PI1, b2 = PI2, b3 = PI3} {b0 = PJ0, b1 = PJ1, b2 = PJ2, b3 = PJ3} {0: Input, 1: Output} In backup mode, if used as general-purpose I/O ports, they will be in the input disabled high-impedance state. If used as segment outputs, they will be held fixed at the low level. After a reset, these pins function as segment output ports. Although the general-purpose port/LCD port setting is a mask option, the setup with the IOS instruction described above is also necessary.	CMOS push-pull 

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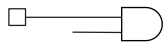
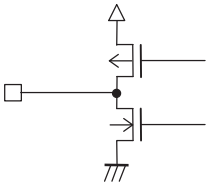
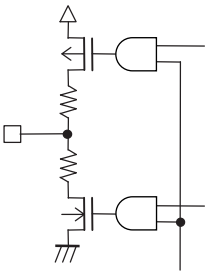
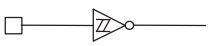
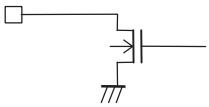
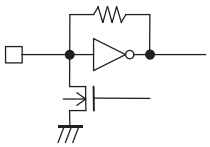
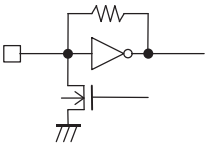
<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>I/O circuit</th></tr>
<tr><td>16
15</td><td>PL1
PL2</td><td>I</td><td>General-purpose input ports
In backup mode, these ports go to the input disabled high-impedance state.</td><td>CMOS input
  </td></tr>
<tr><td>48 to
59</td><td>S12 to S1</td><td>O</td><td>LCD driver segment output pins.
A 1/4-duty 1/2-bias drive technique is used.
The frame frequency is 75 Hz.
In backup mode, the outputs are fixed at the low level.
After a reset, the outputs are fixed at the low level.</td><td>CMOS push-pull
  </td></tr>
<tr><td>60
61
62
63</td><td>COM4
COM3
COM2
COM1</td><td>O</td><td>LCD driver common output pins.
A 1/4-duty 1/2-bias drive technique is used.
The frame frequency is 75 Hz.
In backup mode, the outputs are fixed at the low level.
After a reset, the outputs are fixed at the low level.</td><td>  </td></tr>
<tr><td>64
65
66
67</td><td>DBR4
DBR3
DBR2
DBR1</td><td>I</td><td>LCD power supply step-up voltage inputs.</td><td></td></tr>
<tr><td>68</td><td>$\overline{\text{RES}}$</td><td>I</td><td>System reset input.
In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit.</td><td>  </td></tr>
<tr><td>69</td><td>TU</td><td>O</td><td>Tuning voltage generation circuit outputs.
These pins include a transistor, and a tuning voltage (12 to 17 V) can be generated by connecting external coil, diode, and capacitor components.</td><td>N-channel open-drain
  </td></tr>
<tr><td>72</td><td>FMIN</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected with the PLL instruction CW1.
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>73</td><td>AMIN</td><td>I</td><td>AM VCO (local oscillator) input.
This pin and the bandwidth are selected with the PLL instruction CW1.
<table><tr><th>CW1 b1, b0</th><th>Bandwidth</th></tr><tr><td>1 1</td><td>0.5 to 10 MHz (MW, LW)</td></tr></table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
</table>

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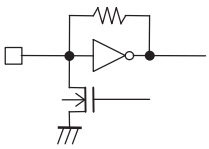
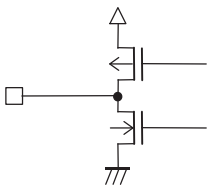
<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>I/O circuit</th></tr>
<tr><td>70</td><td>HCTR</td><td>I</td><td>Special-purpose universal counter input port
• To measure a frequency, set up HCTR frequency measurement mode and the measurement time with a UCS instruction (b3=0, b2=0) and start the count with a UCC instruction.
<table>
<tr><th colspan="3"></th><th>UCS b1 b0</th><th>Measurement time</th></tr>
<tr><th>UCS b3 b2</th><th>Input pin</th><th>Measurement mode</th><th>0 0</th><td>1 ms</td></tr>
<tr><td>0 0</td><td>HCTR</td><td>Frequency measurement</td><td>0 1</td><td>4 ms</td></tr>
<tr><td>0 1</td><td>–</td><td></td><td>1 0</td><td>8 ms</td></tr>
<tr><td>1 0</td><td>–</td><td></td><td>1 1</td><td>32 ms</td></tr>
</table>
The CNTEND flag is set when the count completes. Since the input circuit functions as an AC amplifier in this mode, the input must be capacitance coupled.
This pin goes to the input disabled state in backup mode, halt mode, PLL stop mode, and after a reset.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>76
77
78</td><td>AIN
AOUT
AGND</td><td>I
O
–</td><td>Connections for the built-in transistor used to form a low-pass filter.
AGND is connected to ground.</td><td></td></tr>
<tr><td>75</td><td>EO</td><td>O</td><td>Main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output. The pin is set to the high-impedance state when the frequencies match.
Output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS push-pull
  </td></tr>
<tr><td>74
31
71</td><td>V_{SS}
V_{SS}
V_{DD}</td><td>—</td><td>Power supply pin. This pin must be connected to ground.
This pin must be connected to ground.
This pin must be connected to V_{DD}.</td><td>—</td></tr>
</table>

Note 2: When a pin in an I/O switching port is used as an output, applications must first set up the data with an OUT, SPB, or RPB instruction and then set up output mode with an IOS instruction.

LC72317, 72318 and 72319 Series Instruction Set

Terminology

ADDR : Program memory address
b : Borrow
C : Carry
DH : Data memory address High (Row address) [2 bits]
DL : Data memory address Low (Column address) [4 bits]
I : Immediate data [4 bits]
M : Data memory address
N : Bit position [4 bits]
Rn : Resister number [4 bits]
Pn : Port number [4 bits]
PW : Port control word number [4 bits]
r : General register (One of the addresses from 00H to 0FH of BANK0)
( ), [ ] : Contents of register or memory
M (DH, DL) : Data memory specified by DH, DL

Instructions	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				r			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M), skip if carry	0	1	0	0	0	1	DH		DL				r			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				r			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I, skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C, skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	DH		DL				r			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M), skip if borrow	0	1	1	0	0	1	DH		DL				r			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b, skip if borrow	0	1	1	0	1	1	DH		DL				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I, skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b, skip if borrow	0	1	1	1	1	1	DH		DL				I			

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Instructions	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f e d c b a 9 8 7 6 5 4 3 2 1 0
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) – (M), skip if zero	0 0 0 1 0 0 DH DL r
	SEQI	M	I	Skip if M equal to I	(M) – I, skip if zero	0 0 0 1 1 0 DH DL I
	SNEI	M	I	Skip if M not equal to I	(M) – I, skip if not zero	0 0 0 0 0 1 DH DL I
	SGE	r	M	Skip if r is greater than or equal to M	(r) – (M), skip if not borrow	0 0 0 1 1 0 DH DL r
	SGEI	M	I	Skip if M is greater than equal to I	(M) – I, skip if not borrow	0 0 0 1 1 1 DH DL I
	SLEI	M	I	Skip if M is less than I	(M) – I, skip if borrow	0 0 0 0 1 1 DH DL I
Logic instructions	AND	r	M	AND M with r	r ← (r) AND (M)	0 0 1 0 0 0 DH DL r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0 0 1 DH DL I
	OR	r	M	OR M with r	r ← (r) OR (M)	0 0 1 0 1 0 DH DL r
	ORI	M	I	OR I with M	M ← (M) OR I	0 0 1 0 1 1 DH DL I
	EXL	r	M	Exclusive OR M with r	r ← (r) XOR (M)	0 0 1 1 0 0 DH DL r
	EXLI	M	I	Exclusive OR M with M	M ← (M) XOR I	0 0 1 1 1 0 DH DL I
	SHR	r		Shift r right with carry	carry → (r) → carry	0 0 0 0 0 0 0 0 1 1 1 0 r
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 1 0 1 0 0 DH DL r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1 0 1 DH DL r
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 1 0 1 1 0 DH DL r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 1 0 1 1 1 DH DL r
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 1 1 0 0 0 DH DL1 DL2
	MVI	M	I	Move I to M	M ← I	1 1 1 0 0 1 DH DL I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1s, then skip	1 1 1 1 0 0 DH DL N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0s, then skip	1 1 1 1 0 1 DH DL N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 0 ADDR (13 bits)
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + 1	1 0 1 ADDR (13 bits)
	RT			Return from subroutine	PC ← Stack	0 0 0 0 0 0 0 0 1 0 0 0
	RTI			Return from interrupt	PC ← Stack, BANK ← Stack, CARRY ← Stack	0 0 0 0 0 0 0 0 1 0 0 1

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Instructions	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f e d c b a 9 8 7 6 5 4 3 2 1 0
Status register instructions	SS	SWR	N	Set status register	(Status W-reg) N ← 1	1 1 1 1 0 1 0 1 1 1 SWR N
	RS	SWR	N	Reset status register	(Status W-reg) N ← 0	1 0 1 1 1 1 1 1 1 1 SWR N
	TST	SRR	N	Test status register true	if (Status R-reg) N = all	1 1 1 1 1 0 0 0 0 SRR N
	TSF	SRR	N	Test status register false	if (Status R-reg) N = all	1 1 1 1 1 0 0 0 1 SRR N
	TUL	N		Test Unlock F/F	if Unlock F/F (N) = all 0s, then skip	0 0 0 0 0 0 0 0 1 1 0 1 N
Hardware control instructions	PLL	M		Load M to PLL register	PLL reg ← PLL data	1 1 1 1 1 0 DH DL r
	SIO	I1			SIO reg ← I1, I2	0 0 0 0 0 0 0 0 1 I1 I2
	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0 0 0 0 0 0 0 0 1 I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0 0 0 0 0 0 0 1 0 I
	BEEP	I		Beep control	BEEP reg ← I	0 0 0 0 0 0 0 0 0 1 1 0 I
	DZC	I		Dead zone control	DZC reg ← I	0 0 0 0 0 0 0 0 1 0 1 1 I
	TMS	I		Set timer register	Timer reg ← I	0 0 0 0 0 0 0 0 1 1 0 0 I
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1 1 1 1 1 1 1 0 PWn N
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1 1 1 0 1 0 DH DL Pn
	OUT	M	Pn	Output contents of M to port	P1n ← M	1 1 1 0 1 1 DH DL Pn
	INR	M	Pn	Input port data to M	M ← (Pn)	0 0 1 1 1 0 DH DL Pn
	SPB	P1n	N	Set port1 bits	(Pn)N ← 1	0 0 0 0 0 0 1 0 Pn N
	RPB	P1n	N	Reset port1 bits	(Pn)N ← 0	0 0 0 0 0 0 1 1 Pn N
	TPT	P1n	N	Test port1 bits, then skip if all bits specified are true	if (Pn)N = all 1s, then skip	1 1 1 1 1 1 0 0 Pn N
	TPF	P1n	N	Test port1 bits, then skip if all bits specified are false	if (Pn)N = all 0s, then skip	1 1 1 1 1 1 0 1 Pn N
Bank switching instructions	BANK	I		Select Bank	BANK ← I	0 0 0 0 0 0 0 0 0 1 1 1 I
LCD instructions	LCDA	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1 1 0 0 0 0 DH DL DIGIT
	LCDB	M	I			1 1 0 0 0 1 DH DL DIGIT
	LCPA	M	I	Output segment pattern to LCD digit through LA	LCD (DIGIT) ← LA ← M	1 1 0 0 1 0 DH DL DIGIT
	LCPB	M	I			1 1 0 0 1 1 DH DL DIGIT
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0 0 0 0 0 0 0 0 0 1 0 0 I
	CKSTP			Clock stop	Stop x'tal OSC	0 0 0 0 0 0 0 0 0 1 0 1
	NOP			No operation	No operation	0 0 0 0 0 0 0 0 0 0 0 0