Ordering number : EN5608

CMOS LSI

LC72136N, 72136NM

PLL Frequency Synthesizer for Electronic Tuning

Overview

The LC72136N and LC72136NM are PLL frequency synthesizers for use in radio/cassette players. They allow high-performance AM/FM tuners to be implemented easily.

Features

- High-speed programmable frequency divider
  - — FMIN: 10 to 160 MHz.....Pulse swallower (divide-by-two prescaler built in)
  - — AMIN: 2 to 40 MHz.........Pulse swallower
    0.5 to 10 MHz......Direct division
- IF counter
  IFIN: 0.4 to 12 MHz................For use as an AM/FM IF counter
- Reference frequency
  - — Selectable from one of eight frequencies (crystal oscillator: 75 kHz)
    1, 3, 5, 3.125, 6.25, 12.5, 15, and 25 kHz
- Phase comparator
  - — Supports dead zone control
  - — Built-in unlock detection circuit
  - — Built-in deadlock clear circuit
- Built-in MOS transistor for forming an active low-pass filter
- I/O ports
  - — Dedicated output ports: 6
  - — I/O ports: 2
  - — Supports clock time base output
- Serial Data I/O
  - — Supports CCB format communication with the system controller.
- Operating ranges
  - — Supply voltage: 4.5 to 5.5 V
  - — Operating temperature: –20 to +70°C
- Packages
  —DIP22S/MFP24S

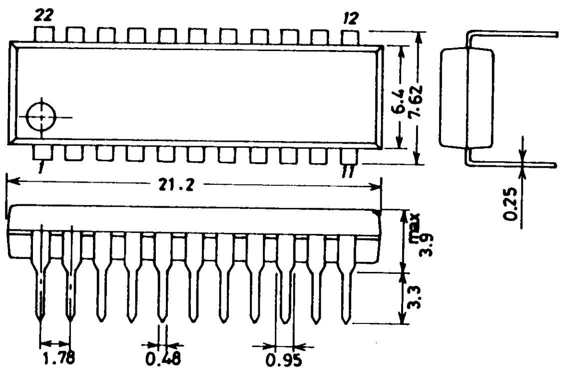
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

unit: mm

3059-DIP22S

[LC72136N]

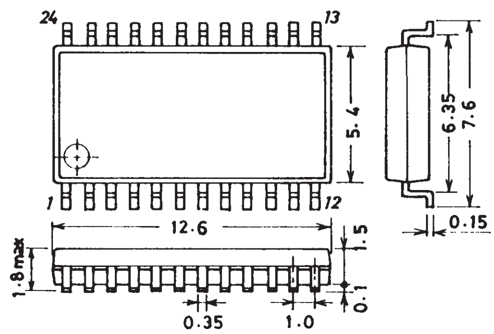


SANYO: DIP22S

unit: mm

3112-MFP24S

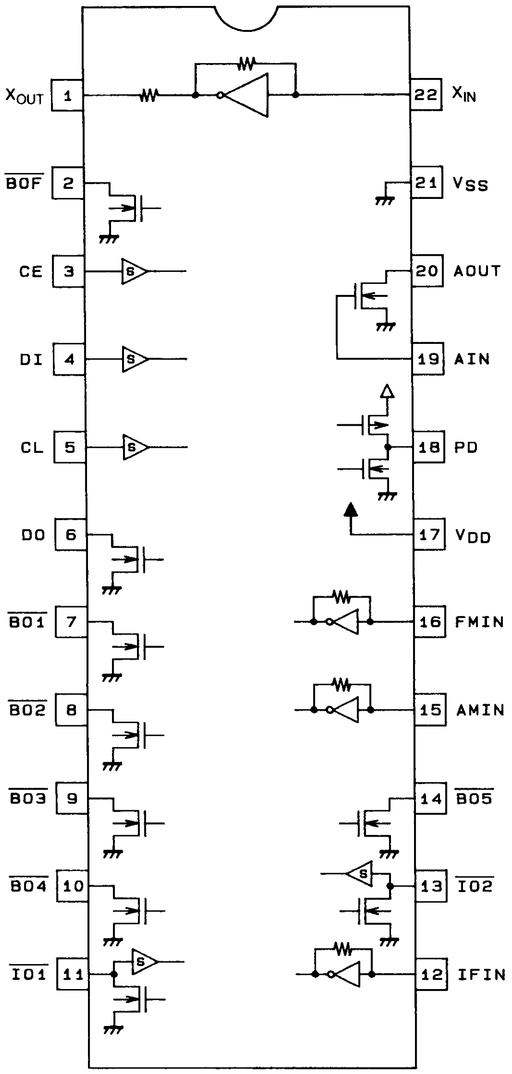
[LC72136NM]



SANYO: MFP24S

Pin Assignments

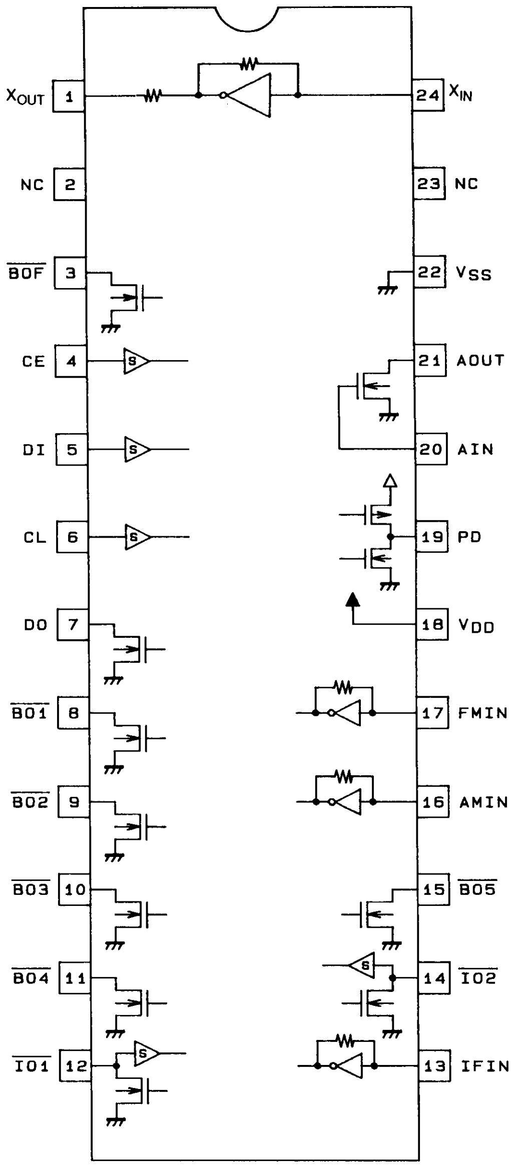
LC72136N



Top view

A04126

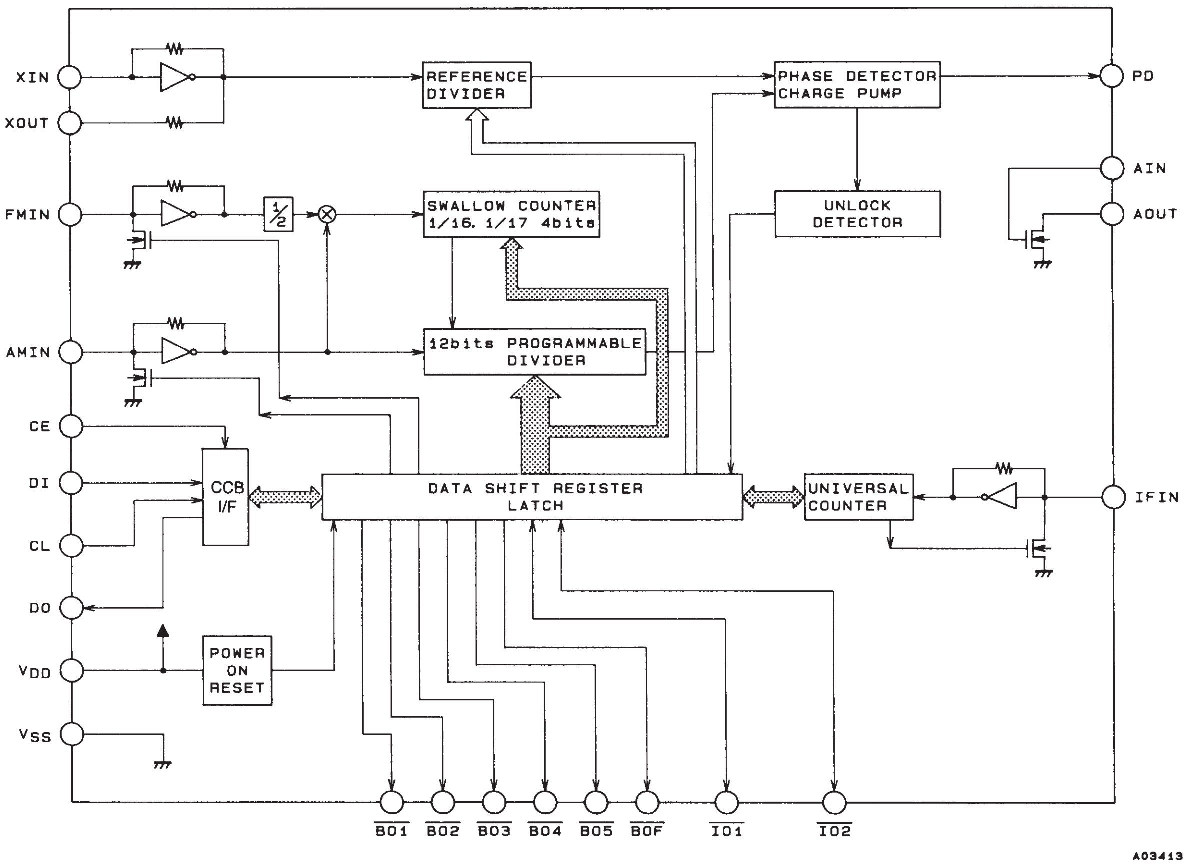
LC72136NM



Top view

A04127

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	V_{IN}1 max	CE, CL, DI, AIN	–0.3 to +7.0	V
	V_{IN}2 max	XIN, FMIN, AMIN, IFIN	–0.3 to V_{DD} + 0.3	V
	V_{IN}3 max	$\overline{IO1}$, $\overline{IO2}$	–0.3 to +15	V
Maximum output voltage	V_O1 max	DO	–0.3 to +7.0	V
	V_O2 max	XOUT, PD	–0.3 to V_{DD} + 0.3	V
	V_O3 max	$\overline{BO1}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$, AOUT	–0.3 to +15	V
Maximum output current	I_O1 max	$\overline{BO1}$	0 to 3.0	mA
	I_O2 max	AOUT, DO	0 to 6.0	mA
	I_O3 max	$\overline{BO2}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$	0 to 10.0	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C: LC72136N (DIP22S)	350	mW
		Ta ≤ 70°C: LC72136NM (MFP24S)	200	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

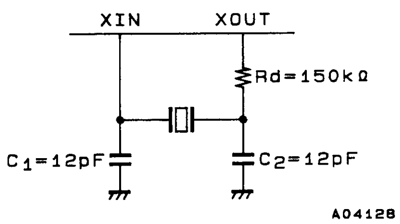
Allowable Operating Ranges at Ta = –20 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
Input high-level voltage	$V_{IH}1$	CE, CL, DI	0.7 V_{DD}		6.5	V
	$V_{IH}2$	$\overline{IO1}$, $\overline{IO2}$	0.7 V_{DD}		13	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$	0		0.3 V_{DD}	V
Output voltage	V_O1	DO	0		6.5	V
	V_O2	$\overline{BO1}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$, AOUT	0		13	V
Input frequency	$f_{IN}1$	XIN: $V_{IN}1$		75		kHz
	$f_{IN}2$	FMIN: $V_{IN}2$	10		160	MHz
	$f_{IN}3$	AMIN: $V_{IN}3$, SNS = 1	2		40	MHz
	$f_{IN}4$	AMIN: $V_{IN}4$, SNS = 0	0.5		10	MHz
	$f_{IN}5$	IFIN: $V_{IN}5$	0.4		12	MHz
Input amplitude	$V_{IN}1$	XIN: $f_{IN}1$	400		1500	mVrms
	$V_{IN}2$-1	FMIN: f = 10 to 130 MHz	40		1500	mVrms
	$V_{IN}2$-2	FMIN: f = 130 to 160 MHz	70		1500	mVrms
	$V_{IN}3$	AMIN: $f_{IN}3$, SNS = 1	40		1500	mVrms
	$V_{IN}4$	AMIN: $f_{IN}4$, SNS = 0	40		1500	mVrms
	$V_{IN}5$-1	IFIN: $f_{IN}5$, IFS = 1	40		1500	mVrms
	$V_{IN}5$-2	IFIN: $f_{IN}6$, IFS = 0	70		1500	mVrms
Guaranteed crystal oscillator frequency	Xtal	XIN, XOUT*		75		kHz

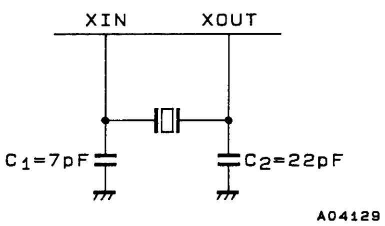
Note: * Crystal oscillator recommended CI value
CI ≤ 35 kΩ (for a 75 kHz crystal)
The circuit constants for the crystal oscillator circuit depend on the crystal used, the printed circuit board pattern, and other items. Therefore we recommend consulting with the manufacturer of the crystal for evaluation and reliability.
The extremely high input impedance of the XIN pins means that applications must take the possibility of leakage into account.

Sample Oscillator Circuits

1. Seiko-Epson C-2-75kHz (C_L = 11 pF)



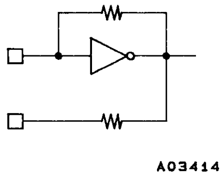
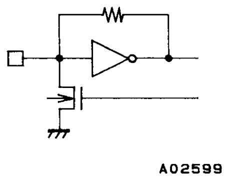
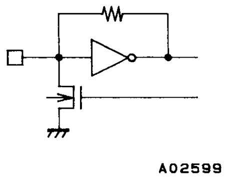
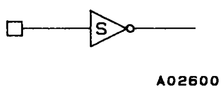
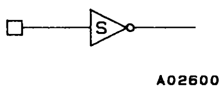
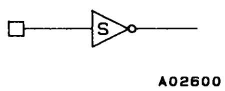
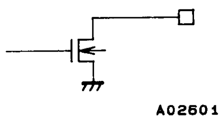
2. Kyocera Corporation KF-38R5-09P0300 (C_L = 9 pF)



Electrical Characteristics at Ta = –20 to +70°C, V_{SS} = 0 V

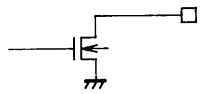
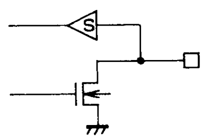
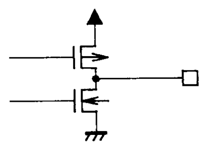
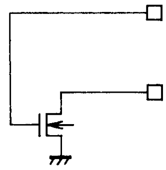
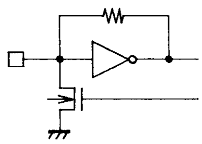
Parameter	Symbol	Conditions	min	typ	max	Unit
Internal feedback resistors	Rf1	XIN		8.0		MΩ
	Rf2	FMIN		500		kΩ
	Rf3	AMIN		500		kΩ
	Rf4	IFIN		250		kΩ
Internal pull-down resistors	Rpd1	FMIN		200		kΩ
	Rpd2	AMIN		200		kΩ
Internal output resistor	Rd	XOUT		250		kΩ
Hysteresis	V_{HIS}	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$		0.1 V_{DD}		V
Output high-level voltage	$V_{OH}1$	PD: I_O = –1 mA	V_{DD} – 1.0			V
Output low-level voltage	$V_{OL}1$	PD: I_O = 1 mA			1.0	V
	$V_{OL}2$	$\overline{BO1}$: I_O = 0.5 mA			0.5	V
		$\overline{BO1}$: I_O = 1 mA			1.0	V
	$V_{OL}3$	DO: I_O = 1 mA			0.2	V
		DO: I_O = 5 mA			1.0	V
	$V_{OL}4$	$\overline{BO2}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$: I_O = 1 mA			0.2	V
		$\overline{BO2}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$: I_O = 5 mA			1.0	V
		$\overline{BO2}$ to $\overline{BO5}$, $\overline{BOF}$, $\overline{IO1}$, $\overline{IO2}$: I_O = 8 mA			1.6	V
	$V_{OL}5$	AOUT: I_O = 1 mA, AIN = 1.3 V			0.5	V
Input high-level voltage	$I_{IH}1$	CE, CL, DI: V_I = 6.5 V			5.0	µA
	$I_{IH}2$	$\overline{IO1}$, $\overline{IO2}$: V_I = 13 V			5.0	µA
	$I_{IH}3$	XIN: V_I = V_{DD}	0.3	0.6	1.4	µA
	$I_{IH}4$	FMIN, AMIN: V_I = V_{DD}	4.0		22	µA
	$I_{IH}5$	IFIN: V_I = V_{DD}	8.0		44	µA
	$I_{IH}6$	AIN: V_I = 6.5 V			200	nA
Input low-level current	$I_{IL}1$	CE, CL, DI: V_I = 0 V			5.0	µA
	$I_{IL}2$	$\overline{IO1}$, $\overline{IO2}$: V_I = 0 V			5.0	µA
	$I_{IL}3$	XIN: V_I = 0 V	0.3	0.6	1.4	µA
	$I_{IL}4$	FMIN, AMIN: V_I = 0 V	4.0		22	µA
	$I_{IL}5$	IFIN: V_I = 0 V	8.0		44	µA
	$I_{IL}6$	AIN: V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	$\overline{BO1}$ to $\overline{BO5}$, $\overline{BOF}$, AOUT, $\overline{IO1}$, $\overline{IO2}$: V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO: V_O = 6.5 V			5.0	µA
High-level tree-state off leakage current	I_{OFFH}	PD: V_O = V_{DD}		0.01	200	nA
Low-level tree-state off leakage current	I_{OFFL}	PD: V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN		6		pF
Current drain	$I_{DD}1$	V_{DD}: Xtal = 75 kHz, $f_{IN}2$ = 130 MHz, $V_{IN}2$ = 40 mVrms		5	10	mA
	$I_{DD}2$	V_{DD}: PLL block stopped (PLL inhibit), Xtal oscillator operating (Xtal = 75 kHz)		0.1		mA
	$I_{DD}3$	V_{DD}: PLL block stopped, Xtal oscillator stopped			10	µA

Pin Functions

Symbol	Pin No. (MFP pin numbers are in parentheses.)	Type	Functions	Circuit configuration
XIN XOUT	22 (24) 1 (1)	Xtal	• Crystal oscillator connections (75 kHz) • The extremely high input impedance of the XIN pins means that applications must take the possibility of leakage into account.	
FMIN	16 (17)	Local oscillator signal input	• FMIN is selected when the serial data input DVS bit is set to 1. • The input frequency range is from 10 to 160 MHz. • The input signal passes through the internal divide-by-two prescaler and is input to the swallow counter. • The divisor can be in the range 272 to 65535. However, since the signal has passed through the divide-by-two prescaler, the actual divisor is twice the set value.	
AMIN	15 (16)	Local oscillator signal input	• AMIN is selected when the serial data input DVS bit is set to 0. • When the serial data input SNS bit is set to 1: — The input frequency range is 2 to 40 MHz. — The signal is directly input to the swallow counter. — The divisor can be in the range 272 to 65535, and the divisor used will be the value set. • When the serial data input SNS bit is set to 0: — The input frequency range is 0.5 to 10 MHz. — The signal is directly input to a 12-bit programmable divider. — The divisor can be in the range 4 to 4095, and the divisor used will be the value set.	
CE	3 (4)	Chip enable	• Set this pin high when inputting (DI) or outputting (DO) serial data.	
CL	5 (6)	Clock	• Used as the synchronization clock when inputting (DI) or outputting (DO) serial data.	
DI	4 (5)	Input data	• Inputs serial data transferred from the controller to the LC72136N.	
DO	6 (7)	Output data	• Outputs serial data transferred from the LC72136N to the controller. The data output is determined by the DOC0 to DOC2 bits in the serial data.	
V_{DD}	17 (18)	Power supply	• The LC72136N power supply pin. (V_{DD} = 4.5 to 5.5 V) • The power on reset circuit operates when power is first applied.	
V_{SS}	21 (22)	Ground	• The LC72136N ground	

Continued on next page.

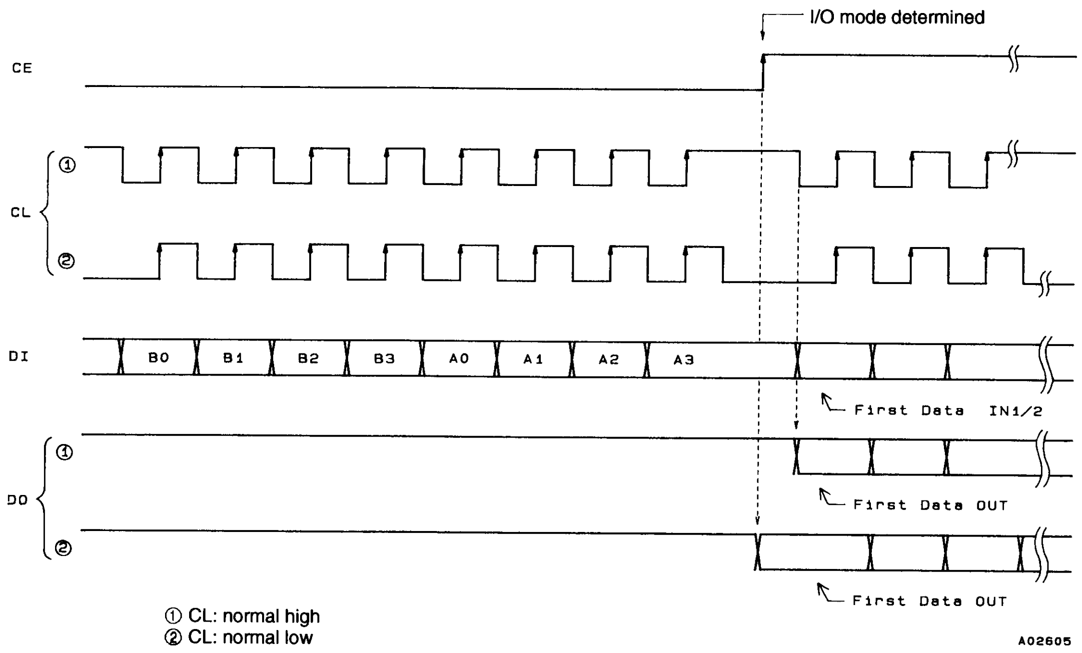
Continued from preceding page.

Symbol	Pin No. (MFP pin numbers are in parentheses.)	Type	Functions	Circuit configuration
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$ $\overline{BO5}$ $\overline{BOF}$	7 (8) 8 (9) 9 (10) 10 (11) 14 (15) 2 (3)	Output ports	• Dedicated outputs • The output states are determined by the BO1 to BO5 bits in the serial data. Data: 0 = open, 1= low • A time base signal (8 Hz) can be output from the $\overline{BO1}$ pin. (When the serial data TBC bit is set to 1.) • Care is required when using the $\overline{BO1}$ pin, since it has a higher on impedance that the other output ports (pins $\overline{BO2}$ to $\overline{BO5}$). • The output state of the $\overline{BOF}$ pin is determined by the serial data DVS bit. Thus this pin can be used as an FM band selection switch. (Note that it should not be used as an AM band selection switch since it is susceptible to noise from the crystal oscillator.) DVS data: 0 = open, 1 = low • All output ports are set to the open state following a power on reset.	 A02601
$\overline{IO1}$ $\overline{IO2}$	11 (12) 13 (14)	Input or output ports	• I/O dual-use pins • The direction (input or output) is determined by bits IOC1 and IOC2 in the serial data. Data: 0 = input port, 1 = output port • When specified for use as input ports: The state of the input pin is transmitted to the controller over the DO pin. Input state: low = 0 data value high = 1 data value • When specified for use as output ports: The output states are determined by the IO1 and IO2 bits in the serial data. Data: 0 = open, 1 = low • These pins function as input pins following a power on reset.	 A02602
PD	18 (19)	Charge pump output	• PLL charge pump output When the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high-impedance state when the frequencies match.	 A02603
AIN AOUT	19 (20) 20 (21)	LPF amplifier transistor connections	• The n-channel MOS transistor used for the PLL active low-pass filter.	 A02604
IFIN	12 (13)	IF counter	• Accepts an input in the frequency range 0.4 to 12 MHz. • The input signal is directly transmitted to the IF counter. • The result is output starting the MSB of the IF counter using the DO pin. • Four measurement periods are supported: 4, 8, 32, and 64 ms.	 A02599

Serial Data I/O Procedures

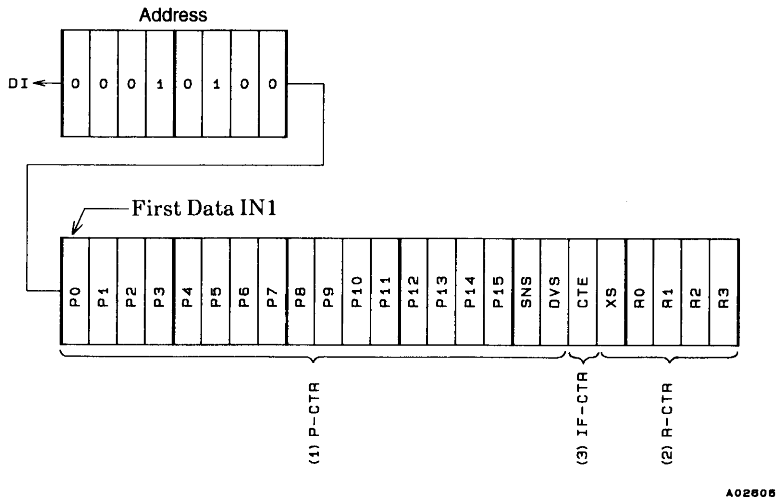
The LC72136N inputs and outputs data using the Sanyo CCB (computer control bus) audio LSI serial bus format. This LSI adopts an 8-bit address format CCB.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
3	OUT (A2)	0	1	0	1	0	1	0	0	• Data output mode (serial data output) • The number of bits output is equal to the number of clock cycles. • See the “DO Output Data (Serial Data Output) Structure” item for details on the meaning of the output data.

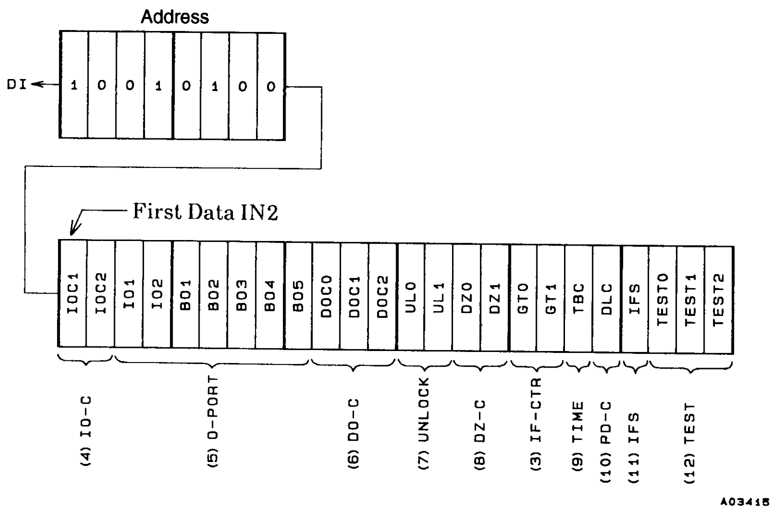


DI Control Data (serial data input) Structure

1. IN1 Mode



2. IN2 Mode



DI Control Data Functions

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15

DVS, SNS</td><td>
• Data that sets the programmable divider
A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS.
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr>
</table>
Note: P0 to P3 are ignored when P4 is the LSB.
• Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the frequency range, and determines the BOF pin output state. (*: Don’t care.)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th><th>BOF pin</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160 MHz</td><td>Low</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td><td>Open</td></tr>
</table>
Note: See the “Programmable Divider” item for details.
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data
R0 to R3

XS</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + Xtal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
Note: PLL INHIBIT
The programmable divider and IF counter blocks are stopped, the FMIN, AMIN, and IFIN pins go to the pulled-down state, and the charge pump output pin goes to the high-impedance state.
• Oscillator margin selection data
XS = 0: “Reduction mode” The oscillator margin is reduced and the crystal radiation is reduced.
XS = 1: Normal mode.
Normal mode is selected following a power-on reset.
</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data
CTE

GT0, GT1</td><td>
• IF counter measurement start specification
CTE = 1: Counter start
CTE = 0: Counter reset
• IF counter measurement time determination
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
Note: See the “IF Counter Structure” item for details.
</td><td>IFS</td></tr>
<tr><td>(4)</td><td>I/O port specification data
IOC1, IOC2</td><td>• Data that specifies input or output for the I/O dual-use pins
Data: 0 = input mode, 1 = output mode</td><td></td></tr>
<tr><td>(5)</td><td>Output port data
BO1 to BO5, IO1, IO2</td><td>• BO1 to BO5, IO1, and IO2 output state data
Data: 0 = open, 1 = low
• “Data = 0: Open” is selected following a power-on reset.</td><td>IOC1
IOC2</td></tr>
</table>

Continued on next page.

Continued from preceding page.

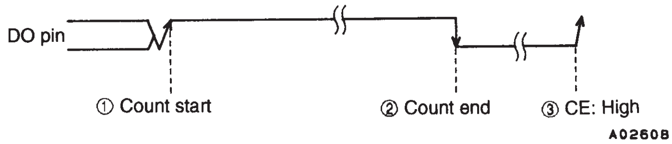
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>DO pin control data
DOC0, DOC1, DOC2</td><td>

• Data that determines DO pin output

<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC*1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The $\overline{IO1}$ pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The $\overline{IO2}$ pin state*2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>

The open state is selected following a power-on reset.

Note: 1. end-UC: IF counter measurement completion check



① When end-UC is set and an IF count is started (CTE = 0 → 1), the DO pin automatically goes to the open state.
② When the IF count measurement completes, the DO pin goes low and the count completion check operation is enabled.
③ The DO pin goes to the open state due to serial data I/O (CE: high).

2. Goes to the open state if the IO pin itself is set to be an output port.

Caution: The DO pin always goes to the open state during the data input period (during the period when CE is high in mode IN1 or IN2), regardless of the values of the DO pin control data (DOC0 to DOC2). Also, the DO pin outputs the content of the internal DO serial data in synchronization with the CL pin signal during the data output period (during the period when CE is high in the OUT mode) regardless of the values of the DO pin control data (DOC0 to DOC2).

</td><td>UL0, UL1,
CTE,
IOC1, IOC2</td></tr>
<tr><td>(7)</td><td>Unlock detection data
UL0, UL1</td><td>

• Selects the phase error (øE) detection range for PLL lock discrimination. When a phase error greater than the specified range occurs, the LC72136N determines that the PLL is unlocked. (*: Don't care.)

<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detector output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>*</td><td>±6.67 µs</td><td>øE is extended by 1 to 2 ms</td></tr>
</table>

Note: When unlocked, the DO pin goes low and the serial data output UL bit is 0.

</td><td>DOC0,
DOC1,
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data
DZ0, DZ1</td><td>

• Phase comparator dead zone control data

<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>

Dead zone width: DZA < DZB < DZC < DZD

</td><td></td></tr>
<tr><td>(9)</td><td>Clock time base
TBC</td><td>• An 8 Hz 40% duty clock time base signal can be output from $\overline{BO1}$ by setting TBC to 1. (The BO1 data will be ignored.)</td><td>BO1</td></tr>
<tr><td>(10)</td><td>Charge pump control data
DLC</td><td>

• Data that forcibly controls the charge pump output

<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced low</td></tr>
</table>

Note: The LC72136N provides a technique for escaping from deadlock by setting Vtune to V_{CC} (deadlock clearing circuit). This is used when the circuit is deadlocked due to the VCO oscillator being stopped by the VCO control voltage (Vtune) being 0 V.

This function goes to the forced low state (DLC = 1) following a power on reset.
The crystal oscillator circuit must be operating normally before this data is changed to return to the normal operating (DLC = 0) state.

</td><td></td></tr>
</table>

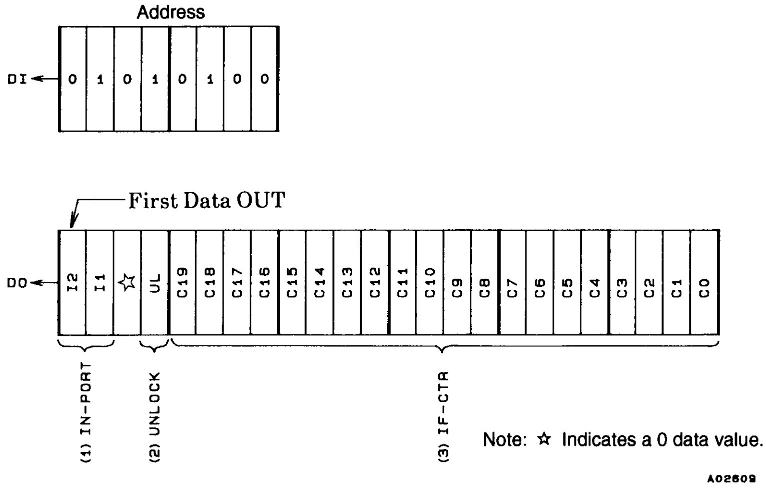
Continued on next page.

Continued from preceding page.

No.	Control block/data	Description	Related data
(11)	IF counter control data IFS	• This data should be set to 1 in normal operation. Setting this data to 0 switches the LC72136N to a reduced input sensitivity mode in which the sensitivity is reduced by 10 to 30 mVrms. * See the “IF Counter Operation” item for details.	
(12)	LSI test data TEST 0 to TEST3	• LSI test data TEST0, TEST1, TEST2: All three bits must be set to 0. All the test data is set to 0 following a power-on reset.	

DO Output Data (Serial Data Output) Structure

3. OUT mode

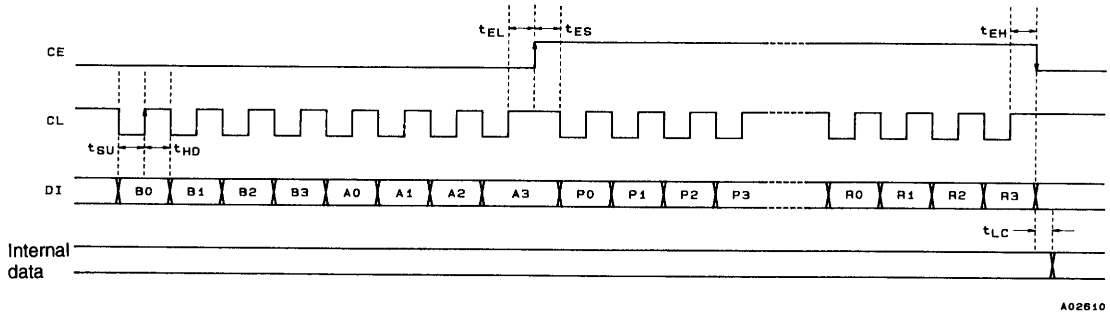


DO Output Data

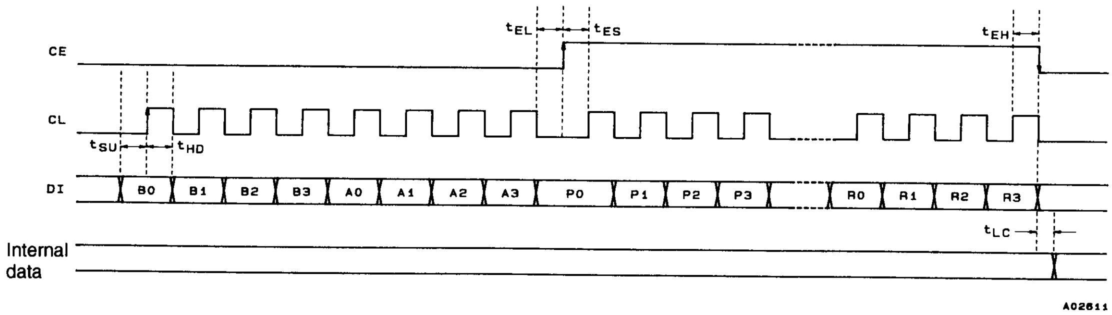
No.	Control block/data	Description	Related data
(1)	I/O port data I2, I1	• Data latched from the states of the I/O ports, pins $\overline{IO1}$ and $\overline{IO2}$. This data reflects the pin states, regardless of whether they are in input or output mode. The data is latched when OUT mode is selected. I1 ← $\overline{IO1}$ pin state, I2 ← $\overline{IO2}$ pin state: High: 1, Low: 0	IOC1, IOC2
(2)	PLL unlock data UL	• Data latched from the state of the unlock detection circuit UL ← 0: Unlocked UL ← 1: Locked or in detection stopped mode	UL0, UL1
(3)	IF counter binary data C19 to C0	• Data latched from the state of the IF counter, which is a 20-bit binary counter. C19 ← Binary counter MSB C0 ← Binary counter LSB	CTE, GT0, GT1

Serial Data Input (IN1/IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH}, ≥ 0.75 µs t_{LC} < 0.75 µs

1. CL: Normal high

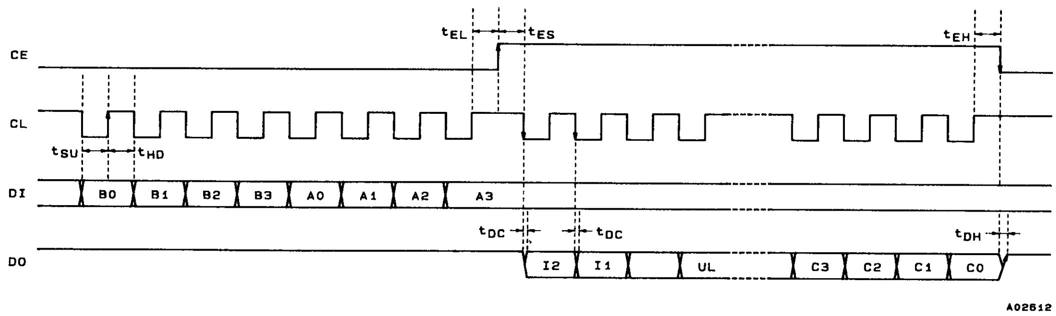


2. CL: Normal low

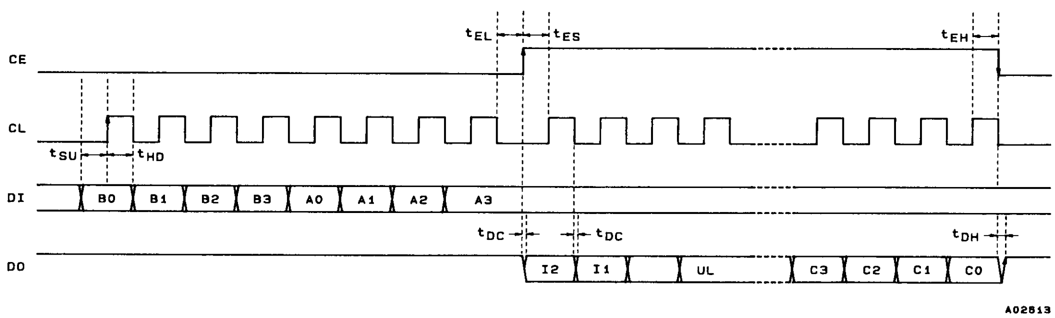


Serial Data Output (OUT) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH}, ≥ 0.75 µs t_{DC}, t_{DH} < 0.35 µs

1. CL: Normal high

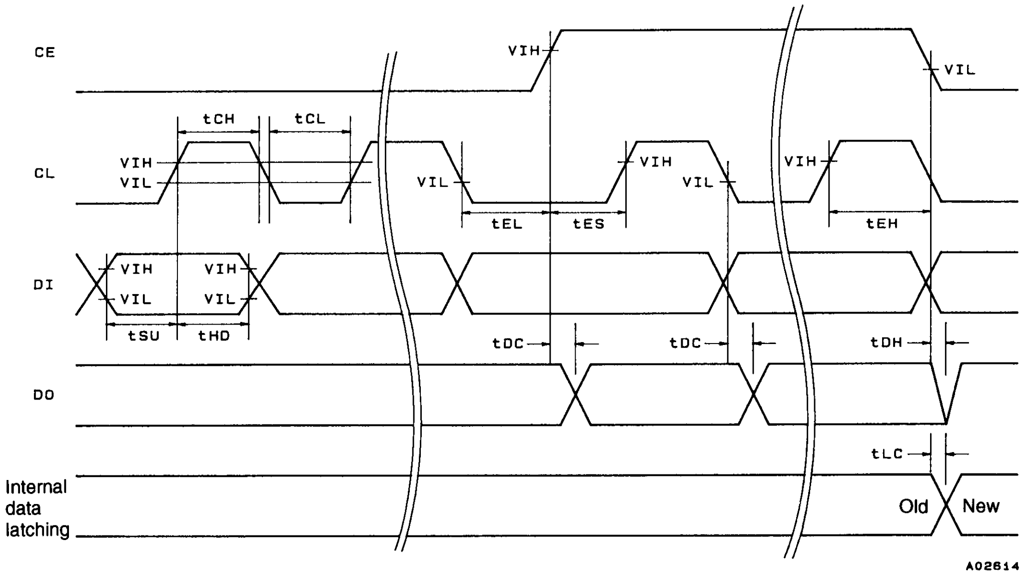


2. CL: Normal low

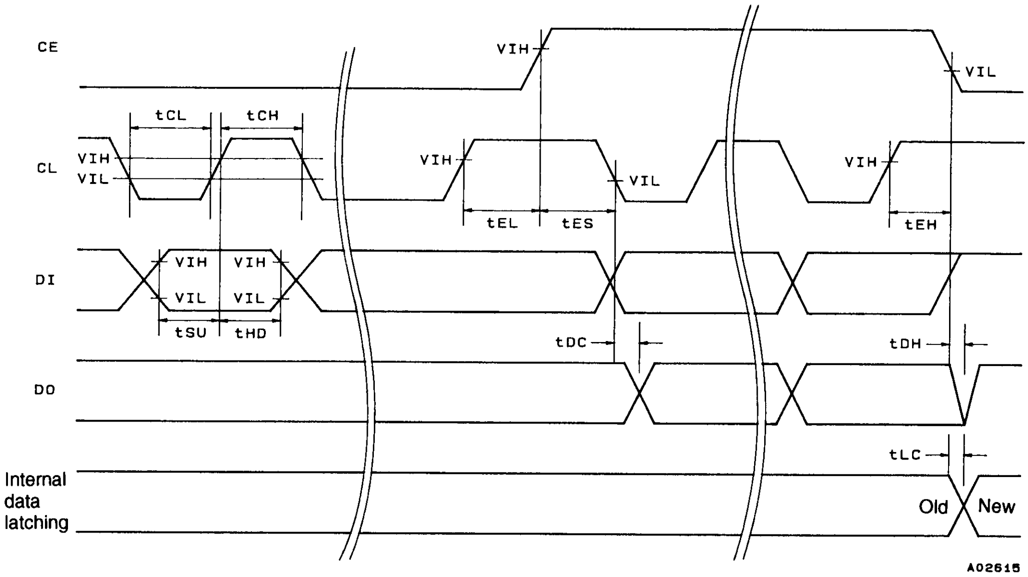


Note: Since the DO pin is an n-channel open drain circuit, the times for the data to change (t_{DC} and t_{DH}) will differ depending on the value of the pull-up resistor, printed circuit board capacitance.

Serial Data Timing



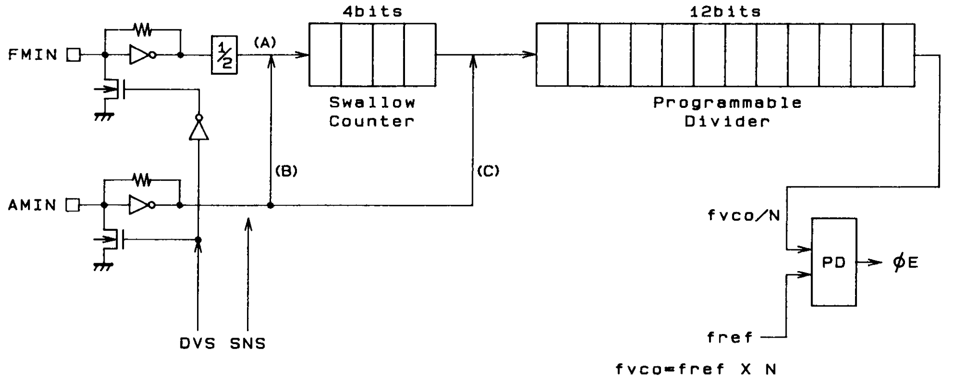
CL Stopped at the Low Level



CL Stopped at the High Level

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Data setup time	t_{SU}	DI, CL		0.75			µs
Data hold time	t_{HD}	DI, CL		0.75			µs
Clock low-level time	t_{CL}	CL		0.75			µs
Clock high-level time	t_{CH}	CL		0.75			µs
CE wait time	t_{EL}	CE, CL		0.75			µs
CE setup time	t_{ES}	CE, CL		0.75			µs
CE hold time	t_{EH}	CE, CL		0.75			µs
Data latch change time	t_{LC}					0.75	µs
Data output time	t_{DC}	DO, CL	These times depend on the pull-up resistance and the printed circuit board capacitances.			0.35	µs
	t_{DH}	DO, CE				0.35	µs

Programmable Divider Structure



A02616

	DVS	SNS	Input pin	Set divisor	Actual divisor: N	Input frequency range (MHz)
A	1	*	FMIN	272 to 65535	Twice the set value	10 to 160
B	0	1	AMIN	272 to 65535	The set value	2 to 40
C	0	0	AMIN	4 to 4095	The set value	0.5 to 10

Note: * Don't care.

Sample Programmable Divider Divisor Calculations

1. For a 50 kHz FM step size (DVS = 1, SNS = *: FMIN selected)
   - FM RF = 90.0 MHz (IF = +10.7 MHz)
     FM VCO = 100.7 MHz
     PLL fref = 25 kHz (R0 to R1 = 1, R2 to R3 = 0)
     100.7 MHz (FM VCO) ÷ 25 kHz (fref) ÷ 2 (FMIN: divide-by-two prescaler) = 2014 → 07DE (HEX)

E				D				7				0											
0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	*	1			1	1	0	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A02617

2. For a 5 kHz SW step size (DVS = 0, SNS = 1: AMIN high-speed side selected)
   - SW RF = 21.75 MHz (IF = +450 kHz)
     SW VCO = 22.20 MHz
     PLL fref = 5 kHz (R0 = R2 = 0, R1 = R3 = 1)
     22.2 MHz (SW VCO) ÷ 5 kHz (fref) = 4440 → 1158 (HEX)

8				5				1				1											
0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0			0	1	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A02618

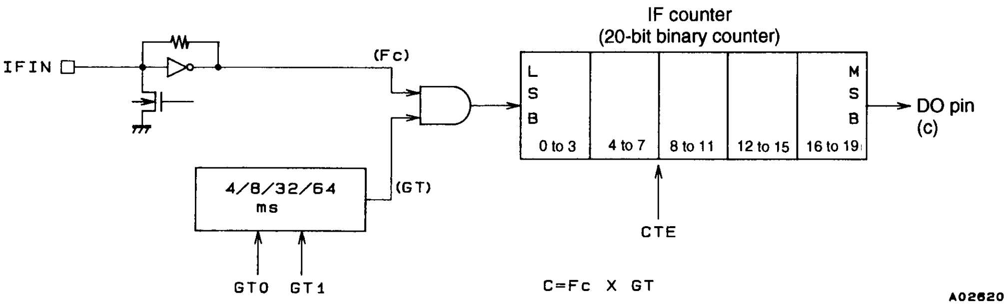
3. For a 9 kHz MW step size (DVS = 0, SNS = 0: AMIN low-speed side selected)
   - MW RF = 1008 kHz (IF = +450 kHz)
     MW VCO = 1458 kHz
     PLL fref = 3 kHz (R0 to R1 = 0, R2 to R3 = 1): using a 3 kHz reference frequency
     1458 kHz (MW VCO) ÷ 3 kHz (fref) = 486 → 1E6 (HEX)

				6				E				1											
*	*	*	*	0	1	1	0	0	1	1	1	1	0	0	0	0	0			0	0	1	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

A03416

IF Counter Structure

The LC72136N IF counter is a 20-bit binary counter. The result of the count can be read out serially, MSB first, from the DO pin.



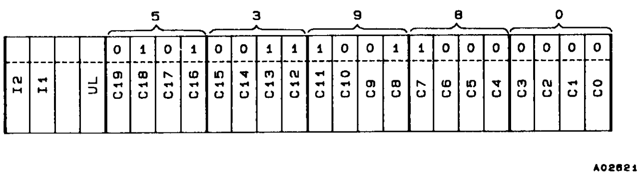
GT1	GT0	Measurement time	
		Measurement period (GT) (ms)	Wait time (t_{WU}) (ms)
0	0	4	3 to 4
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

IF frequency (Fc) measurement consists of determining how many pulses enter the IF counter in a specified measurement time (GT).

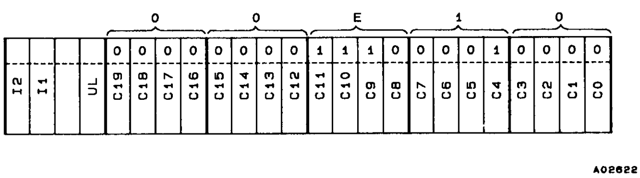
$Fc = \frac{C}{GT}$ (C = Fc × GT) C: count value (number of pulses)

Sample IF Counter Frequency Calculations

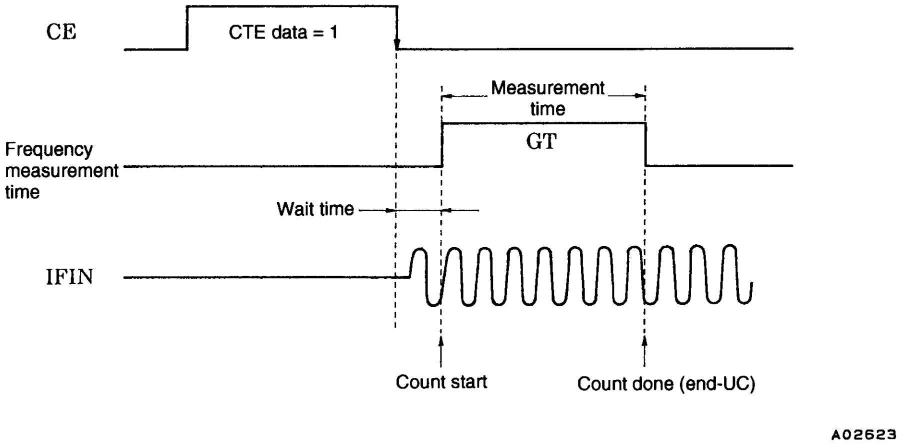
1. For a measurement time (GT) of 32 ms and a count value (C) of 53980 (hexadecimal), which is 342,400 (decimal)
   IF frequency (Fc) = 342,400 ÷ 32 ms = 10.7 MHz



2. For a measurement time (GT) of 8 ms and a count value (C) of E10 (hexadecimal), which is 3600 (decimal)
   IF frequency (Fc) = 3600 ÷ 8 ms = 450 kHz



IF Counter Operation



Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0. The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the LC72136N when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF count at the end of the measurement period must be read out during the period CTE is 1. This is because the IF counter is reset when CTE is set to 0.

Note: When operating the IF counter, the control microprocessor must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output and execute an IF count operation. Auto-search techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

IFIN Minimum Sensitivity Ratings

f (MHz)

IFS	$0.4 \leq f < 0.5$	$0.5 \leq f < 8$	$8 \leq f \leq 12$
1: Normal mode	40 mVrms (0.1 to 3 mVrms)	40 mVrms	40 mVrms (1 to 10 mVrms)
0: Degradation mode	70 mVrms (10 to 15 mVrms)	70 mVrms	70 mVrms (30 to 40 mVrms)

Note: Values in parentheses are actual performance values presented as reference data.

Unlock Detection Timing

1. Unlock Detection Determination Timing
   Unlock detection is performed in the reference frequency (fref) period (interval). Therefore, in principle, unlock determination requires a time longer than the period of the reference frequency. However, immediately after changing the divisor N (frequency) unlock detection must be performed after waiting at least two periods of the reference frequency.

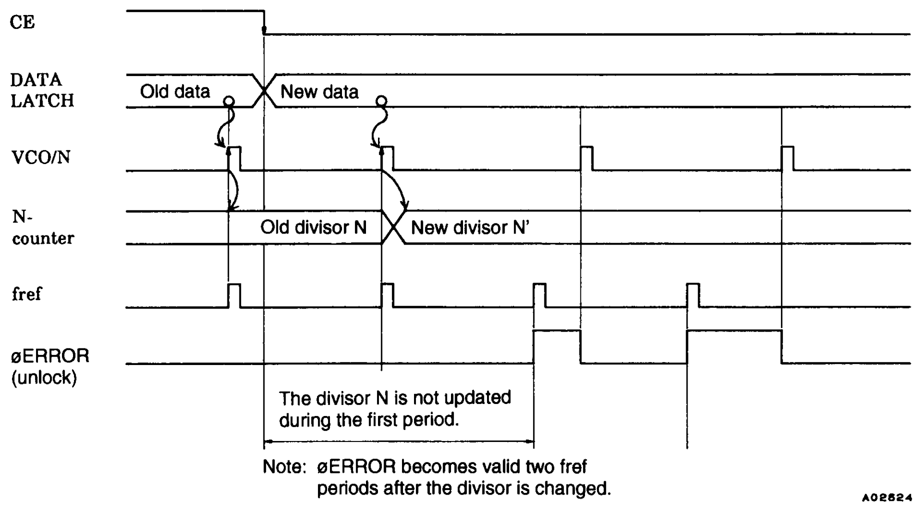


Figure 1 Unlock Detection Timing

For example, if fref is 1 kHz (and thus the period is 1 ms), after changing the divisor N, the system must wait at least 2 ms before checking for the unlocked state.

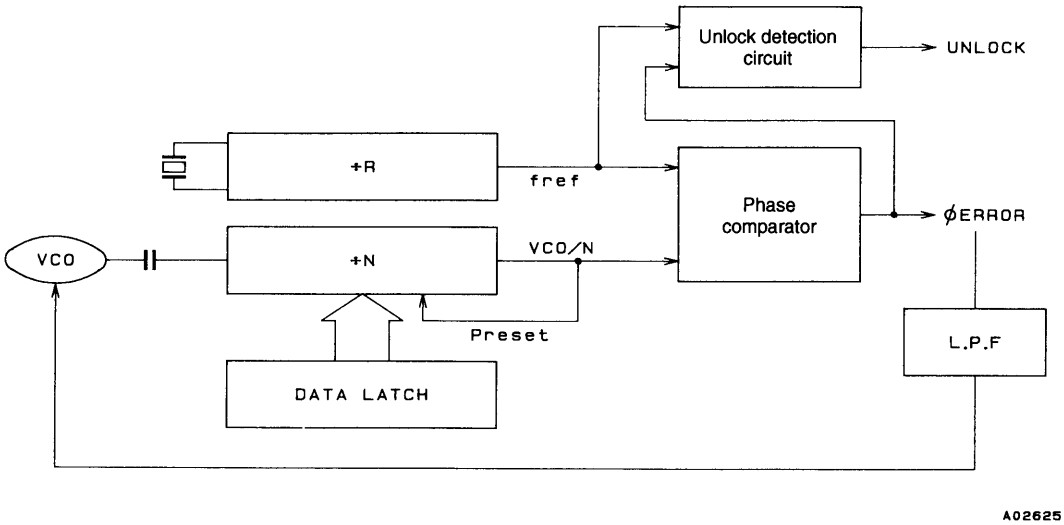


Figure 2 Circuit Structure

2. Unlock Detection Software

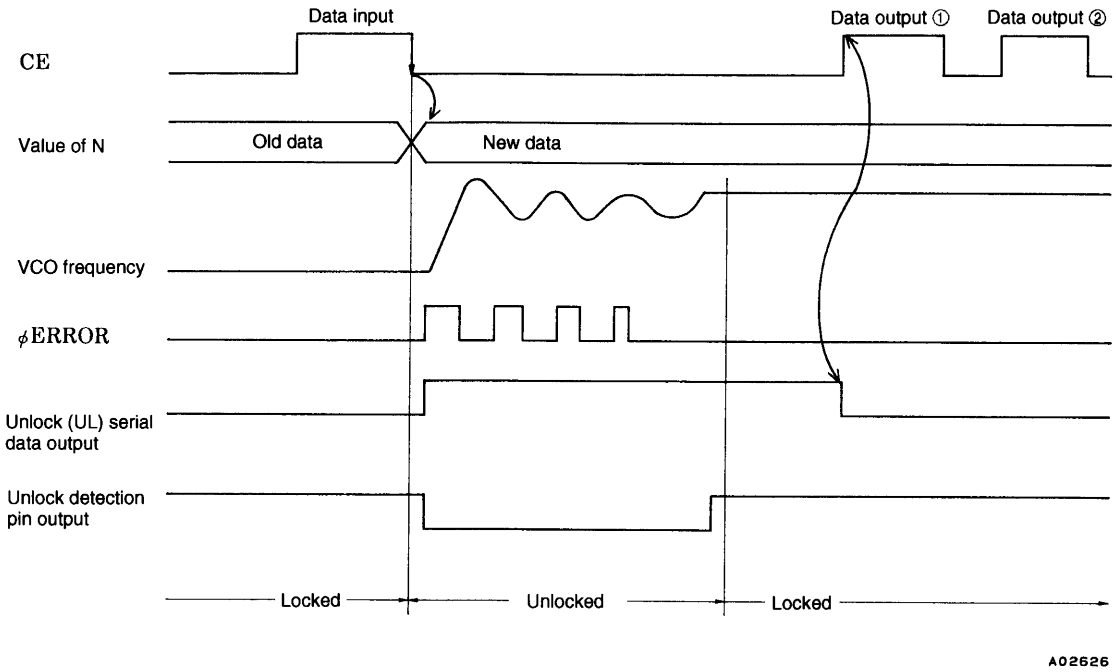
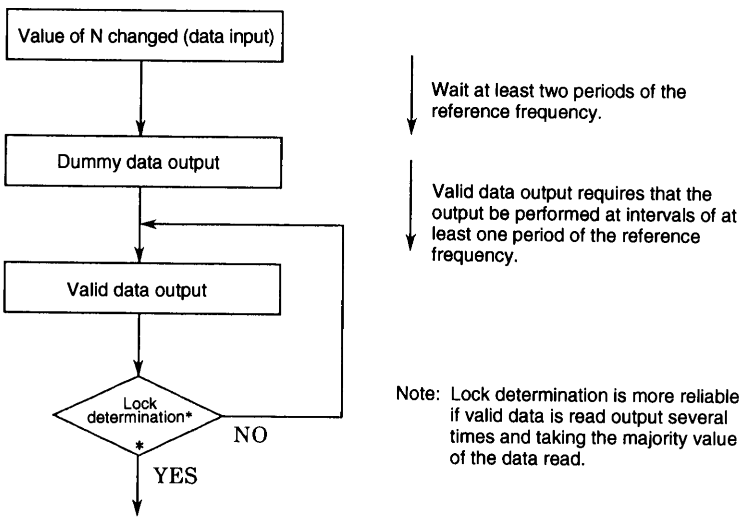


Figure 3

3. When Outputting Unlock Data Using Serial Data Output:
Once the LC72136N detects an unlocked state, it does not reset the unlock data (UL) until the next data output (or data input) operation is performed. At the data output ① point in Figure 3, although the VCO frequency is stable (locked), the unlock data remains set to the unlocked state since no data output has been performed since the value of N was changed. Thus, even though the frequency became stable (locked), from the point of view of the data, the circuit is in the unlocked state. Therefore, the data output ① immediately following a change to the value of N should be seen as a dummy data, and the data from the second data output (data output ②) and later outputs should be seen as valid data.



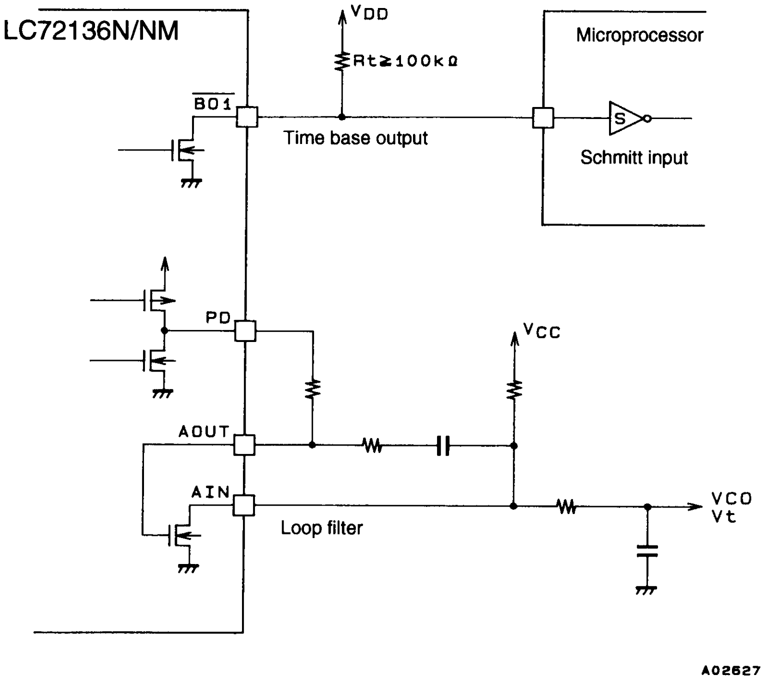
Lock Determination Flowchart

When directly outputting data from the DO pin (set up by the DO pin control data)

Since the DO pin outputs the unlocked state (locked: high, unlocked: low) the timing considerations in the technique described in the previous section are not necessary. After changing the value of N, the locked state can be determined after waiting at least two periods of the reference frequency.

Notes on Clock Time Base Usage

When the clock time base output is used, the value of the pull-up resistor for the output pin ($\overline{\text{BO1}}$) must be at least 100 kΩ. This is to avoid degradation of the VCO C/N characteristics when using the built-in low-pass filter transistor to form the loop filter. Since the clock time base output pin and the low-pass filter transistor ground are the same node in the IC, the time base output pin current fluctuations must be suppressed to limit the influence on the low-pass filter. We recommend the use of a Schmitt input on the receiving controller (microprocessor) to prevent chattering.



Other Items

1. Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead-zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	– –0 sec
0	1	DZB	ON/ON	–0 sec
1	0	DZC	OFF/OFF	+0 sec
1	1	DZD	OFF/OFF	+ +0 sec

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/R ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

Dead Zone

The phase comparator compares fp to a reference frequency (fr) as shown in Figure 4. Although the characteristics of this circuit (see Figure 5) are such that the output voltage is proportional to the phase difference ø (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.
However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

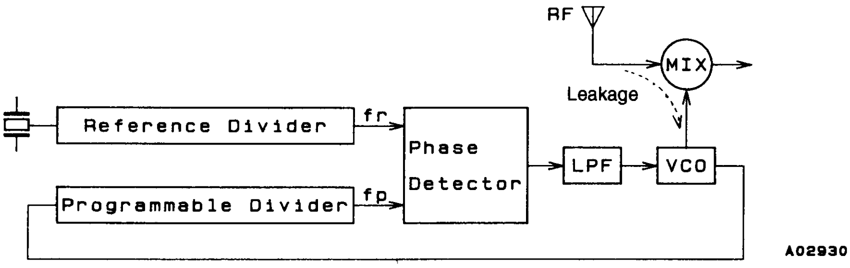


Figure 4

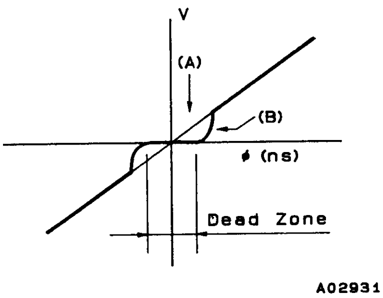


Figure 5

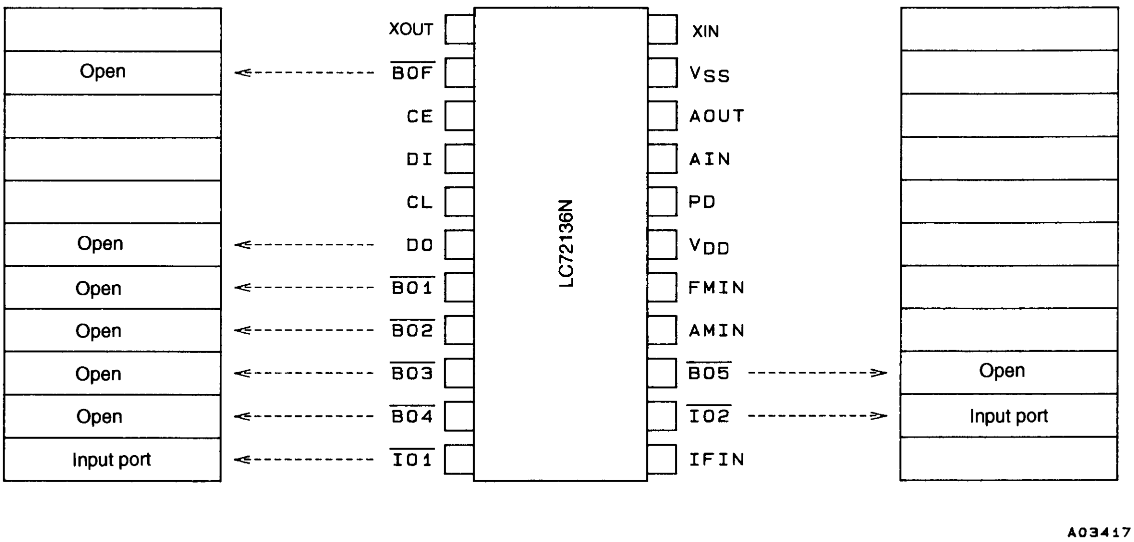
2. Notes on the FMIN, AMIN, and IFIN Pins
   Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100 pF is desirable. In particular, if a capacitance of 1000 pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

3. Notes on IF Counting → SD must be used in conjunction with the IF counting time
   When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can stop at points where there is no signal due to leakage output from the IF counter buffer.

4. DO Pin Usage Techniques
   In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

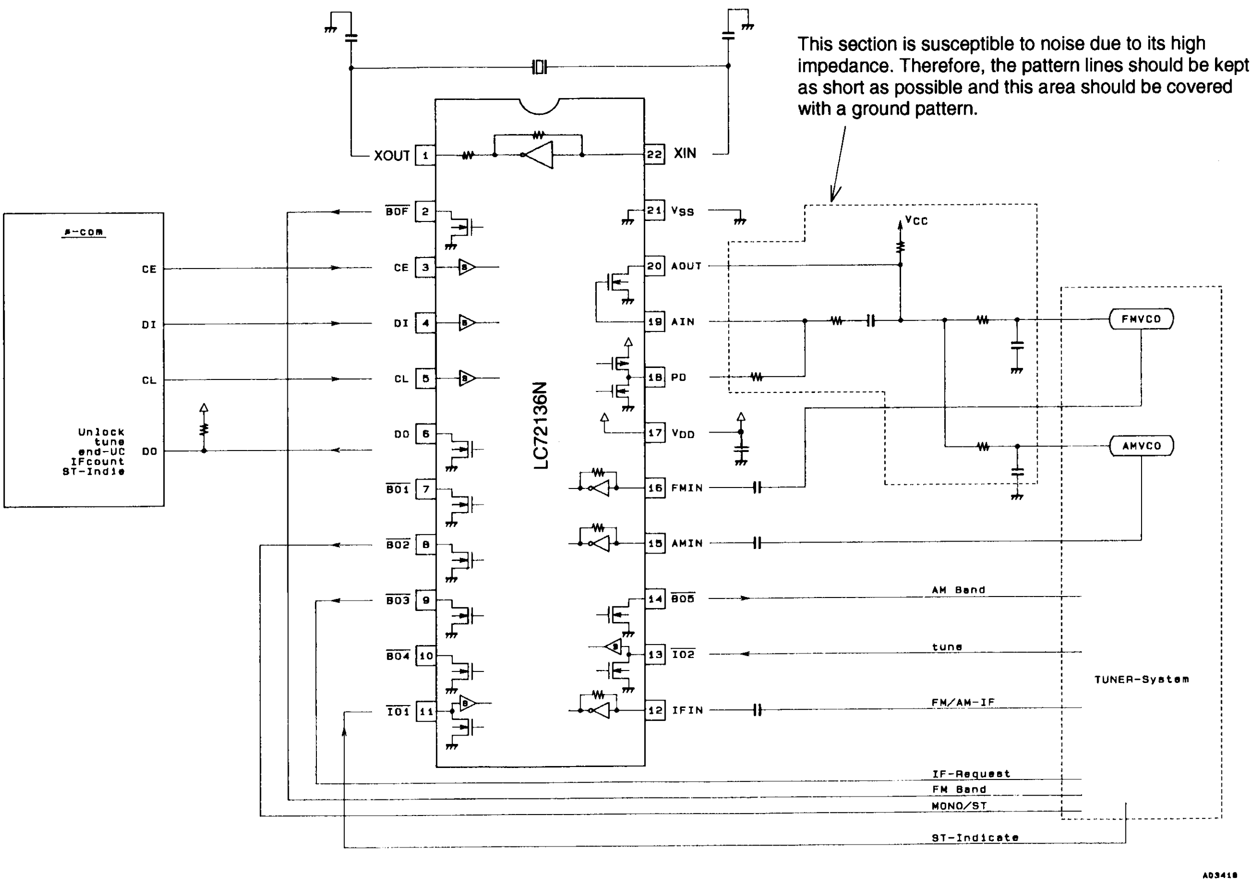
5. Power Supply Pins
   A capacitor of at least 2000 pF must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. This capacitor must be placed as close as possible to the V_{DD} and V_{SS} pins.

Pin States Following a Power-On Reset



Sample Application System

(Using the DIP22S package)



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
  ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
  ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of November, 1996. Specifications and information herein are subject to change without notice.