



# LC7152, 7152M, 7152NM, 7152KM

## Universal Dual-PLL Frequency Synthesizers



### Overview

The LC7152, 7152M, 7152NM, 7152KM are universal dual-PLL frequency synthesizers for use in weak signal type cordless telephone applications in the USA, South Korea, and Japan, and broadcast satellite (BS) tuners in the USA and Europe.

### Features

- Dual charge pump built in for fast channel switching
- Digital lock detector enables PLL lock status check with crystal oscillator precision
- Programmable reference frequency divider supports various applications
- The LC7152NM is a built-in power-on reset circuit version of the LC7152M
- The LC7152KM is an enhanced frequency characteristics version of the LC7152M

### Functions

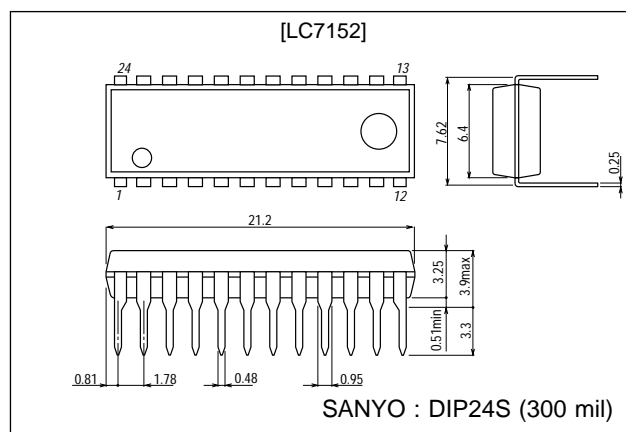
- 2-system PLL built-in (dual PLL)
- 16-bit programmable local-oscillator divider 1.5 to 55 MHz ( $V_{DD} = 2.0$  to  $3.3$  V), LC7152KM: 55 to 80 MHz ( $V_{DD} = 2.7$  to  $3.3$  V)
- 14-bit programmable reference-frequency divider  
320 Hz to 640 kHz reference frequency using a 10.24 MHz crystal oscillator
- Digital lock detector
- Dual charge pump
- Amplifier built-in for an active LPF
- Serial transmission data input (CCB format)
- LC7152NM with power-on reset circuit (pins  $\overline{OUTA}$  and  $\overline{OUTB}$  become open at power-on)
- 2.0 to 3.3 V supply voltage
- DIP24S and MFP24S packages

• CCB is a trademark of SANYO ELECTRIC CO., LTD.  
• CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Package Dimensions

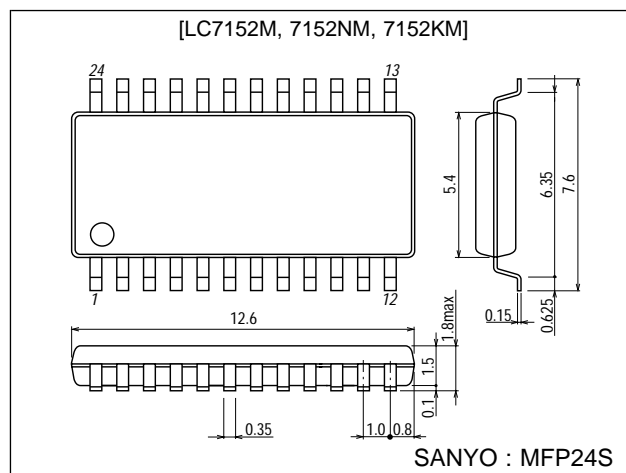
unit : mm

#### 3067-DIP24S



unit : mm

#### 3112-MFP24S



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## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\max}$	$V_{DD}$	-0.3 to +7.0	V
Maximum input voltage	$V_{IN\max(1)}$	CE, CL, DI, AIA, AIB	-0.3 to +7.0	V
	$V_{IN\max(2)}$	XIN, PIA, PIB, TEST	-0.3 to $V_{DD}+0.3$	V
Maximum output voltage	$V_{O\max(1)}$	$\overline{LDI}$ , $\overline{LDB}$	-0.3 to +7.0	V
	$V_{O\max(2)}$	AOA, AOB, $\overline{OUTA}$ , $\overline{OUTB}$	-0.3 to +15	V
	$V_{O\max(3)}$	PDA1, PDA2, PDB1, PDB2, XOUT	-0.3 to $V_{DD}+0.3$	V
Maximum output current	$I_{O\max(1)}$	$\overline{LDA}$ , $\overline{LDB}$ , $\overline{OUTA}$ , $\overline{OUTB}$	0 to 3	mA
	$I_{O\max(2)}$	AOA, AOB	0 to 6	mA
Allowable power dissipation	$P_d \max$	$T_a \leq 85^\circ\text{C}$ , LC7152	350	mW
		$T_a \leq 85^\circ\text{C}$ , LC7152M, 7152NM, 7152KM	160	mW
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +125	$^\circ\text{C}$

### Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD(1)}$	$V_{DD}$	2.0		3.3	V
	$V_{DD(2)}$	$V_{DD}$ : Serial data retention voltage, see Figure1, *1	1.5			V
	$V_{DD(3)}$	$V_{DD}$ : Power-on reset voltage, $t_R \geq 20\text{ ms}$ , see Figure1, *1			0.05	V
Input high-level voltage	$V_{IH(1)}$	CE, CL, DI: $V_{DD} = 2.0\text{ V}$	1.5		5.5	V
	$V_{IH(2)}$	CE, CL, DI: $V_{DD} = 3.3\text{ V}$	1.7		5.5	V
Input low-level voltage	$V_{IL(1)}$	CE, CL, DI: $V_{DD} = 2.0\text{ V}$	0		0.4	V
	$V_{IL(2)}$	CE, CL, DI: $V_{DD} = 3.3\text{ V}$	0		0.6	V
Output voltage	$V_O(1)$	$\overline{LDA}$ , $\overline{LDB}$	0		5.5	V
	$V_O(2)$	AOA, AOB, $\overline{OUTA}$ , $\overline{OUTB}$	0		13	V
Input frequency	$f_{IN(1)}$	XIN: Sine wave, capacitively coupled	1.0		13	MHz
	$f_{IN(2)}$	PIA, PIB: Sine wave, capacitively coupled *2	1.5		55	MHz
	$f_{IN(3)}$	PIA, PIB: Sine wave, capacitively coupled *3	55		80	MHz
Input amplitude	$V_{IN(1)}$	XIN: Sine wave, capacitively coupled	200		600	mVrms
	$V_{IN(2)}$	PIA, PIB: Sine wave, capacitively coupled *2,3	100		600	mVrms
Crystal oscillator frequency	$f_{Xtal}$	XIN, XOUT: $CI \leq 50\ \Omega$ , $CL \leq 16\text{ pF}$ *4	4	10.24	11	MHz

Note \*1 LC7152NM

		FA/FB (serial data input frequency select bits)		$V_{DD}$	Device
		[0]	[1]		
*2	$f_{IN(2)}$	1.5 to 23 MHz	20 to 55 MHz	2.0 to 3.3 V	LC7152, 7152M, LC7152NM, 7152KM
*3	$f_{IN(3)}$	—————	55 to 80 MHz	2.7 to 3.3 V	LC7152KM

\*4 CI is the crystal impedance and CL is the load capacitance.

# LC7152, 7152M, 7152NM, 7152KM

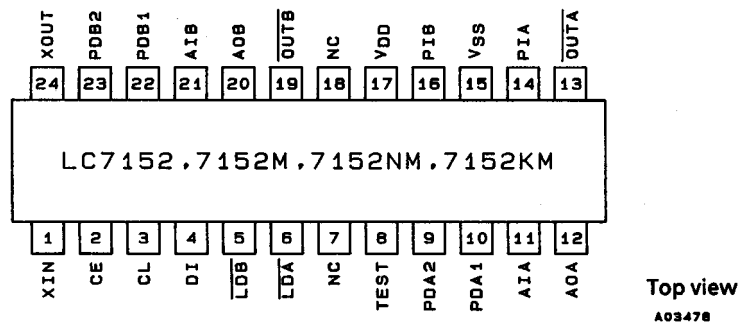
## Electrical Characteristics in the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high-level voltage	V <sub>OH</sub> (1)	PDA1, PDB1: I <sub>O</sub> = 1 mA	V <sub>DD</sub> - 1.0			V
	V <sub>OH</sub> (2)	PDA2, PDB2: I <sub>O</sub> = 2 mA	V <sub>DD</sub> - 1.0			V
Output low-level voltage	V <sub>OL</sub> (1)	PDA1, PDB1: I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL</sub> (2)	PDA2, PDB2: I <sub>O</sub> = 2 mA			1.0	V
	V <sub>OL</sub> (3)	OUTA, OUTB: I <sub>O</sub> = 1 mA			1.0	V
	V <sub>OL</sub> (4)	LDA, LDB: I <sub>O</sub> = 2 mA			1.0	V
	V <sub>OL</sub> (5)	AOA, AOB: I <sub>O</sub> = 0.5 mA, AIA = AIB = 1.2 V			0.5	V
	V <sub>OL</sub> (6)	AOA, AOB: I <sub>O</sub> = 1 mA, AIA = AIB = 1.3 V			0.5	V
Output off-leakage current	I <sub>OFF</sub> (1)	LDA, LDB: V <sub>O</sub> = 5.5 V			5.0	μA
	I <sub>OFF</sub> (2)	PDA1, PDB1, PDA2, PDB2: V <sub>O</sub> = 0/3.3 V		0.01	10.0	nA
	I <sub>OFF</sub> (3)	AOA, AOB, OUTA, OUTB: V <sub>O</sub> = 13 V			5.0	μA
Input high-level current	I <sub>IH</sub> (1)	CE, CL, DI: V <sub>I</sub> = 5.5 V			5.0	μA
	I <sub>IH</sub> (2)	XIN: V <sub>I</sub> = 3.3 V, V <sub>DD</sub> = 3.3 V	2.0		6.5	μA
	I <sub>IH</sub> (3)	PIA, PIB: V <sub>I</sub> = 3.3 V, V <sub>DD</sub> = 3.3 V	3.5		10.0	μA
	I <sub>IH</sub> (4)	AIA, AIB: V <sub>I</sub> = 3.3 V		0.01	10.0	nA
	I <sub>IH</sub> (5)	TEST: V <sub>I</sub> = 3.3 V, V <sub>DD</sub> = 3.3 V		120		μA
Input low-level current	I <sub>IL</sub> (1)	CE, CL, DI: V <sub>I</sub> = 0 V			5.0	μA
	I <sub>IL</sub> (2)	XIN: V <sub>I</sub> = 0 V, V <sub>DD</sub> = 3.3 V	2.0		6.5	μA
	I <sub>IL</sub> (3)	PIA, PIB: V <sub>I</sub> = 0 V, V <sub>DD</sub> = 3.3 V	3.5		10.0	μA
	I <sub>IL</sub> (4)	AIA, AIB: V <sub>I</sub> = 0 V		0.01	10.0	nA
	I <sub>IL</sub> (5)	TEST: V <sub>I</sub> = 0 V, V <sub>DD</sub> = 3.3 V			5.0	μA
Internal feedback resistance	R <sub>f</sub> (1)	XIN: V <sub>DD</sub> = 3.3 V		1.0		MΩ
	R <sub>f</sub> (2)	PIA, PIB: V <sub>DD</sub> = 3.3 V		600		kΩ
Internal pull-down resistance	R <sub>d</sub>	TEST: V <sub>DD</sub> = 3.3 V		30		kΩ
Input capacitance	C <sub>IN</sub>	XIN, PIA, PIB		2.5		pF
Supply current*1	I <sub>DD</sub> (1)	V <sub>DD</sub> (= 2.0 V): f <sub>IN</sub> = 55 MHz		3.0	8.0	mA
	I <sub>DD</sub> (2)	V <sub>DD</sub> (= 3.3 V): f <sub>IN</sub> = 55 MHz		7.0	14.0	mA
Supply current*2	I <sub>DD</sub> (4)	V <sub>DD</sub> (= 2.0 V): f <sub>IN</sub> = 55 MHz		1.5	4.5	mA
	I <sub>DD</sub> (5)	V <sub>DD</sub> (= 3.3 V): f <sub>IN</sub> = 55 MHz		3.9	8.0	mA

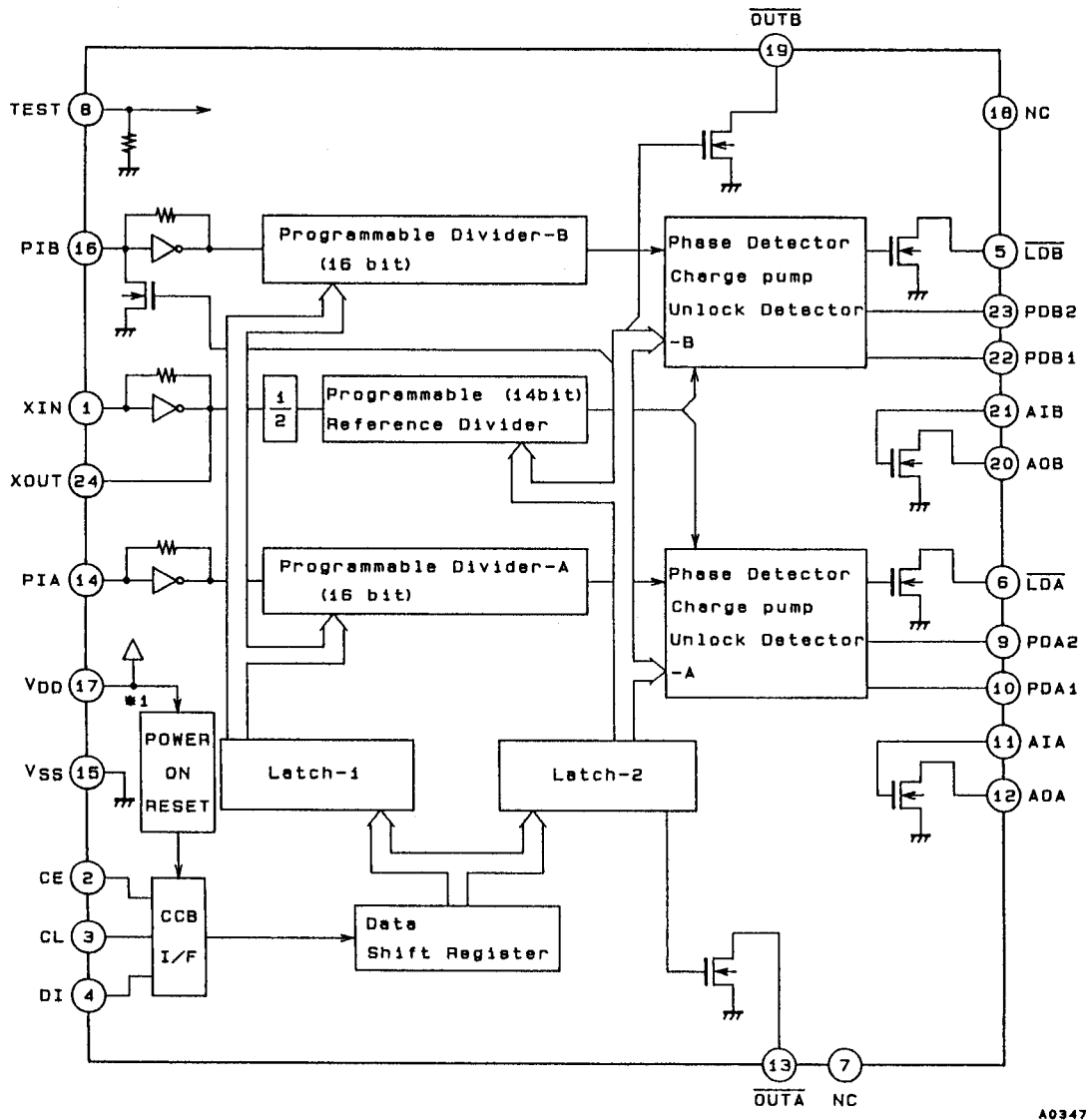
Note \*1. Dual PLL operation (both PLL-A and PLL-B), SB = 0, XIN = 10.24 MHz (crystal), PIA and PIB input = 100mVrms at f<sub>IN</sub>, all other inputs at V<sub>SS</sub>, all other outputs open.

\*2. Standby mode: Single PLL operation (PLL-A operating and PLL-B stopped), SB = 1, XIN = 10.24 MHz (crystal), PIA input = 100mVrms at f<sub>IN</sub>, all other inputs at V<sub>SS</sub>, all other outputs open.

## Pin Assignment



## Equivalent Block Diagram



## Pin Functions

Symbol	Pin No.	Function		Symbol	Pin No.	Function
PIB	16	Side-B oscillator signal input		PDB2	23	Sub charge pump
XIN	1	Crystal oscillator		PDB1	22	Main charge pump
XOUT	24			AIB	21	Low-pass filter transistors
PIA	14	Side-A oscillator signal output		AOB	20	
VDD	17	Power supply		OUTB	19	General-purpose output port
VSS	15	Ground		LDB	5	Side-B unlock detection
CE	2	Serial data input	Chip enable	PDA2	9	Sub charge pump
CL	3		Clock	PDA1	10	Main charge pump
DI	4		Data	AIA	11	Low-pass filter transistors
TEST	8	IC Test		AOA	12	
NC	7, 18	No connections		OUTA	13	General-purpose output port
LDB	5	Side-B unlock detection				

# LC7152, 7152M, 7152NM, 7152KM

## Pin Description

Symbol	Pin No.	Function	Description of function												
PIA	14	Side-A local oscillator signal input	<ul style="list-style-type: none"> <li>Side-A programmable divider. The input frequency ranges are as follows. <table border="1"> <thead> <tr> <th>FA = [0]</th><th>FA = [1]</th><th>V<sub>DD</sub></th><th>Device</th></tr> </thead> <tbody> <tr> <td>1.5 to 23 MHz</td><td>20 to 55 MHz</td><td>2.0 to 3.3 V</td><td>LC7152, 7152M LC7152NM, 7152KM</td></tr> <tr> <td>—————</td><td>55 to 80 MHz</td><td>2.7 to 3.3 V</td><td>LC7152KM</td></tr> </tbody> </table> </li> <li>FA: Serial data</li> <li>Bits DA0 to DA15 determine the divider ratios Divider ratio N = 272 to 65535</li> </ul>	FA = [0]	FA = [1]	V <sub>DD</sub>	Device	1.5 to 23 MHz	20 to 55 MHz	2.0 to 3.3 V	LC7152, 7152M LC7152NM, 7152KM	—————	55 to 80 MHz	2.7 to 3.3 V	LC7152KM
FA = [0]	FA = [1]	V <sub>DD</sub>	Device												
1.5 to 23 MHz	20 to 55 MHz	2.0 to 3.3 V	LC7152, 7152M LC7152NM, 7152KM												
—————	55 to 80 MHz	2.7 to 3.3 V	LC7152KM												
PIB	16	Side-B local-oscillator signal input	<ul style="list-style-type: none"> <li>Side-B programmable divider The input frequency ranges are the same as for PIA. FB(→ FA): Determined by the serial data</li> <li>Bits DB0 to DB15 determine the divider ratios Divider ratio N= 272 to 65535</li> <li>Serial data: Bit SB is the standby mode control bit When SB = 1, standby mode is selected. In standby mode, side-B is stopped, PIB is pulled down to V<sub>SS</sub>. When SB = 0, normal operation is selected.</li> </ul>												
XIN XOUT	1 24	Crystal oscillator	<ul style="list-style-type: none"> <li>Crystal oscillator connections (C<sub>I</sub> ≤ 50 Ω, C<sub>L</sub> ≤ 16pF).</li> <li>Note) When using a crystal other than as indicated above, its compatibility with the crystal oscillator must be thoroughly studied.</li> </ul>												
PDA1  PDB1	10  22	Side-A main charge pump  Side-B main charge pump	<ul style="list-style-type: none"> <li>These are PLL charge pump outputs that output the PLL phase error signals. When the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, the charge pump outputs a high-level signal for the phase error; when lower, the charge pump outputs a low-level signal for the phase error. If the two values match, these pins go to high-impedance.</li> <li>fosc/N &gt; fref or leading → Positive Pulse</li> <li>fosc/N &lt; fref or lagging → Negative Pulse</li> <li>fosc/N = fref and coincidence → High-Impedance (*SB = [1] : PDB1 → High-Impedance)</li> </ul>												
PDA2  PDB2	9  23	Side-A sub charge pump  Side-B sub charge pump	<ul style="list-style-type: none"> <li>PLL charge pump output; outputs PLL phase error signal only when the unlock condition is detected.</li> <li>The unlock detection threshold is set by serial data bits UL0 and UL1.</li> <li>When a phase error that is shorter than the detection threshold occurs, this signal goes to high impedance and the phase error signal for the main charge pump is output.</li> <li>The output pulse of the phase error signal has the same polarity as the main charge pump.</li> </ul>												
$\overline{\text{LDA}}$  $\overline{\text{LDB}}$	6  5	Side-A unlock detector output  Side-B unlock detector output	<ul style="list-style-type: none"> <li>Outputs the PLL lock/unlock status. Locked: Open Unlocked: Low</li> <li>The unlock detection threshold for lock/unlock discrimination is set by serial data bits UL0 and UL1.</li> <li>The output phase error extension is set by serial data bits UE0 and UE1.</li> <li>For details, refer to the description of the serial data.</li> <li>SB = 1: <math>\overline{\text{LDB}}</math> → Open</li> </ul>												
AIA AOA AIB OAB	11 12 21 20	Side-A low-pass filter transistor  Side-B low-pass filter transistor	<ul style="list-style-type: none"> <li>MOS N-channel transistor for the PLL filter</li> <li>The AOA and AOB output withstand voltage is 13V.</li> </ul>												
$\overline{\text{OUTA}}$  $\overline{\text{OUTB}}$	13  19	Side-A general purpose output port  Side-B general purpose output port	<ul style="list-style-type: none"> <li>These latch the serial data bits OA and OB that are sent from the controller, and then invert and output the data. (OUTA can also output XIN divided by two.)</li> <li>In the LC7152NM, OUTA and OUTB are open at the power-on reset.</li> </ul>												

For more information on crystal oscillator : Nihon Dempa Kogyo Co., Ltd.

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# LC7152, 7152M, 7152NM, 7152KM

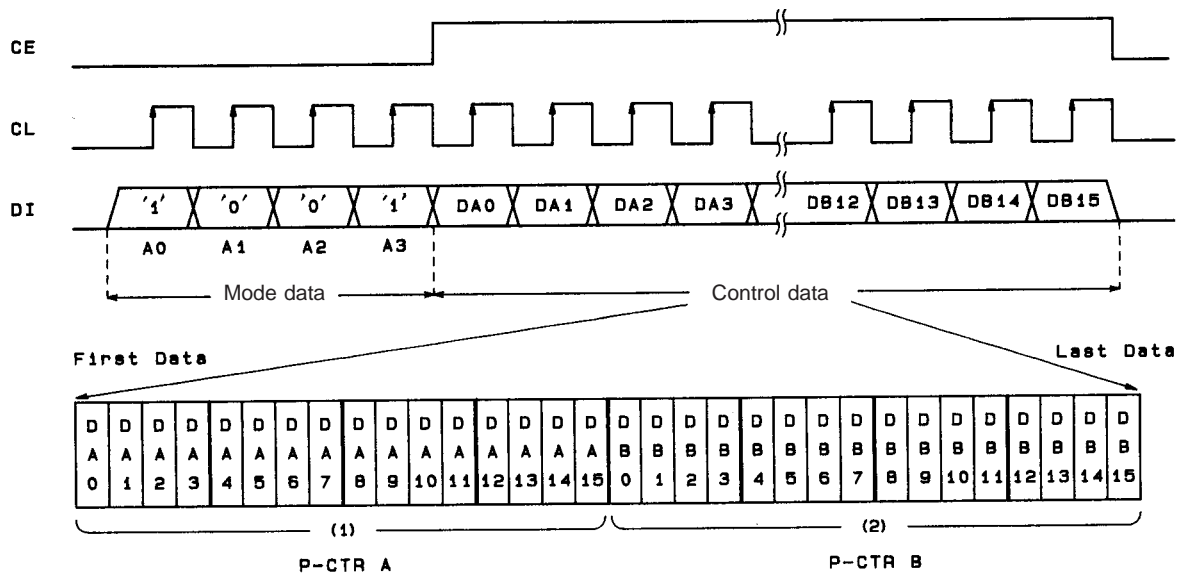
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Symbol	Pin No.	Function	Description of function
CE *1	2	Chip enable input	• Set this pin high when inputting serial data to the LC7152.
CL *1	3	Clock input	• Clock for data synchronization when inputting serial data to the LC7152.
DI *1	4	Data input	• Input for serial data being sent from the controller to the LC7152.
V <sub>DD</sub> V <sub>SS</sub>	17 15	Power supply Ground	• LC7152 power supply pin.
TEST	8	IC Test input	• LC7152 test pin. (Normally V <sub>SS</sub> or open.) • However, divide-by-two XIN frequency is output from the pin $\overline{\text{OUTA}}$ by applying the V <sub>DD</sub> level voltage after serial data transfer (T0 = T1 = T2 = 0). Crystal oscillation frequency can be checked normally when the pin is left open.

\*1 The input “H” voltage and the input “L” voltage on the CE, CL, and DI pins are V<sub>IH</sub> = 1.5 to 5.5V and V<sub>IL</sub> = 0 to 0.4V when V<sub>DD</sub> = 2.0V. When V<sub>DD</sub> = 3.3V, then V<sub>IH</sub> = 1.7 to 5.5V and V<sub>IL</sub> = 0 to 0.6V. (Voltage greater than V<sub>DD</sub> may be applied to V<sub>IH</sub>.)

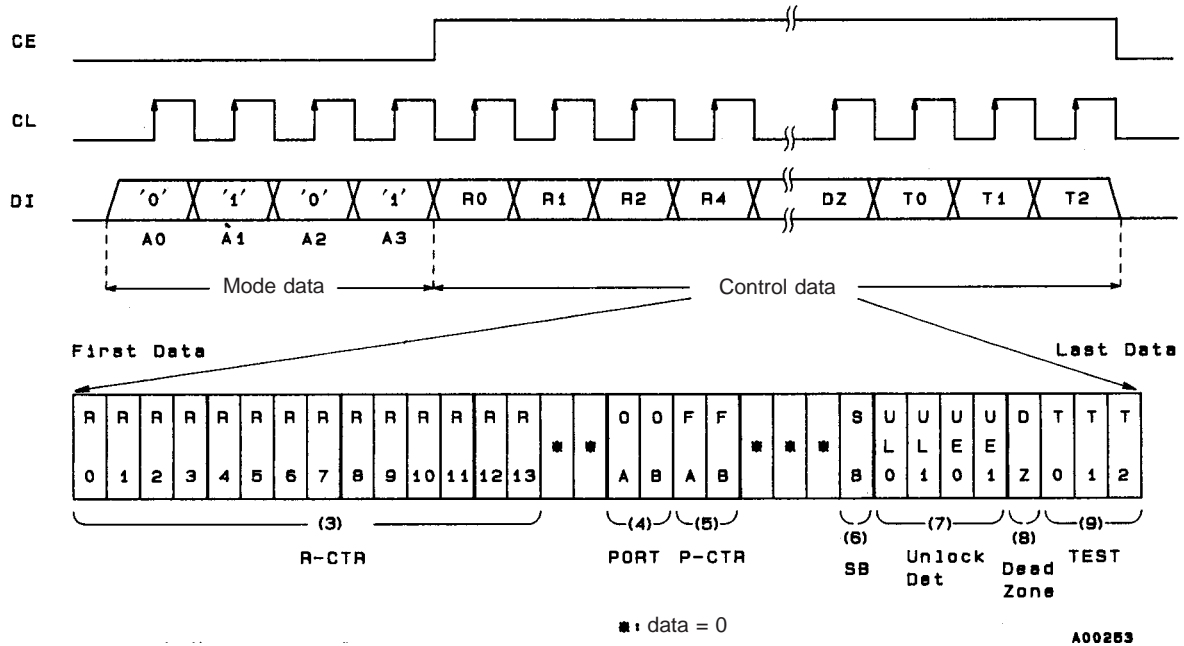
## Serial Input Data (PLL Control data) format

### Mode1: Latch-1 data (programmable divider data)

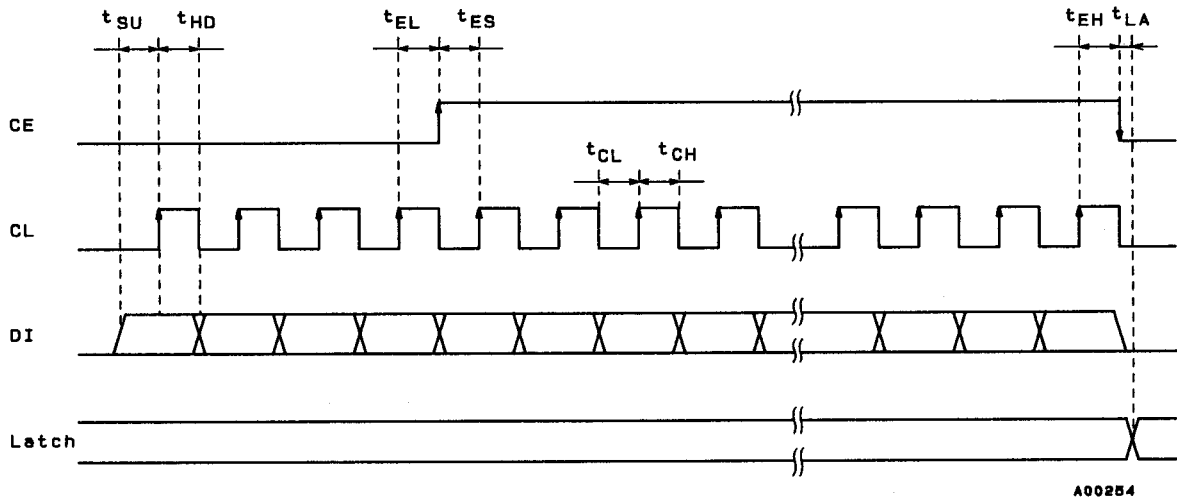


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Mode 2: Latch-2 data (reference divider and control data)



Serial Data Transfer Timing



Symbol	Parameter	10.24 MHz crystal	Other crystal frequencies
$t_{SU}$	Data setup time	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{HD}$	Data hold time	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{EL}$	Enable low-level pulse width	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{ES}$	Enable setup time	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{EH}$	Enable hold time	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{CL}$	Clock low-level pulse width	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{CH}$	Clock high-level pulse width	At least 0.40 $\mu$ s	At least $4/f_{X'tal}$
$t_{LA}$	Latch propagation delay	Up to 0.40 $\mu$ s	Up to $4/f_{X'tal}$

Note Perform data transfer after the crystal oscillations normalize. Data transferred before normal oscillations will not be recognized.

# Description of Serial Data

No.	Controller/Data	Description	Related Data																																																																														
(1)	Side-A programmable divider data: DA0 to DA15	<ul style="list-style-type: none"><li>This data sets the side-A programmable divider number. This data is a binary value in which DA0 is the LSB.</li><li>The range of divider values that can be set is 272 to 65,535.</li><li><math>NA = fVCO-A/fref</math></li></ul>	R0 to R13																																																																														
(2)	Side-B programmable divider data: DB0 to DB15	<ul style="list-style-type: none"><li>This data sets the side-B programmable divider number. This data is a binary value in which DB0 is the LSB.</li><li>The range of divider values that can be set is 272 to 65,535.</li><li><math>NB = fVCO-B/fref</math></li></ul>	R0 to R13																																																																														
(3)	Reference frequency data: R0 to R13	<ul style="list-style-type: none"><li>This data sets the reference divider number. This data is a binary value in which R0 is the LSB.</li><li>The range of divider values that can be set is 8 to 16,383.</li><li>(Actual divider number) = (setting) x 2</li><li>(reference frequency: fref) = (fX<sub>tal</sub>: XIN)/(actual divider number)</li></ul>	UL0 UI1 UE0 UE1																																																																														
(4)	Output port data: OA, OB	<ul style="list-style-type: none"><li>This data determines the output on the general-purpose output port.</li><li>OA → OUTA</li><li>OB → OUTB</li><li>Data 0: open; Data 1: low</li><li>During the power-on reset in the LC7152NM, OA and OB are both “0”.</li></ul>																																																																															
(5)	Input frequency range switching data: FA, FB	<ul style="list-style-type: none"><li>This data switches the input frequency range for the PIA and PIB pins.</li><li>(FA → PIA, FB → PIB)</li></ul> <table><tr><th>Data</th><th>Supply voltage (V<sub>DD</sub>)</th></tr><tr><td></td><td>2.0 to 3.3 V</td></tr><tr><td>[0]</td><td>1.5 to 23 MHz</td></tr><tr><td>[1]</td><td>20 to 55 MHz</td></tr></table> <ul style="list-style-type: none"><li>In the case of the LC7152KM: Data 1: 55 to 80 MHz (V<sub>DD</sub> = 2.7 V to 3.3 V)</li></ul>	Data	Supply voltage (V <sub>DD</sub> )		2.0 to 3.3 V	[0]	1.5 to 23 MHz	[1]	20 to 55 MHz	DA0 to DA15 DB0 to DB15																																																																						
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[1]	20 to 55 MHz																																																																																
(6)	Standby mode data : SB	<ul style="list-style-type: none"><li>This data puts the PLL in standby mode.</li><li>SB = 1: standby mode (LDB pin: open) → Single PLL operation: Side-A operating, side-B stopped</li><li>SB = 0: standby mode off → Dual PLL operation: Side-A operating, side-B operating</li><li>During the power-on reset in the LC7152NM, SB is “1”.</li></ul>																																																																															
(7)	Unlock detection data  : UL0, UL1          : UE0, UE1	<ul style="list-style-type: none"><li>This is the phase error detection threshold data that is used for PLL lock/unlock discrimination. If the threshold shown in the table is exceeded, the unlocked state is detected.</li></ul> <p style="text-align: right;">unit : μs</p> <table><tr><th rowspan="2">UL0</th><th rowspan="2">UL1</th><th rowspan="2">Phase error detector threshold</th><th colspan="5">XIN : fXIN [MHz] example</th></tr><tr><th>4.0</th><th>7.2</th><th>8.0</th><th>10.24</th><th>12.8</th></tr><tr><td>0</td><td>0</td><td>0</td><td>←</td><td>←</td><td>←</td><td>←</td><td>←</td></tr><tr><td>1</td><td>0</td><td>±4/fX<sub>tal</sub></td><td>±1.00</td><td>±0.55</td><td>±0.50</td><td>±0.39</td><td>±0.31</td></tr><tr><td>0</td><td>1</td><td>±16/fX<sub>tal</sub></td><td>±4.00</td><td>±2.22</td><td>±2.00</td><td>±1.56</td><td>±1.20</td></tr><tr><td>1</td><td>1</td><td>±64/fX<sub>tal</sub></td><td>±16.00</td><td>±8.88</td><td>±8.00</td><td>±6.25</td><td>±5.00</td></tr></table> <p>(Note) Note that if the data changes in lock state, the PLL will be unlocked temporarily.</p> <ul style="list-style-type: none"><li>The detected phase error (øE) signal can be extended by a certain amount of time and output on the LDA and LDB pins. This data determines the length of this extension. However, when UL0 = UL1 = 0, the phase error is not extended, and is output directly.</li></ul> <p style="text-align: right;">unit : ms</p> <table><tr><th rowspan="2">UE0</th><th rowspan="2">UE1</th><th rowspan="2">Reference frequency fref</th><th colspan="3">Reference frequency : fref [kHz] example</th></tr><tr><th>1 kHz</th><th>5 kHz</th><th>12.5 kHz</th></tr><tr><td>0</td><td>0</td><td>4 × (1/fref)</td><td>4.0*</td><td>0.8</td><td>0.32</td></tr><tr><td>1</td><td>0</td><td>8 × (1/fref)</td><td>8.0</td><td>1.6</td><td>0.64</td></tr><tr><td>0</td><td>1</td><td>32 × (1/fref)</td><td>32.0</td><td>6.4*</td><td>2.56</td></tr><tr><td>1</td><td>1</td><td>64 × (1/fref)</td><td>64.0</td><td>12.8</td><td>5.12*</td></tr></table> <p style="text-align: right;">(*standard value)</p>	UL0	UL1	Phase error detector threshold	XIN : fXIN [MHz] example					4.0	7.2	8.0	10.24	12.8	0	0	0	←	←	←	←	←	1	0	±4/fX <sub>tal</sub>	±1.00	±0.55	±0.50	±0.39	±0.31	0	1	±16/fX <sub>tal</sub>	±4.00	±2.22	±2.00	±1.56	±1.20	1	1	±64/fX <sub>tal</sub>	±16.00	±8.88	±8.00	±6.25	±5.00	UE0	UE1	Reference frequency fref	Reference frequency : fref [kHz] example			1 kHz	5 kHz	12.5 kHz	0	0	4 × (1/fref)	4.0*	0.8	0.32	1	0	8 × (1/fref)	8.0	1.6	0.64	0	1	32 × (1/fref)	32.0	6.4*	2.56	1	1	64 × (1/fref)	64.0	12.8	5.12*	
UL0	UL1	Phase error detector threshold				XIN : fXIN [MHz] example																																																																											
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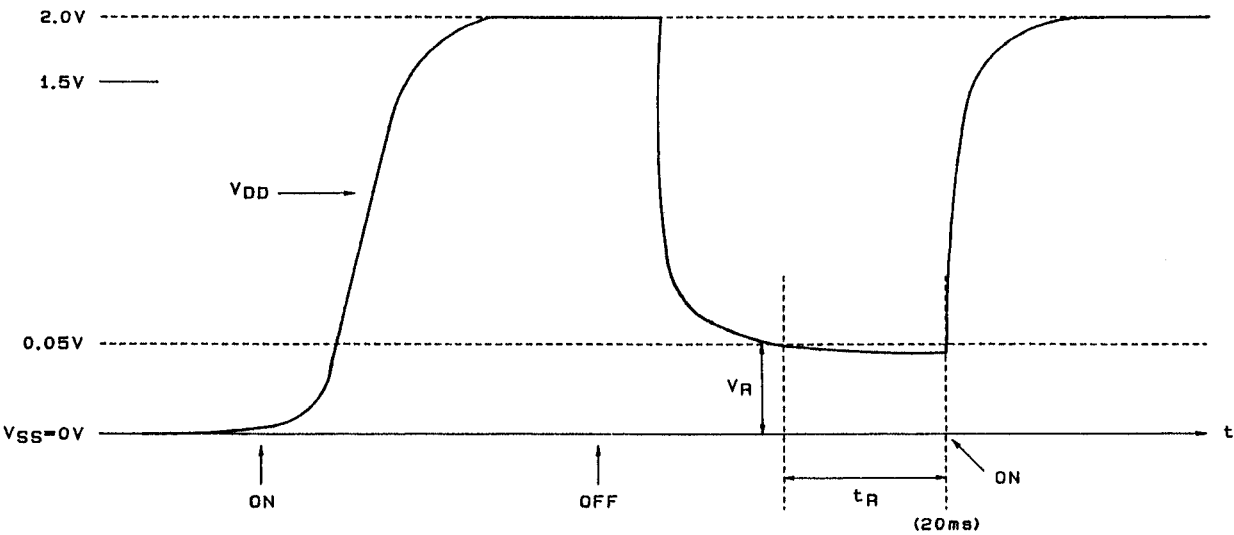
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No.	Controller/Data	Description	Related Data						
(8)	Dead zone control data: DZ	<div><div>• This data controls the phase comparator dead zone. (DZA &lt; DZB)</div><table><tr><td>DZ</td><td>Mode</td></tr><tr><td>0</td><td>DZA</td></tr><tr><td>1</td><td>DZB</td></tr></table></div>	DZ	Mode	0	DZA	1	DZB	
DZ	Mode								
0	DZA								
1	DZB								
(9)	IC test data: T0, T1, T2	<div><div>• This is the IC test mode switching data. The user does not need to be concerned about this data. Assume that T0 = T1 = T2 = 0. Normally, the test pins must be either at V<sub>SS</sub> or left open.</div></div>							

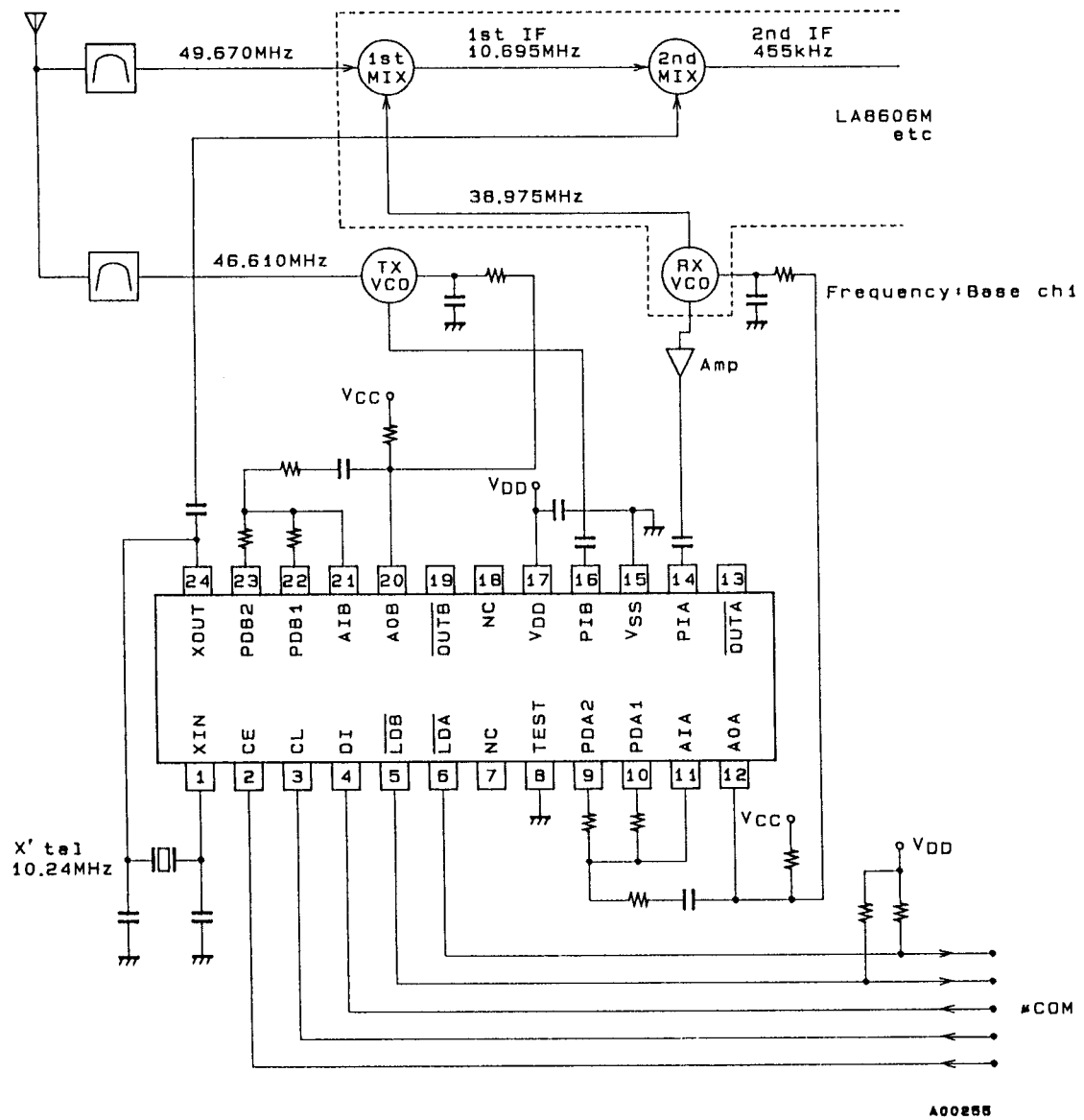
Power-on Reset supply voltage



- Power-on reset is performed when the supply voltage  $V_{DD}$  exceeds 2.0 V by power application after the  $V_{DD}$  has once fallen under 0.05 V and kept the level for at least 20ms.
- Latch data is retained when the  $V_{DD}$  is 1.5 V, where power-on reset is not performed.

# LC7152, 7152M, 7152NM, 7152KM

## Sample Application Circuit (FCC: 10 ch 46/49 MHz cordless telephone)



## LC7152, 7152M, 7152NM, 7152KM

**Example: FCC 1-channel 46/49 MHz cordless telephone base station (See diagram in the preceding page.)**

for fref: 5 kHz, RX VCO: 38.975 MHz, TX VCO: 46.610 MHz

### Programmable Divider Data

$$(1) \quad NA = \frac{f_{VCO} - A}{f_{ref}} = \frac{RX \text{ VCO}}{f_{ref}} = \frac{38.975 \text{ MHz}}{5 \text{ kHz}} = 7795 \text{ (DA0 to DA15)} \\ (1E73) \text{ Hex}$$

$$(2) \quad \text{NB} = \frac{\text{fVCO} - \text{B}}{\text{fref}} = \frac{\text{TX VCO}}{\text{fref}} = \frac{46.610\text{MHz}}{5\text{kHz}} = 9322 \text{ (DB0 to DB15)}$$

(246A)Hex

(3) Reference frequency data

$$NR = \left( \frac{fX'_{tal}}{f_{ref}} \right) \div 2 = \frac{10.24MHz}{5kHz} \div 2 = 1024 \text{ (R0 to R13)}$$

(400)Hex

(4) Output port data

General-purpose output port: Open (OA = 0, OB = 0)

(5) Input frequency range select bits

$$FA = FB = 1$$

(6) Standby mode

During standby (SB = 1)

(7) Unlock detector output

Extends the phase error signal by 6.4ms if a phase error of  $\pm 6.25 \mu\text{s}$  or more is generated.

$$: \text{UL0} = \text{UL1} = 1$$

: UE0 = 0, UE1 = 1

(8) Dead-zone control data

DZA mode :  $DZ = 0$

(9) LSI test data:  $T_0 = T_1 = T_2 = 0$

**(1) Mode 1: Latch-1 data**

D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 0	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15
1	1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	0	0

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## (2) Mode 2: Latch-2 data

R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	■	■	D	D	F	F	■	■	■	S	U	U	U	U	D	T	T	T
0	1	2	3	4	5	6	7	8	9	10	11	12	13			A	B	A	B				B	L	L	E	E	Z	0	1	2	
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	0	

```
data = 0
```

A00257



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