

SANYO**LC7151**

C MOS Si Gate IC

Meeting FCC 10-Channel Standard PLL for Cordless Telephone

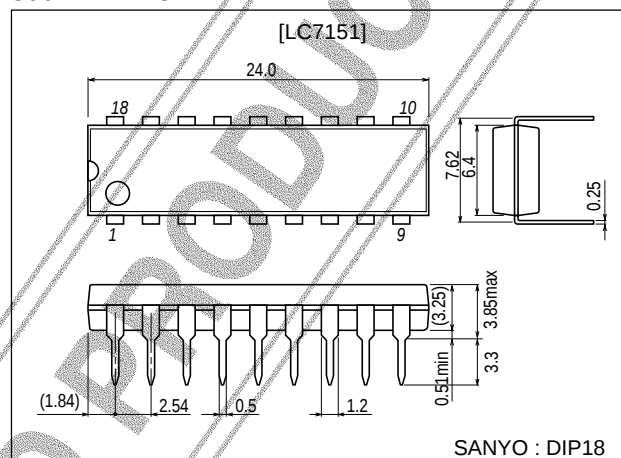
Functions

- On-chip PLL for transmission/reception.
- On-chip digital unlock detector.
(only PLL for transmission)
- 5.0kHz/4.4kHz output pins for guard tone.
- Standby function.
- Pull-down resistance at CH select pins (D1 to D4).
LC7150 : With (for mechanical SW)
LC7151 : Without (for μ COM)

Package Dimensions

unit:mm

3007B-DIP18



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\max}$		-0.3 to +6.5	V
Maximum input voltage	$V_I\max$	All input pins	-0.3 to $V_{DD}+0.3$	V
Maximum output voltage	$V_{O1\max}$	F1, F2 output OFF	-0.3 to +6.5	V
	$V_{O2\max}$	Output pins other than V_{O1}	-0.3 to $V_{DD}+0.3$	V
Output current	I_{OUT}	F1, F2, LDT	0 to 3.0	mA
Allowable power dissipation	$P_d\max$	$T_a \leq 75^\circ\text{C}$	350	mW
Operating temperature	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Allowable Operating Conditions at $T_a = 25^\circ\text{C}$, $V_{SS}=0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0		5.5	V
Input high-level voltage	V_{IH1}	D1 to D4, $\overline{SB}$	$0.7V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL1}	D1 to D4, $\overline{SB}$	0		$0.3V_{DD}$	V
Input high-level voltage	V_{IH2}	$\overline{R/B}$	$0.9V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL2}	$\overline{R/B}$	0		$0.1V_{DD}$	V

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SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC7151

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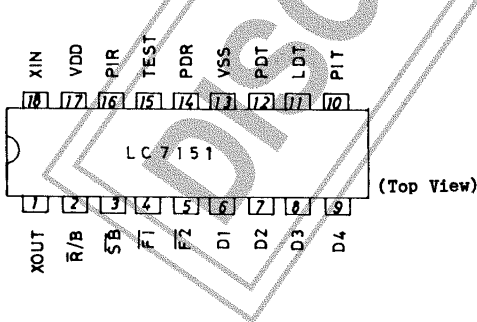
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input frequency	f_{IN1}	PIT ; $V_{IN}=0.15V_{rms}$	10		27	MHz
	f_{IN2}	PIR ; $V_{IN}=0.15V_{rms}$	30		42	MHz
	f_{IN3}	XIN ; $V_{IN}=0.3V_{rms}$	5.0	10.24	11.0	MHz
Input amplitude	V_{IN1}	PIT ; $f_{IN}=27MHz$	0.15		$0.3V_{DD}$	Vrms
	V_{IN2}	PIR ; $f_{IN}=42MHz$	0.15		$0.3V_{DD}$	Vrms
	V_{IN3}	XIN ; $f_{IN}=11MHz$	0.3		$0.3V_{DD}$	Vrms

Electrical Characteristics at $T_a = 25^{\circ}C$, under Allowable Operating Conditions

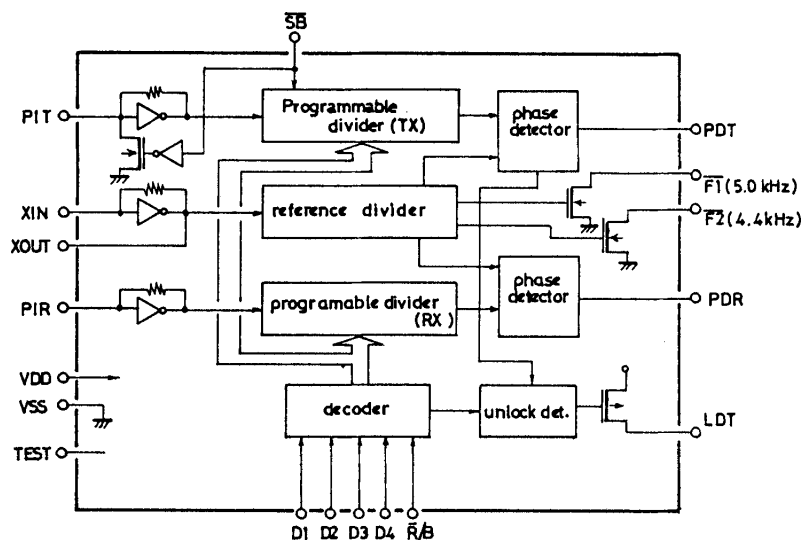
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH1}	XIN ; $V_I=V_{DD}$			20	μA
Input low-level current	I_{IL1}	XIN ; $V_I=V_{SS}$			20	μA
Input high-level current	I_{IH2}	PIT, PIR ; $V_I=V_{DD}$			40	μA
Input low-level current	I_{IL2}	PIT, PIR ; $V_I=V_{SS}$			40	μA
Input high-level current	I_{IH3}	$\overline{SB}$, $\overline{R/B}$, D1 to D4 ; $V_I=V_{DD}$			10	μA
Input low-level current	I_{IL3}	$\overline{SB}$, $\overline{R/B}$, D1 to D4 ; $V_I=V_{SS}$			10	μA
Feedback Resistance	R_{f1}	XIN ; $V_{DD}=4.3V$		1.0		$M\Omega$
	R_{f2}	PIT, PIR ; $V_{DD}=4.3V$		0.5		$M\Omega$
Output high-level voltage	V_{OH1}	PDT, PDR ; $I_O=0.5mA$	$V_{DD}-1.0$			V
Output low-level voltage	V_{OL1}	PDT, PDR ; $I_O=0.5mA$			1.0	V
Output OFF leakage current	I_{off1}	PDT, PDR ; $V_O=V_{DD}/V_{SS}$		0.01	1.0	nA
Output high-level voltage	V_{OH2}	LDT ; $I_O=1mA$	$V_{DD}-1.0$			V
Output OFF leakage current	I_{off2}	LDT ; output OFF $V_O=V_{SS}$			5.0	μA
Output low-level voltage	V_{OL2}	F1, F2 ; $I_O=1mA$			1.0	V
Output OFF leakage current	I_{off3}	F1, F2 ; output OFF $V_O=5.5V$			5.0	μA
Current drain	I_{DD1}	(C3) $V_{DD}=3.0V$		4		mA
	I_{DD2}	(C3) $V_{DD}=4.5V$		7		mA
	I_{DD3}	(C3) $V_{DD}=5.5V$		13		mA
	I_{DD4}	(C2) $V_{DD}=3.0V$		3		mA
	I_{DD5}	(C2) $V_{DD}=4.5V$		5		mA
	I_{DD6}	(C2) $V_{DD}=5.5V$		10		mA
		(C3) : XIN=10.24MHz, Xtal connected PIT=27MHz 150mVrms PIR=42MHz 150mVrms $\overline{R/B}=V_{DD}$, $\overline{SB}=V_{DD}$, other pin open				
		(C2) : XIN=10.24MHz, Xtal connected PIR=42MHz, 150mVrms $\overline{R/B}=V_{DD}$, $\overline{SB}=V_{SS}$, other pin open				

(Note) Power $V_{DD}-V_{SS}$: Insert a capacitor of 2000pF or greater.

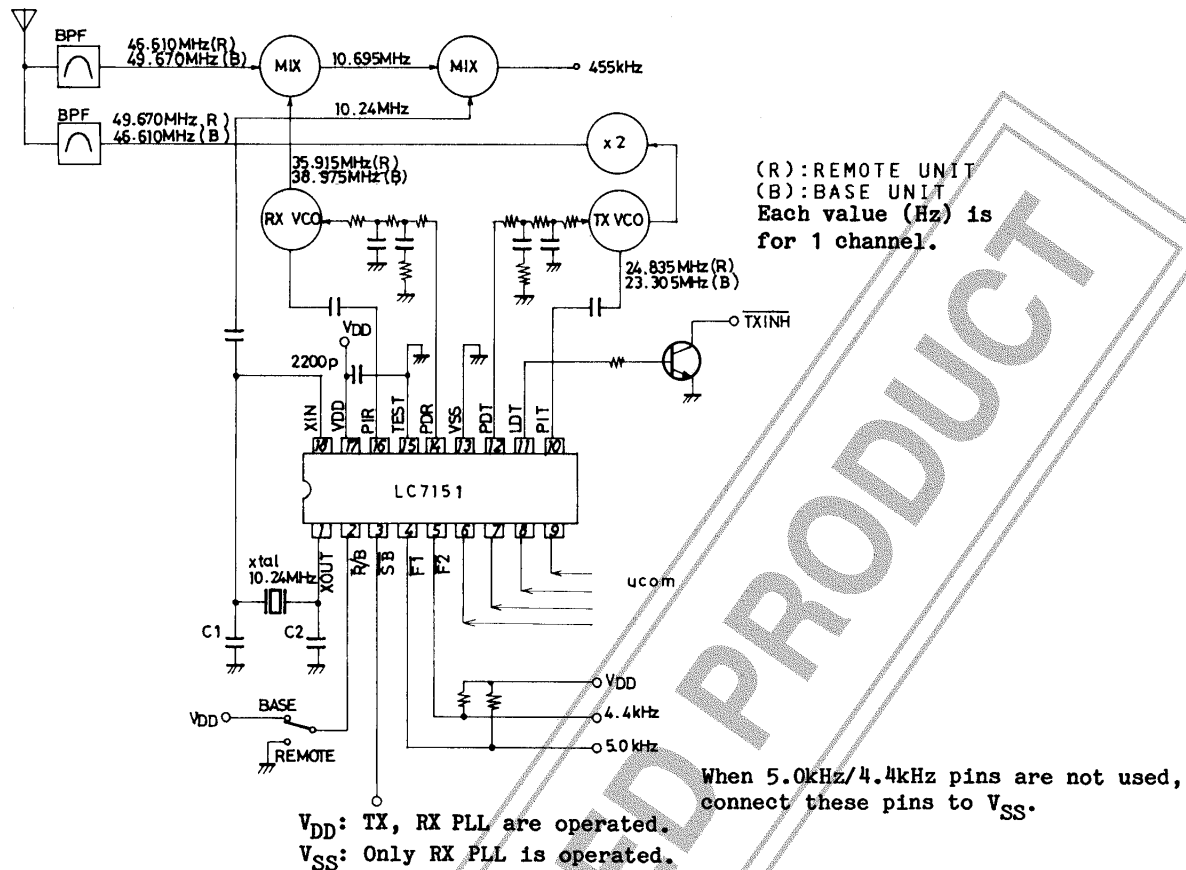
Pin Assignment



Equivalent Circuit Block Diagram



Sample Application Circuit



Pin Description

- F1: 5.0kHz output. When not used, connect to V_{SS}.
- F2: 4.4kHz output (10.24MHz+2304). When not used, connect to V_{SS}.
- V_{DD}, V_{SS}: Power supply.
- XIN, XOUT: Crystal resonator (10.24MHz).
- D1 to D4: Channel select pin.
- R/B: Base unit/remore unit select pin.
 - R/B= "0" (V_{SS}) Remote unit
 - R/B= "1" (V_{DD}) Base unit
- SB: Used to stop the TX PLL at the standby mode to minimize current drain.
 - SB= "0" (V_{SS}) The charge pump enters a high-impedance mode. Standby mode. Only the RX PLL is operated.
 - SB= "1" (V_{DD}) The TX, RX PLL are operated.
- PIT: TX programmable divider input pin.
- PIR: RX programmable divider input pin.
- PDT: TX charge pump output pin.
- PDR: RX charge pump output pin.
- TEST: IC test input pin. Connected to V_{SS}.
- LDT: TX PLL unlock signal output pin.

When the phase difference becomes t_D ($=6.25\mu\text{s}$) or more, 5.6ms output pulse is delivered at the LDT pin.

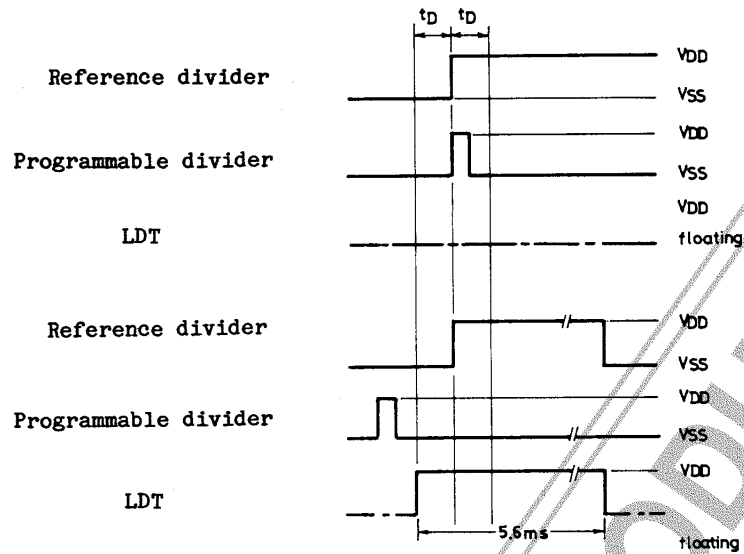
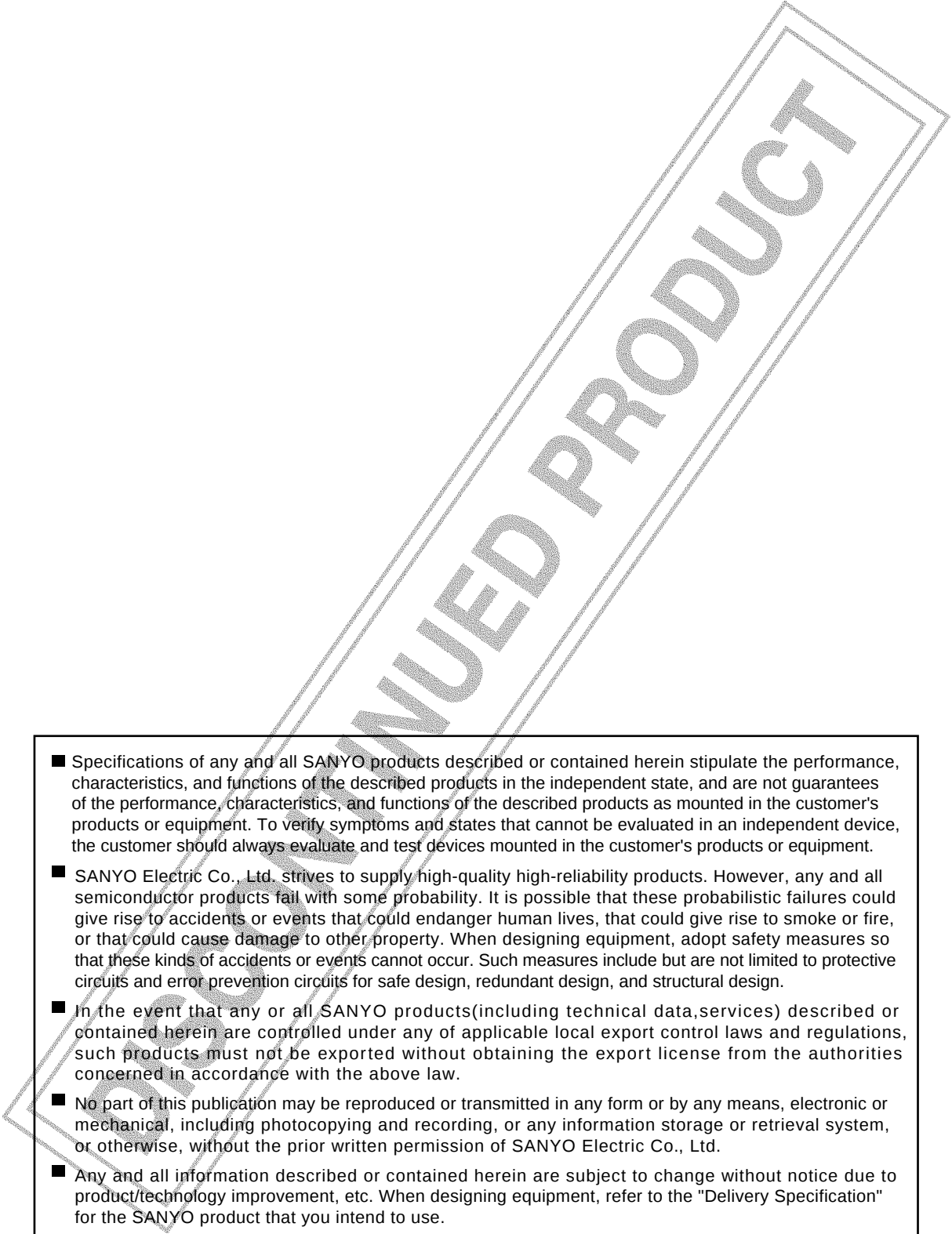


Table of Frequency Division

INPUT	C H	REMOTE ($\bar{R}/B=0'$)					BASE ($R/B=1'$)				
		TX (fref=2.5kHz)			RX (fref=5kHz)		TX (fref=2.5kHz)			RX (fref=5kHz)	
D1D2D3D4		f _{TX} (MHz)	f _{VCO} (MHz)	N	f _{VCO} (MHz)	N	f _{TX} (MHz)	f _{VCO} (MHz)	N	f _{VCO} (MHz)	N
1 0 0 0	1	49.670	24.8350	9934	35.915	7183	46.610	23.305	9322	38.975	7795
0 1 0 0	2	49.845	24.9225	9969	35.935	7187	46.630	23.315	9326	39.150	7830
1 1 0 0	3	49.860	24.9330	9972	35.975	7195	46.670	23.335	9334	39.165	7833
0 0 1 0	4	49.770	24.8850	9954	36.015	7203	46.710	23.355	9342	39.075	7815
1 0 1 0	5	49.875	24.9375	9975	36.035	7207	46.730	23.365	9346	39.180	7836
0 1 1 0	6	49.830	24.9150	9966	36.075	7215	46.770	23.385	9354	39.135	7827
1 1 1 0	7	49.890	24.9450	9978	36.135	7227	46.830	23.415	9366	39.195	7839
0 0 0 1	8	49.930	24.9650	9986	36.175	7235	46.870	23.435	9374	39.235	7847
1 0 0 1	9	49.990	24.9950	9998	36.235	7247	46.930	23.465	9386	39.295	7859
0 1 0 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 1 0 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 0 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 0 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 1 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
1 1 1 1	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855
0 0 0 0	10	49.970	24.9850	9994	36.275	7255	46.970	23.485	9394	39.275	7855

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