Ordering number:ENN *3932

CMOS IC

LC7073, 7073M

Error Detection and Correction ICs for RDS Demodulators

Preliminary

Overview

The LC7073 and LC7073M are error detection and correction ICs that provide an easy interface to the LA2230 and LA2231 radio data system (RDS) demodulators. Both devices incorporate an on-chip oscillator that connects directly to an external ceramic resonator.

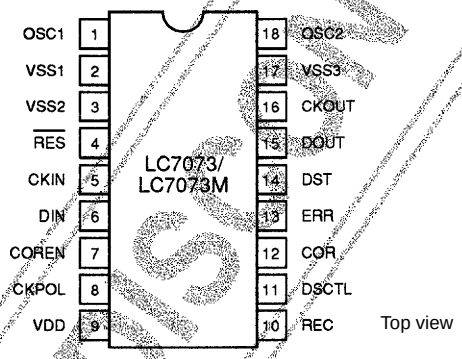
The LC7073 and LC7073M provide group synchronization, selectable error detection and correction, output clock polarity selection, a block data start signal output and an error output that signals error correction failures.

The LC7073 and LC7073M operate from a 5 V supply and are available in 18-pin DIPs and MFPs, respectively.

Features

- RDS error detection and correction.
- Easy interface with LA2230 and LA2231 demodulator ICs.
- Serial data transfer system.
- Group synchronization capability.
- Selectable error detection and correction.
- Output clock polarity selection.
- Block data start output.
- Error output.
- On-chip oscillator.
- 5 V supply.
- 18-pin DIP (LC7073) and 18-pin MFP (LC7073M).

Pin Assignment

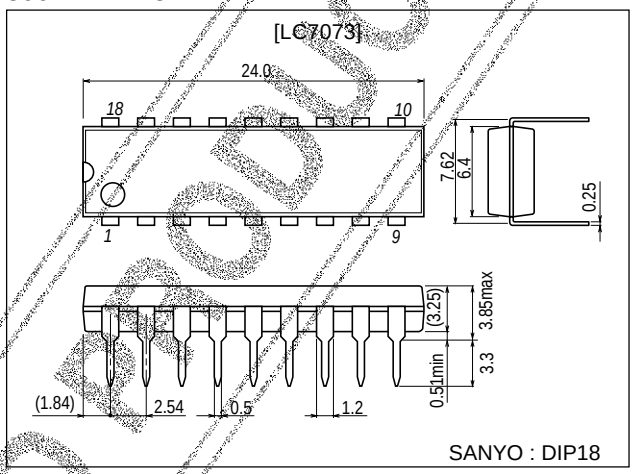


Top view

Package Dimensions

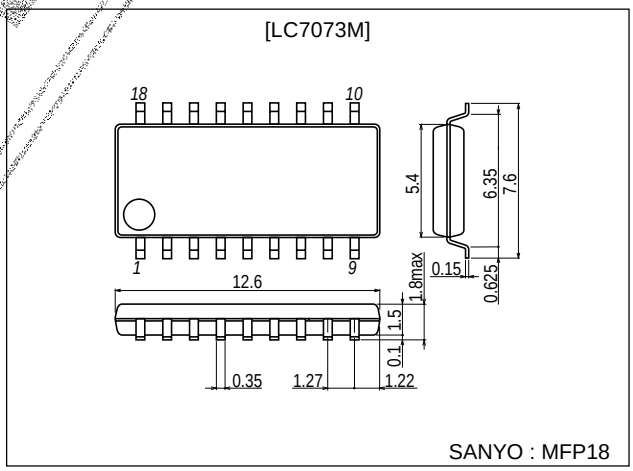
unit:mm

3007B-DIP18



unit:mm

3095-MFP18



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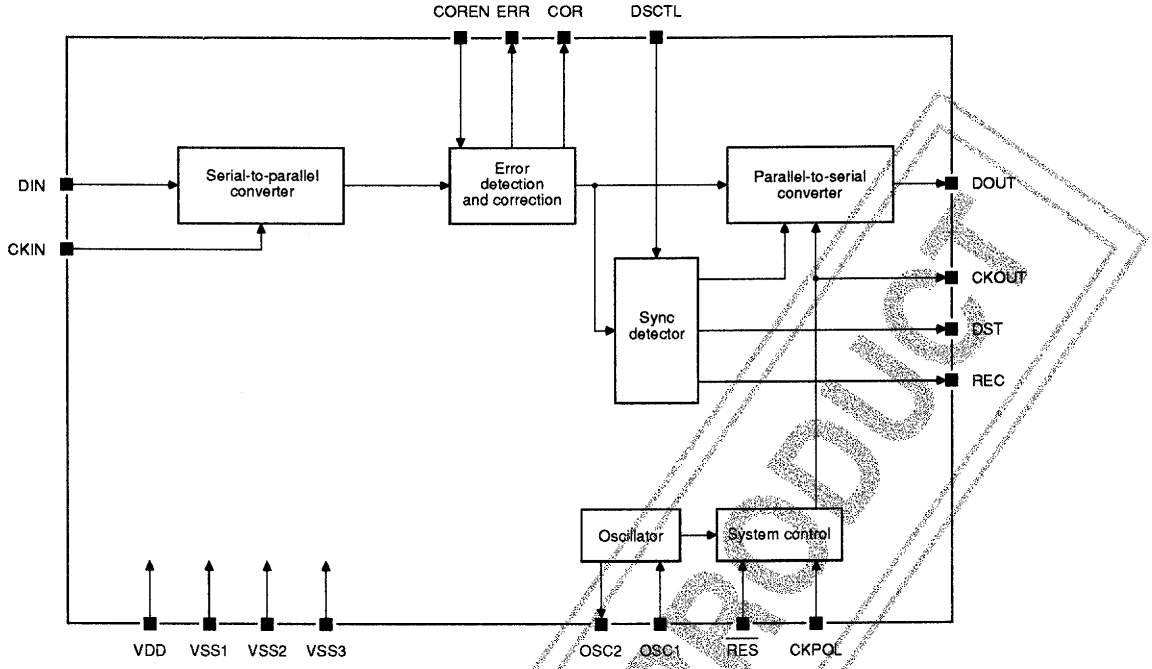
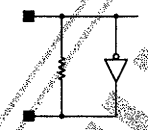
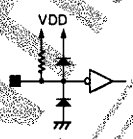
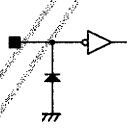
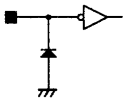
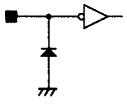
Block Diagram



Pin Function

Number	Name	Equivalent circuit	Description
1	OSC1		External ceramic resonator connection 1
2	V_{SS1}		Ground
3	V_{SS2}		Ground
4	$\overline{RES}$		Schmitt-trigger reset input. Held LOW for a minimum of 4 clock cycles
5	CKIN		Serial data input clock. Connects to RDS demodulator output clock
6	DIN		Serial data input. Connects to RDS demodulator data output
7	COREN		Error-correction enable input. LOW disables error correction and HIGH enables error correction

Continued on next page.

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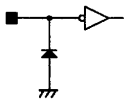
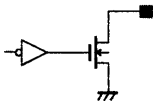
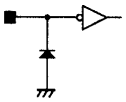
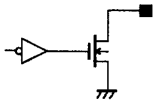
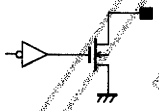
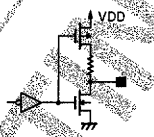
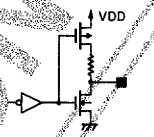
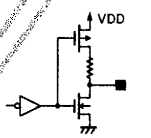
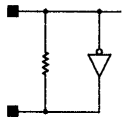
Number	Name	Equivalent circuit	Description
8	CKPOL		Serial data output clock polarity select input
9	V_{DD}		5 V supply
10	REC		Serial data receive detect output. LOW while receiving, after sync detection. High impedance when not receiving. High impedance after reset
11	DSTCTL		Data start control input. LOW initiates data start for second block, and HIGH, for all blocks
12	COR		Error-correction enabled/disabled output. LOW when error correction occurs and HIGH when no error correction occurs. High impedance after reset
13	ERR		Error-detect output. LOW when error correction fails. High impedance when error correction does not fail. High impedance after reset
14	DST		Serial data start output. LOW indicates no data start, and HIGH, data start. HIGH after reset
15	DOUT		Serial data output. HIGH after reset
16	CKOUT		Serial data output clock
17	V_{SS3}		Ground
18	OSC2		External ceramic resonator connection 2

Specifications

Absolute Maximum Ratings at Ta = +25˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$		−0.3 to +7.0	V
OSC2, DST, DOUT and CKOUT output voltage	V_{O1}		−0.3 to V_{DD}+0.3	V
REC, COR and ERR output voltage	V_{O2}		−0.3 to +15	V
RES and OSC1 input voltage	V_{I1}		−0.3 to V_{DD}+0.3	V
CKIN, DIN, COREN, CKPOL and DSCTL input voltage	V_{I2}		−0.3 to +15	V
REC, COR and ERR output current	I_{O1}		20	mA
DST, DOUT and CKOUT output current	I_{O2}		−2 to +20	mA
Output pins total current	I_O		−14 to +90	mA
DIP allowable power dissipation	Pd max	DIP: Ta=–40 to +85˚C	to 280	mW
MFP allowable power dissipation	Pd max	MFP: Ta=–40 to +85˚C	to 200	mW
Operating temperature	Topr		–40 to +85	˚C
Storage temperature	Tstg		–55 to +125	˚C

Reommended Operating Conditions at Ta = –40 to +85˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V, V_{DD} = 4.5 to 6.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage range	V_{DD}		4.5		6.0	V
CKIN, DIN, COREN, CKPOL and DSCTL high-level input voltage	V_{IH1}		$0.7V_{DD}$		13.5	V
$\overline{RES}$ and OSC1 high-level input voltage	V_{IH2}		$0.8V_{DD}$		V_{DD}	V
CKIN, DIN, COREN, CKPOL and DSCTL low-level input voltage	V_{IL1}		V_{SS}		$0.3V_{DD}$	V
$\overline{RES}$ low-level input voltage	V_{IL2}		V_{SS}		$0.25V_{DD}$	V

Electrical Characteristics at Ta = –40 to +85˚C, V_{SS1}, V_{SS2}, V_{SS3} = 0V, V_{DD} = 4.5 to 6.0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CKIN, DIN, COREN, CKPOL and DSCTL high-level input current	I_{IH1}	V_I=13.5V			5.0	µA
CKIN, DIN, COREN, CKPOL and DSCTL low-level input current	I_{IL1}	V_I=V_{SS}	−1.0			µA
$\overline{RES}$ low-level input current	I_{IL2}	V_I=V_{SS}	−45	−10		µA
DST, DOUT and CKOUT high-level output voltage	V_{OH}	I_{OH}=−50µA	V_{DD}−1.2			V
		I_{OH}=−10µA	V_{DD}−0.5			
REC, COR, ERR, DST, DOUT and CKOUT low-level output voltage	V_{OL}	I_{OL}=10mA			1.5	V
		I_{OL}=1.8mA, See note 1.			0.4	
REC, COR and ERR output leakage current	I_{OFF}	V_O=13.5V			5.0	µA
		V_O=V_{SS}	−1.0			
$\overline{RES}$ hysteresis voltage	V_{HYS}			$0.1V_{DD}$		V
Supply current	I_{DD}	See note 2.		4	10	mA
Oscillator stabilization time	t_{CFS}	See figure 7.			10	ms

Note

1. Idle pins have output currents less than 1mA.
2. Oscillator running, V_I=V_{DD}, I_O=0mA

Timing Diagrams

The relationship between the LC7073 and LC7073M input data (RDS demodulated data output) and output data is shown in figure 1.

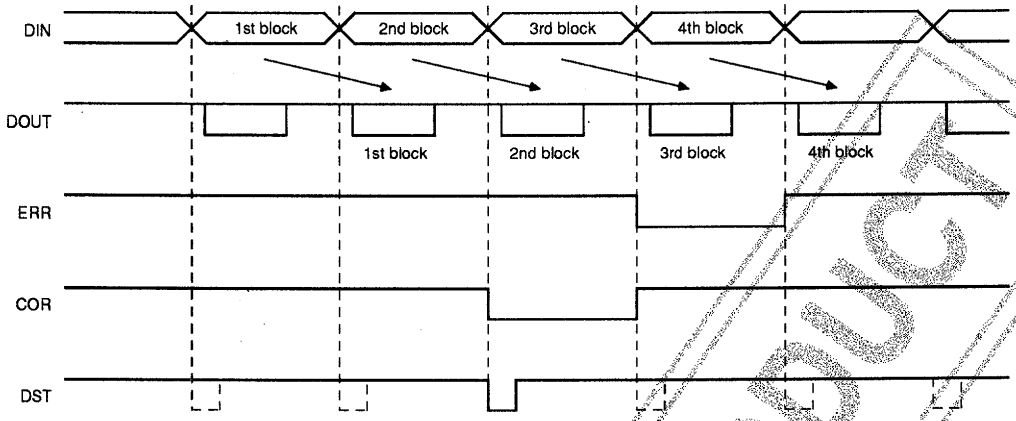


Figure 1. Input and output data

Note

The dotted lines show data start (DST) pulses when the data start control (DSTCTL) is LOW. The serial output data is delayed by one block between input and output. The error (ERR) and correction (COR) signals remain active if errors are detected continually.

Serial Output Data Timing and Format

The following list shows the symbols used in the serial output data string in figure 2.

S	Start bit (normally 0)
E	Error flag (See table 1.)
F	Correction flag (See table 1.)
OE	Offset E (normally 0, not used)
OF	Offset F (normally 0, not used)
A/B	Group. 0–group A, 1–group B
B0, B1	Block bits. 00–1st block, 01–2nd block, 10–3rd block, 11–4th block
D0 to D15	Output data

Table 1. Error and correction flags

Indication	E	F
No error	0	0
Error corrected	0	1
Not correctable	1	×

Note

× = don't care

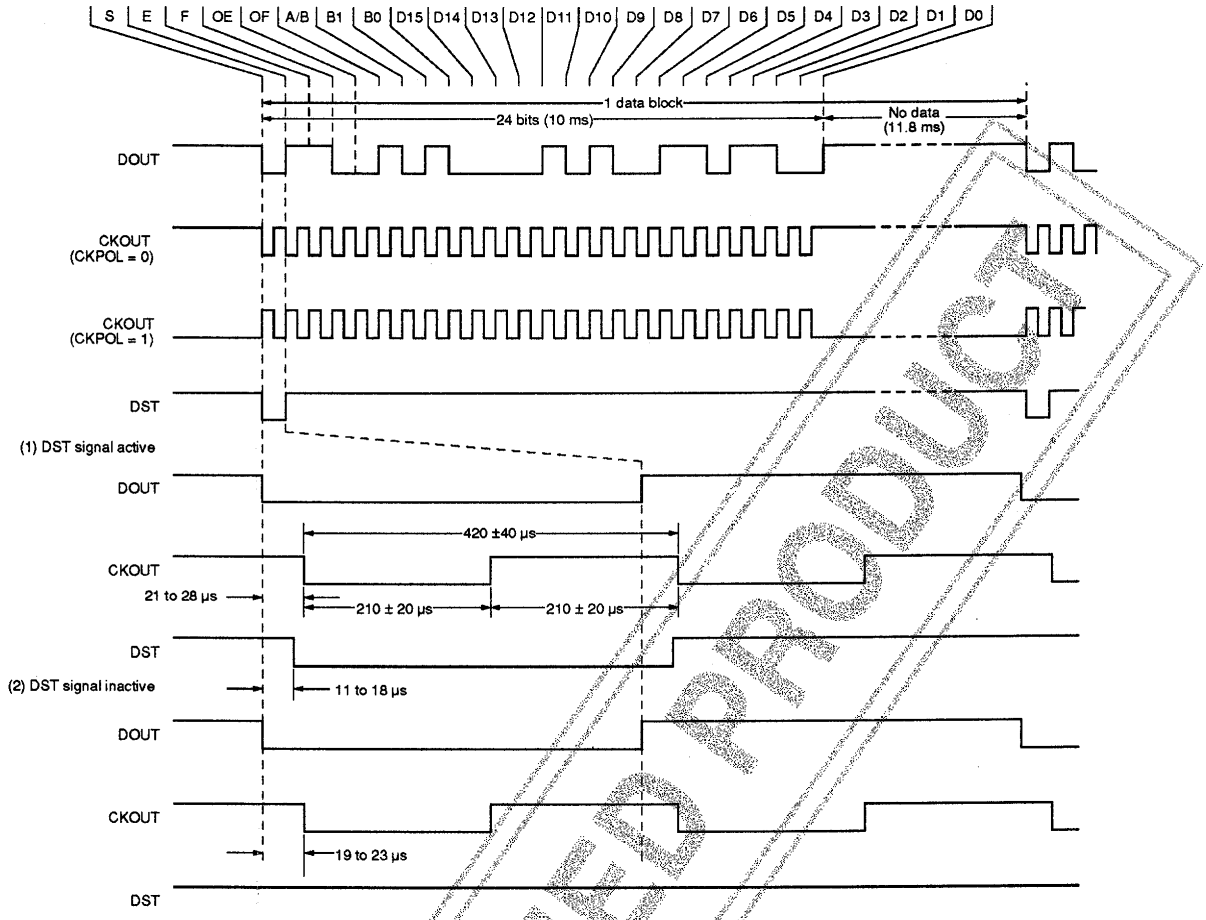


Figure 2. Serial output data format and timing

CKPOL Input Read Delay

CKPOL is read 1 ms after a reset as shown in figure 3.

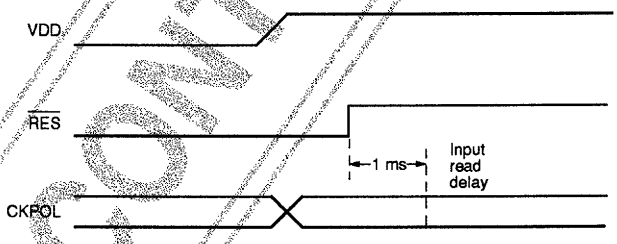


Figure 3. CKPOL input read delay

COREN and DSTCTL Input Read

COREN and DSTCTL are monitored at intervals of one input clock cycle, and their logic states can be changed at any time. During sync detection, a change in input state occurs if either pin remains steady for four successive clock intervals as shown in figure 4.

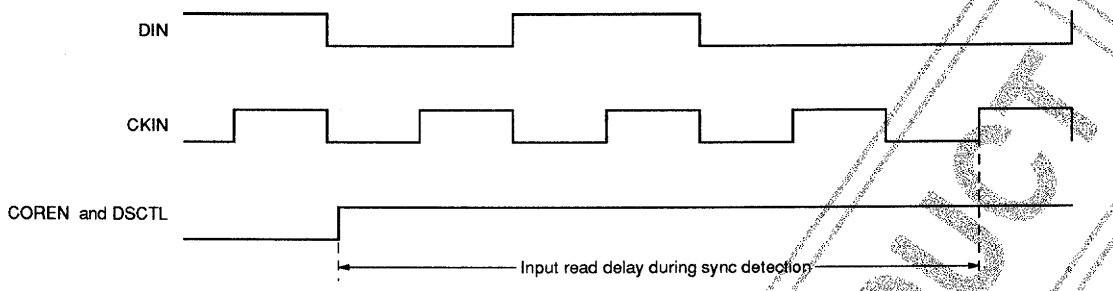


Figure 4. Input read during sync detection

After sync detection a change in input state occurs if either COREN or DSTCTL remains steady for four successive input data blocks as shown in figure 5.

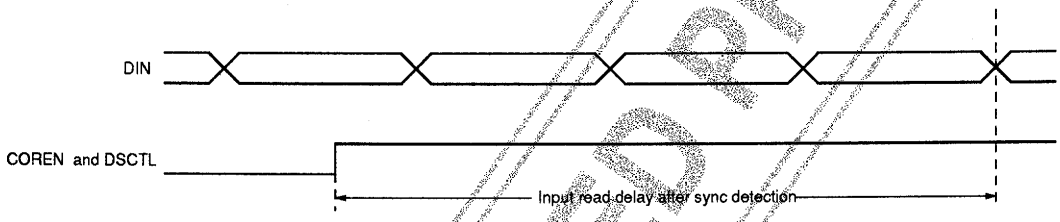


Figure 5. Input read after sync detection

Design Notes

Oscillator specifications are shown in table 2 and figure 6. Oscillator stabilization delay is shown in figure 7. Reset input circuitry is shown in figure 8. Supply rise time versus $\overline{RES}$ delay is shown in figure 9.

Table 2. Oscillator capacitor values

4 MHz resonator type	C1, C2
Murata-CSA4.00MG	30 pF ±10%
Kyocera-KBR4.0M	30 pF ±10%

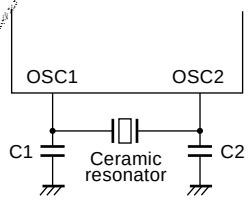
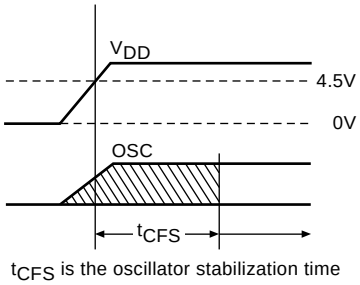


Figure 6. Oscillator circuit



t_{CFS} is the oscillator stabilization time

Figure 7. Oscillator stabilization delay

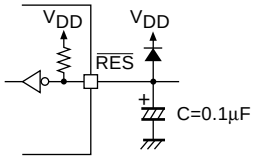


Figure 8. Reset input

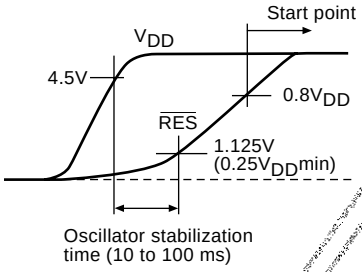


Figure 9. Supply rise time vs. reset delay

A minimum delay of 10 ms should be allowed for oscillator stabilization. A 10 to 100 ms reset delay is generated using a 0.1 μF reset capacitor, C. A larger capacitor should be used if the supply rise time is longer.

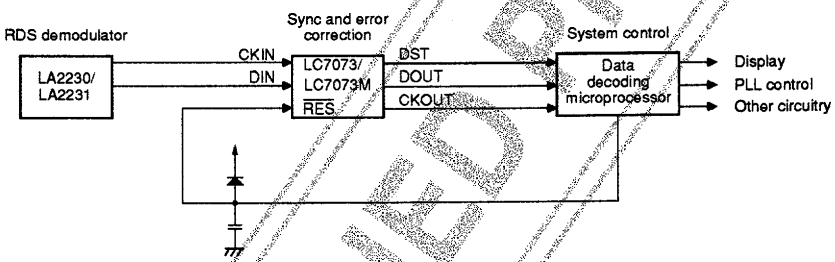


Figure 10. System block diagram

Device Comparison

The LC7070N, LC7070M and LC7071NM have identical basic functions, pinouts and input/output timing to those of the LC7073 and LC7073M. Their respective packages and output circuitry are compared in table 3.

Table 3. Device comparison

Device	Package	Output type
LC7070N	18-pin DIP	Open-drain
LC7070NM	18-pin MFP	
LC7071NM	18-pin MFP	Totem-pole using MOS transistors
LC7073	18-pin DIP	
LC7073M	18-pin MFP	

The differences in output data format between the LC7070N/LC7070NM/LC7071NM and LC7073/LC7073M are as follows.

Offset Words E and F

The LC7070N/LC7070NM/LC7071NM recognizes offset words E and F and performs group sync detection. The LC7073/LC7073M does not recognize offset words E and F–it only detects A, B, C, C' and D.

Input Data Bits

If all data bits are 0, the LC7070N/LC7070NM/LC7071NM only recognizes offset word E. The LC7073/LC7073M does not recognize the offset word E block. No sync detection occurs if all input data bits are 0. Once data cutoff has been determined, output data stops and the sync cutoff sequence begins.

Sync Detection Method

The LC7070N/LC7070NM/LC7071NM searches for 5 consecutive blocks in the correct sequence within each group of 12 blocks. The LC7073/LC7073M searches for 2 consecutive blocks in the correct sequence within each group of 3 blocks.

Data Output After Sync Detection

The LC7070N/LC7070NM/LC7071NM starts data output with the first block (offset A) directly after the last block in the sync detection group. If sync detection occurs during the first block (offset A), the LC7073/LC7073M starts data output with the second block (offset B). If sync detection occurs during the second or third block (offset B or C), and finishes before the end of the fourth block (offset D), the LC7073/LC7073M starts data output with the first block (offset A) of the second group.

Sync Error

A sync error occurs if no offset word is detected for more than five consecutive blocks. This applies to both the LC7070N/ LC7070NM/LC7071NM and LC7073/LC7073M.

Error Correction

In error-correction mode, an error of less than 5 bits is corrected to an accuracy of 5 bits. This applies to both the LC7070N/LC7070NM/LC7071NM and the LC7073/LC7073M.

Precaution

Note that the solder-dip method should not be used for the LC7073M (MFP).