



LC66P308

4-bit Microcontroller with Built-in PROM

Overview

The LC66P308 is a 4-bit microcontroller with a built-in 8 Kbyte PROM. It is compatible with the LC663XX series mask ROM devices, making it ideal for prototyping and software development and testing.

The LC66P308 features 33 user-defined options comprising output configuration, output level after reset, watchdog timer and oscillator configuration options. The output configuration options are open-drain, open-drain with pull-up, and CMOS. The oscillator options are ceramic resonator, RC oscillator and external clock.

The LC66P308 operates from a 5 V supply and is available in 42-pin DIPs and 48-pin QIPs.

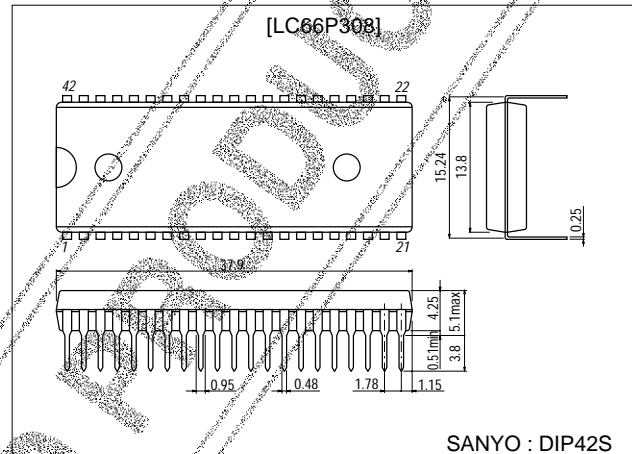
Features

- 33 user-defined options including port output configuration, output level after reset and watchdog timer options
- Ceramic resonator, RC oscillator or external clock option
- 8 Kbyte PRQM (0000H to 2007H user addressable)
- Compatible with the LC663XX series mask ROM devices
- 0.92 to 10.0 μ s instruction cycle time
- 5 V supply
- 42-pin DIP and 48-pin QIP

Package Dimensions

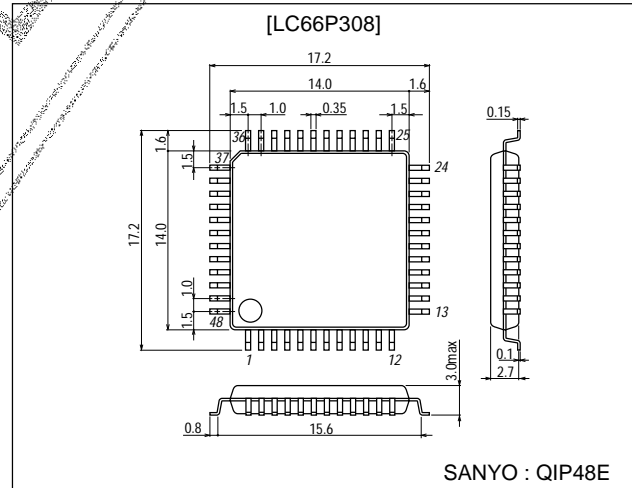
Unit:mm

3025B-DIP42S



Unit:mm

3156-QIP48E



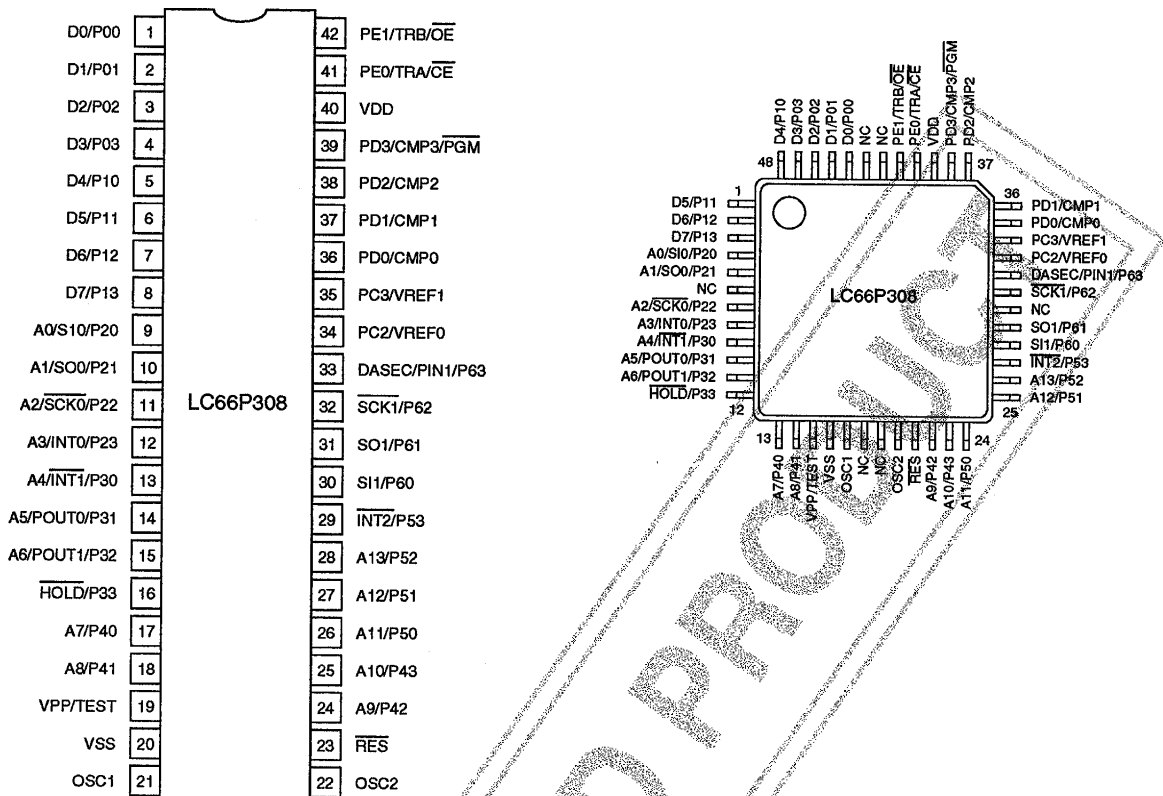
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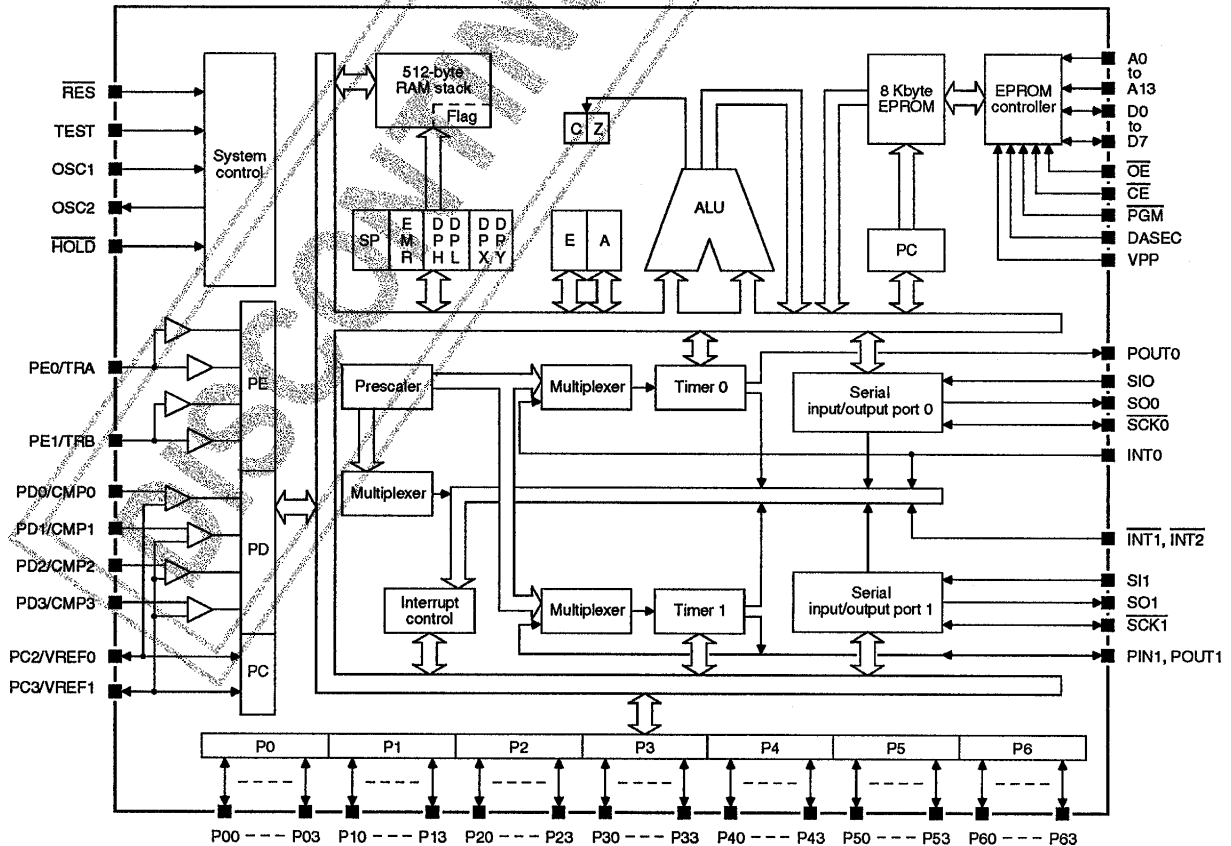
LC66P308

Pin Assignment



Top view

Block Diagram



LC66P308

Pin Description

| Number | | Name | Description |
|--------|-----------------------|----------------|--|
| DIP42S | DIP48E | | |
| 1 | 44 | D0/P00 | Multiplexed 4-bit input/output port P0 (P00 to P03) and PROM data bus lines (D0 to D3) |
| 2 | 45 | D1/P01 | |
| 3 | 46 | D2/P02 | |
| 4 | 47 | D3/P03 | |
| 5 | 48 | D4/P10 | Multiplexed 4-bit input/output port P1 (P10 to P13) and PROM data bus lines (D4 to D7) |
| 6 | 1 | D5/P11 | |
| 7 | 2 | D6/P12 | |
| 8 | 3 | D7/P13 | |
| 9 | 4 | A0/SI0/P20 | Multiplexed 4-bit input/output port P2 (P20 to P23), serial input 0 (SI0), serial output 0 (SO0), serial clock 0 (SCK0), interrupt request 0 (INT0) and PROM address bus lines (A0 to A3) |
| 10 | 5 | A1/SO0/P21 | |
| 11 | 7 | A2/SCK0/P22 | |
| 12 | 8 | A3/INT0/P23 | |
| 13 | 9 | A4/INT1/P30 | Multiplexed 3-bit input/output port P3 (P30 to P32), interrupt request 1 (INT1), timer outputs (POUT0 and POUT1) and address bus lines (A4 to A6) multiplexed single-bit input port (P33) and hold-mode control input (HOLD) |
| 14 | 10 | A5/POUT0/P31 | |
| 15 | 11 | A6/ROUT1/P32 | |
| 16 | 12 | HOLD/P33 | |
| 17 | 13 | A7/P40 | Multiplexed 4-bit input/output port P4 (P40 to P43) and PROM address bus lines (A7 to A10) |
| 18 | 14 | A8/P41 | |
| 24 | 22 | A9/P42 | |
| 25 | 23 | A10/P43 | |
| 19 | 15 | VPP/TEST | CPU test input |
| 20 | 16 | VSS | Ground |
| 21 | 17 | OSC1 | External oscillator connections |
| 22 | 20 | OSC2 | |
| 23 | 21 | RES | Reset input |
| 26 | 24 | A11/P50 | Multiplexed 4-bit input/output port P5 (P50 to P53), interrupt request 2 (INT2) and PROM address bus lines (A11 to A13) |
| 27 | 25 | A12/P51 | |
| 28 | 26 | A13/P52 | |
| 29 | 27 | INT2/P53 | |
| 30 | 28 | SI1/P60 | Multiplexed 4-bit input/output port P6 (P60 to P63), serial input 1 (SI1), serial output 1 (SO1), serial clock 1 (SCK1), event counter input (PIN1) and PROM data security control input (DASEC) |
| 31 | 29 | SO1/P61 | |
| 32 | 31 | SCK1/P62 | |
| 33 | 32 | DASEC/PIN1/P63 | |
| 34 | 33 | PC2/VREF0 | Multiplexed 2-bit input/output port PC (PC2 and PC3), CMP0 reference voltage input (VREF0) and CMP1 to CMP3 reference voltage input (VREF1) |
| 35 | 34 | PC3/VREF1 | |
| 36 | 35 | PD0/CMP0 | Multiplexed 4-bit input port PD (PD0 to PD3), PROM program control input (PGM) and comparator inputs (CMP0 to CMP3) |
| 37 | 36 | PD1/CMP1 | |
| 38 | 37 | PD2/CMP2 | |
| 39 | 38 | PD3/CMP3/PGM | |
| 40 | 39 | VDD | 5V supply |
| 41 | 40 | PE0/TRA/CE | Multiplexed 2-bit input port PE (PE0 and PE1), 2-bit three-level input port (TRA and TRB), PROM chip enable (CE) and output enable (OE) |
| 42 | 41 | PE1/TRB/OE | |
| | 6, 18, 19, 30, 42, 43 | NC | No connection |

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|-------------------|------------|----------------------|------------------|
| Supply voltage | V_{DD} | | -0.3 to +7.0 | V |
| Ports P2 to P6 (excluding P33) input voltage | V_{I1} | See note 1 | -0.3 to +15.0 | V |
| Input voltage range for all inputs | V_{I2} | See note 2 | -0.3 to $V_{DD}+0.3$ | V |
| Ports P2 to P6 (excluding P33) output voltage | V_{O1} | See note 1 | -0.3 to +15.0 | V |
| Output voltage range for all outputs | V_{O2} | See note 2 | -0.3 to $V_{DD}+0.3$ | V |
| Ports P0, P1, P4 and P5 output source current | $-I_{OP1}$ | | 2 | mA |
| Ports P2, P3 (excluding P33), P6 and PC output source current | $-I_{OP2}$ | | 4 | mA |
| Ports P0 to P6 (excluding P33) and PC output sink current | I_{ON} | | 20 | mA |
| Ports P0 to P3 (excluding P33), P40 and P41 total sink current | ΣI_{ON1} | | 75 | mA |
| Ports P42, P43, P5, P6 and PC total sink current | ΣI_{ON2} | | 75 | mA |
| Ports P0 to P3 (excluding P33), P40 and P41 total source current | $-\Sigma I_{OP1}$ | | 25 | mA |
| Ports P42, P43, P5, P6 and PC total source current | $-\Sigma I_{OP2}$ | | 25 | mA |
| Power dissipation (DIP42S) | P_{D1} | | 600 | mW |
| Power dissipation (QIP48E) | P_{D2} | See note 3 | 430 | mW |
| Operating temperature range | T_{opr} | | -30 to +70 | $^\circ\text{C}$ |
| Storage temperature range | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Notes

1. Open-drain output configuration option
2. All output configuration options
3. Heat-soak the QIP package before mounting. Do not immerse the package in the solder dip tank when mounting the QIP on the substrate, and avoid prolonged contact with the solder.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|----------|------------|------------|------|
| Supply voltage | V_{DD} | | 5 | V |
| Supply voltage range | V_{DD} | | 4.5 to 5.5 | V |
| Hold-mode supply voltage range for data retention | V_{DD} | | 1.8 to 5.5 | V |

Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$, unless otherwise noted

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|------------|--|--------------|------|--------------|---------------|
| | | | min | typ | max | |
| Reset-mode supply current | I_{DD} | 4MHz ceramic resonator | | 4.5 | 8.0 | mA |
| | | 4MHz external clock | | 6.5 | 11.0 | mA |
| | | RC oscillator | | 4 | 8 | mA |
| Halt-mode supply current | I_{DDHT} | 4MHz ceramic resonator | | 3.0 | 5.0 | mA |
| | | 4MHz external clock | | 3.5 | 6.0 | mA |
| | | RC oscillator | | 3.0 | 5.0 | mA |
| Hold-mode supply current | I_{DDHD} | $V_{DD} = 1.8$ to 5.5V | | 0.01 | 10.0 | μA |
| Ports P2, P3 (excluding P33), P5 and P6, RES and OSC1 LOW-level input voltage | V_{IL1} | Output n-channel transistor OFF. See note 1. | V_{SS} | | $0.25V_{DD}$ | V |
| HOLD/P33 LOW-level input voltage | V_{IL2} | $V_{DD} = 1.8$ to 5.5V | V_{SS} | | $0.25V_{DD}$ | V |
| Ports P0, P1, P4 PC, PD and PE, and TEST LOW-level input voltage | V_{IL3} | Output n-channel transistor OFF. See note 1. | V_{SS} | | $0.3V_{DD}$ | V |
| Ports PE LOW-level input voltage | V_{IL4} | Ternary input mode. | V_{SS} | | $0.2V_{DD}$ | V |
| Ports PE MID-level input voltage | V_{IM} | Ternary input mode. | $0.4V_{DD}$ | | $0.6V_{DD}$ | V |
| Ports P2 to P6 (excluding P33) HIGH-level input voltage | V_{IH1} | Output n-channel transistor OFF. See note 2. | $0.75V_{DD}$ | | 13.5 | V |
| HOLD/P33, RES and OSC1 HIGH-level input voltage | V_{IH2} | Output n-channel transistor OFF | $0.75V_{DD}$ | | V_{DD} | V |
| Ports P0, P1, PC, PD and PE HIGH-level input voltage | V_{IH3} | Output n-channel transistor OFF. See note 1. | $0.7V_{DD}$ | | V_{DD} | V |
| Port PE HIGH-level input voltage | V_{IH4} | Ternary input mode. | $0.8V_{DD}$ | | V_{DD} | V |

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LC66P308

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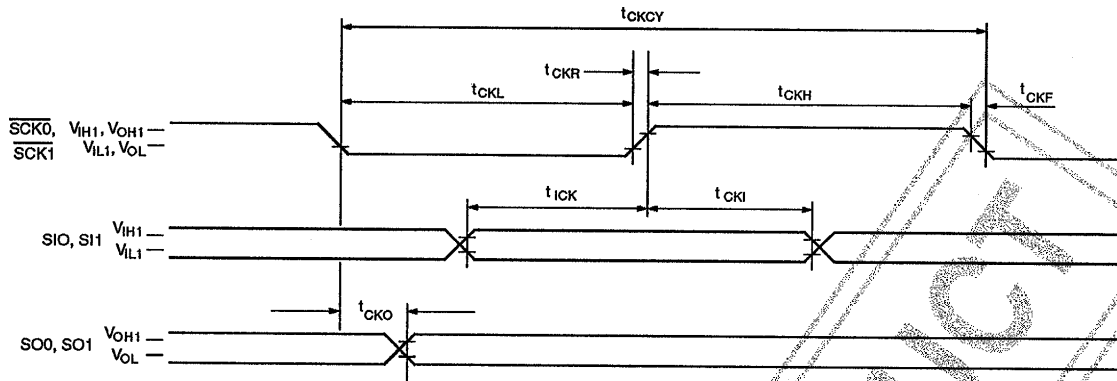
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|------------|--|---------------|-------------|--------------|---------------|
| | | | min | typ | max | |
| Ports P0 to P6 (excluding P33) and PC LOW-level output voltage | V_{OL} | $I_{OL}=1.6\text{mA}$ | | | 0.4 | V |
| | | $I_{OL}=10\text{mA}$ | | | 1.5 | V |
| Ports P2, P3 (excluding P33), P6 and PC HIGH-level output voltage | V_{OH1} | $I_{OH}=-1\text{mA}$. See note 3. | $V_{DD}-1.0$ | | | V |
| | | $I_{OH}=-0.1\text{mA}$. See note 3. | $V_{DD}-0.5$ | | | V |
| Ports P0, P1, P4 and P5 HIGH-level output voltage | V_{OH2} | $V_{DD}=4.5\text{V}$, $I_{OH}=-0.2\text{mA}$. See note 4. | 2.4 | | | V |
| | | $I_{OH}=-0.13\text{mA}$. See note 4. | $V_{DD}-1.35$ | | | V |
| Ports PC and PD in-phase, comparator input voltage | V_{CMM} | | 1.0 | | $V_{DD}-1.5$ | V |
| Port PD comparator offset voltage | V_{OFF} | $V_I=1.0$ to $V_{DD}-1.5\text{V}$ | | ± 50 | ± 300 | mV |
| Ports P2, P3, P5 and P6, and $\overline{\text{RES}}$ and OSC1 Schmitt-trigger LOW-level threshold voltage | V_{tL} | | $0.25V_{DD}$ | | $0.5V_{DD}$ | V |
| Ports P2, P3, P5 and P6, and $\overline{\text{RES}}$ and OSC1 Schmitt-trigger HIGH-level threshold voltage | V_{tH} | | $0.5V_{DD}$ | | $0.75V_{DD}$ | V |
| Ports P2, P3, P5 and P6, $\overline{\text{RES}}$ and OSC1 Schmitt-trigger hysteresis voltage | V_{HYS} | | | $0.1V_{DD}$ | | V |
| LOW-level input current for all inputs | I_{iL} | $V_I=V_{SS}$, output n-channel transistor OFF. See note 2 | -1 | | | μA |
| Ports P2 to P6 (excluding P33) HIGH-level input current | I_{iH1} | $V_I=13.5\text{V}$, output n-channel transistor OFF. See note 2 | | | 5 | μA |
| Ports P0, P1 and P33, and $\overline{\text{RES}}$ and OSC1 HIGH-level input current | I_{iH2} | $V_I=V_{DD}$, output n-channel transistor OFF. See note 1 | | | 1 | μA |
| Ports PC2, PC3, PD and PE HIGH-level input current | I_{iH3} | $V_I=V_{DD}$, output n-channel transistor OFF. See note 1 | | | 1 | μA |
| Ports P2 to P6 output leakage current | I_{OFF1} | $V_I=13.5\text{V}$. See note 2. | | | 5 | μA |
| Ports P0, P1 and PC output leakage current | I_{OFF2} | $V_I=V_{DD}$. See note 2. | | | 1 | μA |
| Ports P0, P1, P4 and P5 output current with pull-up option | I_{PO} | $V_I=V_{SS}$, $V_{DD}=5.5\text{V}$. See note 4. | -1.6 | | | mA |
| Ceramic resonator input frequency | f_{CF} | 4MHz resonator | | 4 | | MHz |
| Ceramic resonator input stabilization time | f_{CFS} | 4MHz resonator | | | 10 | ms |
| RC oscillator input frequency | f_{RC} | $R=2.2\text{k}\Omega\pm 1\%$, $C=100\text{pF}\pm 5\%$ | 2 | 3 | 4 | MHz |
| External RC oscillator capacitance | C_{ext} | | | 100 | | pF |
| External RC oscillator resistance | R_{ext} | | | 2.2 | | k Ω |

Notes

1. Ports with CMOS output configuration option cannot be used as input ports.
2. Open-drain output configuration option
3. CMOS output configuration option
4. Pull-up output configuration option

Timing Characteristics

Serial input/output timing

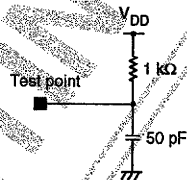


Ta = -30 to +70 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0V

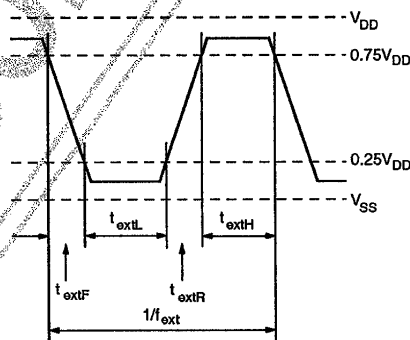
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|-------------------|------------|-------------------|-----|-----|------|
| | | | min | typ | max | |
| Instruction cycle time | t _{CYC} | | 0.92 | | 10 | μs |
| SCK0 and SCK1 serial clock input cycle time | t _{CKCY} | | 0.9 | | | μs |
| SCK0 and SCK1 serial clock output cycle time | t _{OCY} | | 2t _{CYC} | | | μs |
| SCK0 and SCK1 serial clock input pulsewidth | t _{CKL} | | 0.4 | | | μs |
| SCK0 and SCK1 serial clock output pulsewidth | t _{CKH} | | t _{CYC} | | | μs |
| SCK0 and SCK1 serial clock output rise time | t _{CKR} | | | | 0.1 | μs |
| SCK0 and SCK1 serial clock output fall time | t _{CKF} | | | | 0.1 | μs |
| SIO and SI1 serial data setup time | t _{ICK} | | 0.3 | | | μs |
| SIO and SI1 serial data hold time | t _{CKI} | | 0.3 | | | μs |
| SO0 and SO1 serial data output delay | t _{CKO} | | | | 0.3 | μs |

Note

Each test input and output has an RC load as shown in the following figure.



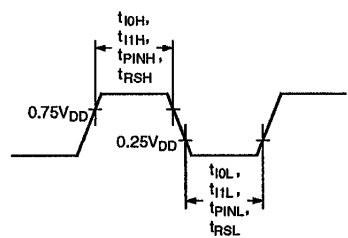
External clock timing



Ta = -30 to +70 °C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|-------------------|------------|---------|-----|------|------|
| | | | min | typ | max | |
| OSC1 external clock input frequency | f _{ext} | | 0.4 | | 4.35 | MHz |
| OSC1 external clock LOW-level input pulsewidth | f _{extL} | | 70 | | | ns |
| OSC1 external clock HIGH-level input pulsewidth | f _{extH} | | 70 | | | ns |
| OSC1 external clock input rise time | f _{extR} | | | | 30 | ns |
| OSC1 external clock input fall time | f _{extF} | | | | 30 | ns |

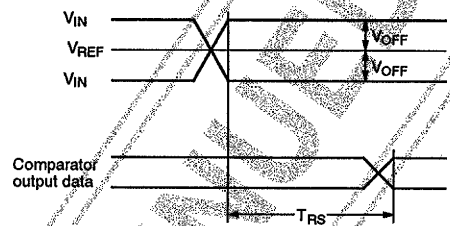
Interrupt and reset timing



Ta = -30 to +70 °C, VDD = 4.5 to 5.5 V, VSS = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-------------------------------------|--------|------------|---------|-----|-----|------|
| | | | min | typ | max | |
| INT0 LOW-level pulsewidth | tIOL | | 2tCYC | | | μs |
| INT0 HIGH-level pulsewidth | tIOH | | 2tCYC | | | μs |
| INT1 and INT2 LOW-level pulsewidth | tI1L | | 2tCYC | | | μs |
| INT1 and INT2 HIGH-level pulsewidth | tI1H | | 2tCYC | | | μs |
| PIN1 LOW-level input pulsewidth | tPINL | | 2tCYC | | | μs |
| PIN1 HIGH-level input pulsewidth | tPINH | | 2tCYC | | | μs |
| RES LOW-level input pulsewidth | tRSL | | 3tCYC | | | μs |
| RES HIGH-level input pulsewidth | tRSH | | 3tCYC | | | μs |

Comparator timing



Ta = -30 to +70 °C, VDD = 4.5 to 5.5 V, VSS = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------------|--------|------------|---------|-----|-----|------|
| | | | min | typ | max | |
| Port PD comparator response time | tRS | | | | 30 | μs |

LC66P308

Input and Output Functions

The LC66P308 has many multiplexed pins whose function is controlled by software. The function of each of these pins is shown in the following table.

| Name | Function |
|----------------|--|
| D0/P00 | Ports P00 to P03 can be addressed as either a 4-bit port or four, single-bit ports. They function as data bus lines when memory is addressed. They also have halt-mode control functions. Level after reset is set by user option. |
| D1/P01 | |
| D2/P02 | |
| D3/P03 | |
| D4/P10 | Ports P10 to P13 can be addressed as either a 4-bit port or four, single-bit ports. They function as data bus lines when memory is addressed. Level after reset is set by user option. |
| D5/P11 | |
| D6/P12 | |
| D7/P13 | |
| A0/SIO/P20 | Ports P20 to P23 can be addressed as either a 4-bit port or four, single-bit ports. They function as address bus inputs when memory is addressed. Port P20 also functions as a serial data input, P21 as a serial data output, P22 as a serial data clock and P23 as an interrupt request, pulsewidth measurement and event counter input using timer 0. |
| A1/SO0/P21 | |
| A2/SCK0/P22 | |
| A3/INT0/P23 | |
| A4/INT1/P30 | Ports P30 to P32 can be addressed as either a 3-bit port, a 4-bit port with P33 or three, single-bit ports. They function as address bus inputs when memory is addressed. Port P30 also functions as an interrupt request input, P31 as a square-wave output from timer 0 and P32 as a square-wave output from timer 1 and a PWM output. |
| A5/POUT0/P31 | |
| A6/POUT1/P32 | |
| HOLD/P33 | |
| A7/P40 | Ports P40 to P43 can be addressed as either a 4-bit port, four, single-bit ports or an 8-bit port with P50 to P53. They function as address bus inputs when memory is addressed. |
| A8/P41 | |
| A9/P42 | |
| A10/P43 | |
| A11/P50 | Ports P50 to P53 can be addressed as either a 4-bit port, four, single-bit ports or an 8-bit port with P40 to P43. Ports P50 to P52 function as address bus inputs when memory is addressed. Port P53 also functions as an interrupt request input. |
| A12/P51 | |
| A13/P52 | |
| INT2/P53 | |
| SI1/P60 | Ports P60 to P63 can be addressed as either a 4-bit port or four, single-bit ports. Port P60 also functions as a serial data input, P61 as a serial data output, P62 as a serial data clock and P63 as a data security control input and timer 1 event counter input. |
| SO1/P61 | |
| SCK1/P62 | |
| DASEC/PIN1/P63 | |
| PC2/VREF0 | Ports PC2 and PC3 can be addressed as either a 2-bit port or two, single-bit ports. In addition, Port PC2 also functions as the PD0 reference voltage input, and PC3 as the PD1 to PD3 reference voltage input. |
| PC3/VREF1 | |
| PD0/CMP0 | Ports PD0 to PD3 can be addressed as either a 4-bit port or four, single-bit ports. They also function as comparator inputs. In addition, port PD3 also functions as the memory program control input. |
| PD1/CMP1 | |
| PD2/CMP2 | |
| PD3/CMP3/PGM | |
| PE0/TRA/CE | Ports PE0 to PE1 can be addressed as either a 2-bit port or two, single-bit ports. They function as chip enable and write enable, respectively, when memory is addressed. They also function as three-level inputs. |
| PE1/TRB/OE | |
| OSC1 | OSC1 and OSC2 function as the external ceramic resonator or RC oscillator connections. When an external clock is used, OSC2 is left open. |
| OSC2 | |
| RES | When $\overline{\text{RES}}$ goes LOW while $\overline{\text{HOLD/P33}}$ is HIGH, the CPU is reset. |
| VPP/TEST | CPU test input. Normally connected to ground. |

User Options

Oscillator Options

There are three user options for the oscillator—an external clock, an RC oscillator and a ceramic resonator. The internal circuits of OSC1 and OSC2 for the external clock, RC oscillator and ceramic resonator options are shown in figures 1, 2 and 3, respectively. Note the Schmitt-trigger inputs for both the external clock and RC oscillator options.



Figure 1. External clock option

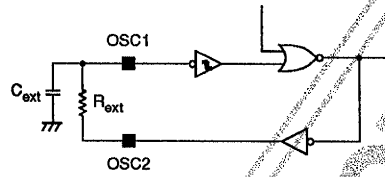


Figure 2. RC oscillator option

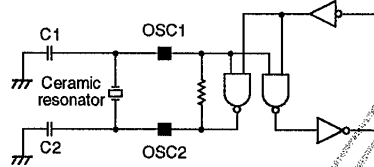


Figure 3. Ceramic resonator option

Output Options

There are two user options for the output configuration of each port—n-channel open drain and p-channel, active pull-up, shown in figures 4 and 5, respectively. Ports P2, P3, P5 and P6 have Schmitt-trigger inputs in both output configurations.

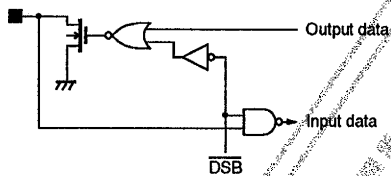


Figure 4. N-channel open-drain option

The p-channel pull-up option for ports P0, P1, P4 and P5 results in an n-channel sink transistor with a p-channel, active pull-up transistor configuration, and for ports P2, P3, P6 and PC, a CMOS configuration.

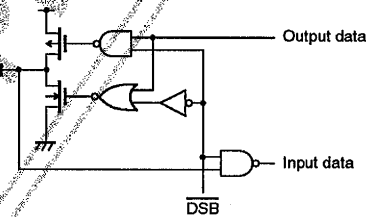


Figure 5. P-channel pull-up option

The n-channel open-drain outputs for ports P2 to P6 have a withstand voltage greater than 15 V.

Output Level After Reset Option

The output level of ports P0 and P1 after a CPU reset is user selectable.

Watchdog Timer Option

A watchdog timer is available to prevent program run-away.

PROM Specification

Specifying Programs and Options

The user-addressable memory is 0000H to 2007H. Addresses 0000H to 1FFFH are for user programs, and addresses 2000H to 2007H, for option specification.

Addresses 2008H and above can neither be programmed or read. The option specification is coded using the information shown in the following table.

| Address | Data bit | Parameter | Option | | |
|---------|----------|-------------------------------|---------------------------------|-------------------|----------|
| | | | 0 | 1 | |
| 2000H | D0 | Watchdog timer function | No | Yes | |
| | D1 | Port P0 level after reset | LOW | HIGH | |
| | D2 | Port P1 level after reset | LOW | HIGH | |
| | D3 | No function | Set to 0 | | |
| | D4 | Oscillator | RC oscillator or external clock | Ceramic resonator | |
| | D5 to D7 | No function | Set to 0 | | |
| 2001H | D0 | Port P00 output configuration | Open-drain | Pull-up | |
| | D1 | Port P01 output configuration | | | |
| | D2 | Port P02 output configuration | | | |
| | D3 | Port P03 output configuration | | | |
| | D4 | Port P10 output configuration | Open-drain | Pull-up | |
| | D5 | Port P11 output configuration | | | |
| | D6 | Port P12 output configuration | | | |
| | D7 | Port P13 output configuration | | | |
| 2002H | D0 | Port P20 output configuration | Open-drain | CMOS | |
| | D1 | Port P21 output configuration | | | |
| | D2 | Port P22 output configuration | | | |
| | D3 | Port P23 output configuration | | | |
| | D4 | Port P30 output configuration | Open-drain | CMOS | |
| | D5 | Port P31 output configuration | | | |
| | D6 | Port P32 output configuration | | | |
| | D7 | No function | | | Set to 0 |
| 2003H | D0 | Port P40 output configuration | Open-drain | Pull-up | |
| | D1 | Port P41 output configuration | | | |
| | D2 | Port P42 output configuration | | | |
| | D3 | Port P43 output configuration | | | |
| | D4 | Port P50 output configuration | Open-drain | Pull-up | |
| | D5 | Port P51 output configuration | | | |
| | D6 | Port P52 output configuration | | | |
| | D7 | Port P53 output configuration | | | |
| 2004H | D0 | Port P60 output configuration | Open-drain | CMOS | |
| | D1 | Port P61 output configuration | | | |
| | D2 | Port P62 output configuration | | | |
| | D3 | Port P63 output configuration | | | |
| | D4 to D7 | No function | Set to 0 | | |
| 2005H | D0 to D7 | No function | Set to 0 | | |
| 2006H | D0 to D7 | No function | Set to 0 | | |
| 2007H | D0, D1 | No function | Set to 0 | | |
| | D2 | Port PC2 output configuration | Open-drain | CMOS | |
| | D3 | Port PC3 output configuration | | | |
| | D4 to D7 | No function | Set to 0 | | |

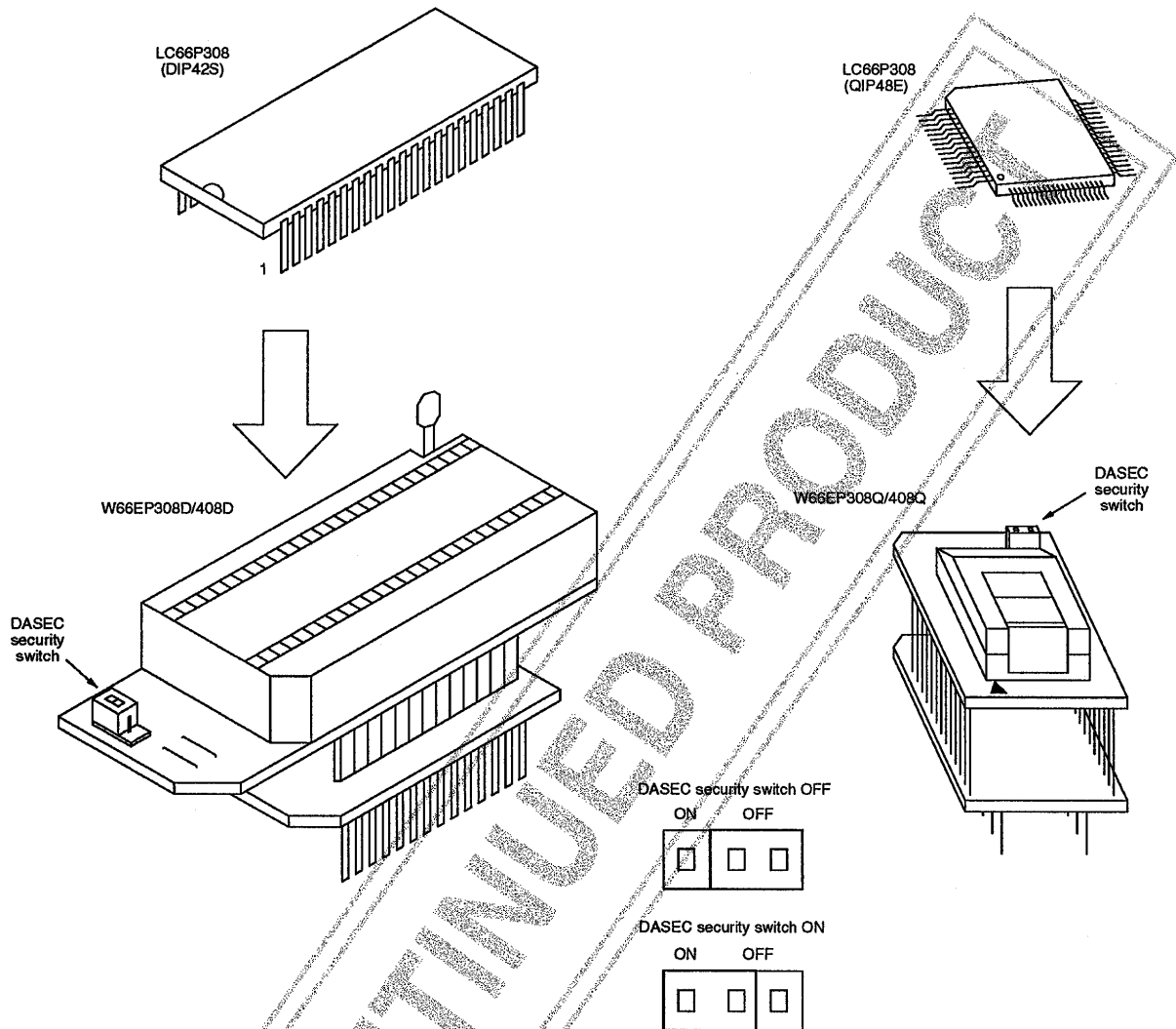
The assembler execute command when specifying programs and options using a SANYO cross assembler is LC66S.EXE.

LC66P308

PROM Programming

The PROM can be programmed using a special adapter board, W66EP308D/408D for the 42-pin DIP and

W66EP308Q/408Q for the 48-pin QIP as shown in the following figure, and a universal EPROM programmer.



Program the LC66P308 using the M mode of the PV command of the EVA800 or EVA850. The EPROM programmer should be Intel 27128 compatible with $V_{PP} = 21\text{ V}$. The recommended programmers are shown in the following table. Please contact your nearest SANYO representative if you intend to use an alternative EPROM programmer.

| Manufacturer | Model |
|--------------|--|
| ADVANTEST | TR4943, R4944A, R4945 or equivalent |
| SANYO | EVA850 or EVA800 special-purpose Programmers |

Notes

1. Intel is a registered trademark of Intel Corporation.
2. ADVANTEST is a registered trademark of ADVANTEST Corporation.

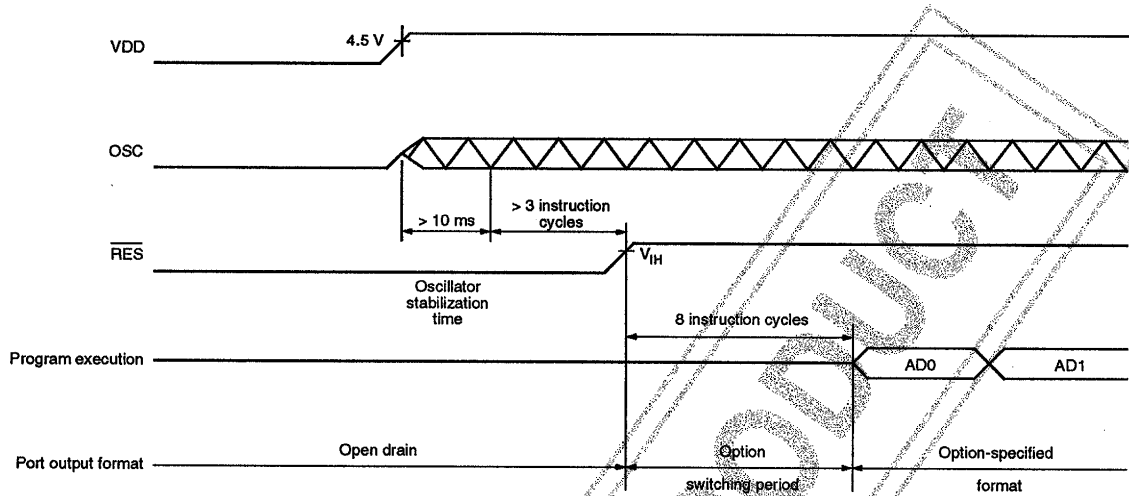
The EPROM programmer adapter incorporates a data security switch. When this switch is ON, data is secure, and when OFF, the data lines are floating and the PROM can be programmed. Note that when the data lines are floating, the EPROM programmer will return an error. This error can be ignored.

Application Notes

Reset Timing

The reset signal on $\overline{\text{RES}}$ should be held LOW for a minimum of three instruction cycles after the oscillator has

stabilized to ensure correct operation, as shown in the following figure.



After a reset occurs, all I/O ports are reset to open-drain output configuration with floating outputs, except for ports P0 and P1 which both have an output level after reset option. The output configuration of each port is then set using the specified options during the eight instruction cycles after $\overline{\text{RES}}$ goes HIGH. Program execution then begins from address 0000H.

The LC66E308/P308 can be reset while in hold mode ($\overline{\text{HOLD/P33}}$ is LOW). When $\overline{\text{RES}}$ goes LOW in hold mode, $\overline{\text{HOLD/P33}}$ must go HIGH before $\overline{\text{RES}}$ goes HIGH again.

Reference Clock

The external circuit for a ceramic resonator is shown in figure 6, and the recommended resonator and component values, in the following table. The oscillator stabilization characteristics are shown in figure 7.

| Ceramic resonator | Capacitance | |
|---|---------------|---------------|
| | C1 | C2 |
| 4 MHz Murata CSA -4.00MG | 33 pF ±10% | 33 pF ±10% |
| 4 MHz Kyocera KBR -4.0MS | 33 pF ±10% | 33 pF ±10% |
| 4 MHz Murata CST -4.00MG with internal capacitor | N/A | N/A |
| 4 MHz Kyocera KBR -4.0MES with internal capacitor | N/A | N/A |

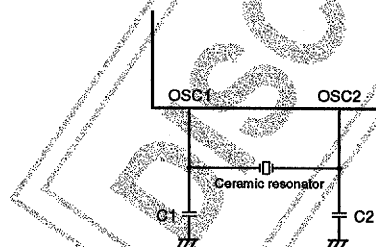


Figure 6. Ceramic resonator

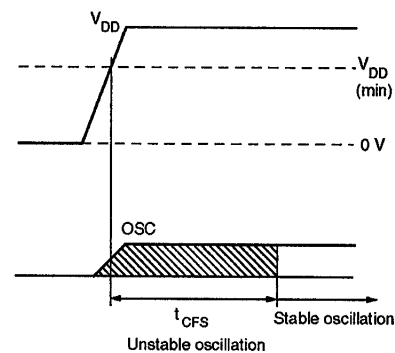
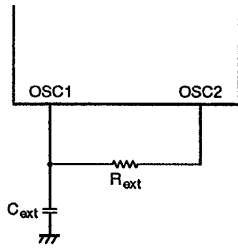
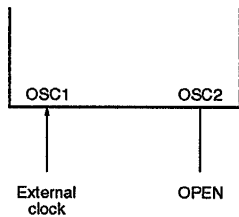


Figure 7. Ceramic resonator stabilization time

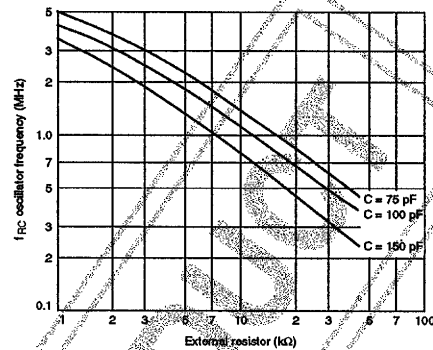
The external circuit for an RC oscillator is shown in the following figure.



The external clock input connection is OSC1. The remaining oscillator connection, OSC2, should be left open as shown in the following figure.



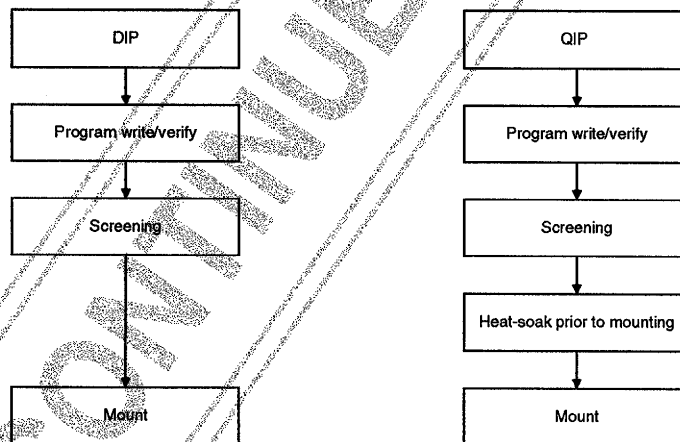
The RC oscillator frequency is determined by the external resistor and capacitor and has only been specified for $R_{ext} = 2.2 \text{ k}\Omega$ and $C_{ext} = 100 \text{ pF}$. The frequency for other values of R_{ext} and C_{ext} can be determined from the graph in the following figure.



Preparation Procedure

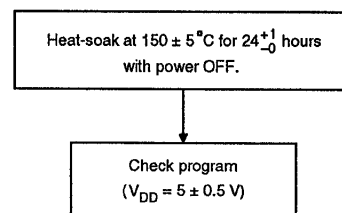
The preparation procedures shown in the following figure for DIP and QIP packages should always be followed prior to mounting the packages on the substrate. Note that

the QIP package should be heat-soaked for 24 hours at 125°C immediately prior to mounting.



Screening procedure

The construction of the microcontroller with a blank built-in PROM makes it impossible for SANYO to completely factory-test it before shipping. To prove reliability of the programmed devices, the screening procedure shown in the following figure should always be followed.



Note that it is not possible to perform a write test on the blank PROM. 100% yield, therefore, cannot be guaranteed.

LC66P308

Ordering Information

When ordering identical mask ROM and PROM devices simultaneously, provide an EPROM containing the target memory contents together with separate order forms for each of the mask ROM and PROM versions.

When ordering a PROM device, provide an EPROM containing the target memory contents together with an order form. When ordering either an LC66354A 4 Kbyte or LC66356A 6 Kbyte mask ROM device, insert a jump command, or any similar command, to avoid executing an address beyond the range of the target device. In addition, write a 0 into all locations above 2007H.

A comparison of the LC66P308 characteristics with those of the LC663XX mask ROM devices is shown in the following table.

| Parameter | Symbol | Condition | LC66P308 | LC663XX series | | Unit |
|---|-------------------|--|------------|--------------------------|--------------------------|--------|
| | | | | LC6630X series | LC66354A/6A/8A | |
| Supply voltage range | V _{DD} | t _{CYC} =0.92 to 10μs | 4.5 to 5.5 | 4.0 to 6.0 | — | V |
| | | t _{CYC} =3.92 to 10μs | — | — | 2.2 to 5.5 | |
| | | t _{CYC} =1.96 to 10μs | — | — | 3.0 to 5.5 | |
| Maximum halt-mode supply current | I _{DDHT} | 4MHz ceramic resonator | 5.0 | 2.5 | 2.5 | mA |
| | | 4MHz external clock | 6.0 | 3.5 | 3.5 | |
| | | 3MHz (typ) RC oscillators | 5.0 | 2.5 | — | |
| Hold-mode release hardware delay | N _{HOLD} | | 65,536 | 65,536 | 16,384 | Cycles |
| Hold-mode release time | t _{HOLD} | f _{OSC} =4MHz (t _{CYC} =1μs) | ≈ 64 | ≈ 64 | — | ms |
| | | f _{OSC} =2MHz (t _{CYC} =2μs) | — | — | ≈ 32 | |
| | | f _{OSC} =1MHz (t _{CYC} =4μs) | — | — | ≈ 64 | |
| External RC oscillator capacitance | C _{ext} | | 100 | 100 | — | pF |
| External RC oscillator resistance | R _{ext} | | 2.2 | 2.7 | — | kΩ |
| Timer 0 contents after reset or hold-mode release | | | FF0 | FF0 | FFC | Hex |
| Port output configuration after reset | | | See note. | Specified by user option | Specified by user option | |

Note

Ports P2 to P6 and PC are open-drain and floating. Ports P0 and P1 have pull-up resistances and are HIGH or LOW.

A breakdown of the LC66 series devices, which includes the LC66308 and LC663XX devices, is shown in the following table.

| Device | Pins | ROM capacity | RAM capacity | Package type |
|--|-------|---------------------|--------------|------------------|
| LC66304A/306A/308A | 42/48 | 4/6/8 Kbyte ROM | 512 bytes | DIP42S or QIP48E |
| LC66354A/356A/358A | 42/48 | 4/6/8 Kbyte ROM | 512 bytes | DIP42S or QIP48E |
| LC6635S [▽] /356S [▽] /358S [▽] | 44 | 4/6/8 Kbyte ROM | 512 bytes | QIP44M |
| LC66 E308 | 42/48 | 8 Kbyte EPROM | 512 bytes | DIP42S or QIP48E |
| LC66 P308 | 42/48 | 8 Kbyte PROM | 512 bytes | DIP42S or QIP48E |
| LC66404A/406A/408A | 42/48 | 4/6/8 Kbyte ROM | 512 bytes | DIP42S or QIP48E |
| LC66 E408 | 42/48 | 8 Kbyte EPROM | 512 bytes | DIP42S or QIP48E |
| LC66 P408 | 42/48 | 8 Kbyte PROM | 512 bytes | DIP42S or QIP48E |
| LC66506B/508B/512B/516B | 64 | 6/8/12/16 Kbyte ROM | 512 bytes | DIP64S or QIP64A |
| LC66556A/558A/562A/566A | 64 | 6/8/12/16 Kbyte ROM | 512 bytes | DIP64S or QIP64E |
| LC66E516 | 64 | 16 Kbyte EPROM | 512 bytes | DIP64S or QIP64E |
| LC66P516 | 64 | 16 Kbyte PROM | 512 bytes | DIP64S or QIP64E |

Note

▽ = under development

SANYO ROM Services

SANYO offers various services at nominal charges. These include ROM writing, ROM reading, and package stamping and screening. Contact your local SANYO representative for further information.

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