

**SANYO****LC573010A, 573015A****4-bit Single Chip Microcontroller****Overview**

LC573010A and LC573015A are CMOS 4-bit microcontroller featuring low-voltage operation and low power dissipation.

Both LC573010A and LC573015A incorporate a 4-bit parallel processing ALU, 1 K bytes/1.5 K bytes ROM, a 32 × 4-bit RAM, a 16-bit timer, and an infrared remote control transmission carrier output circuit.

**Applications**

- Remote controller
- Control of small measuring instruments

**Features**

- ROM : 1024 × 8 bits (LC573010A)  
1536 × 8 bits (LC573015A)
- RAM : 32 × 4 bits
- Cycle time

Cycle time	System clock generator	Oscillation frequency	Supply voltage
17.6 $\mu$ sec	Ceramic oscillation circuit	455 kHz	2.3 to 6.0 V

- Current dvain

At normal operation

Current drain	System clock generator	Oscillation frequency	Supply voltage
150 $\mu$ A typ	CR oscillation	455 kHz	3.0 V
400 $\mu$ A typ	CR oscillation	455 kHz	5.0 V

HALT mode

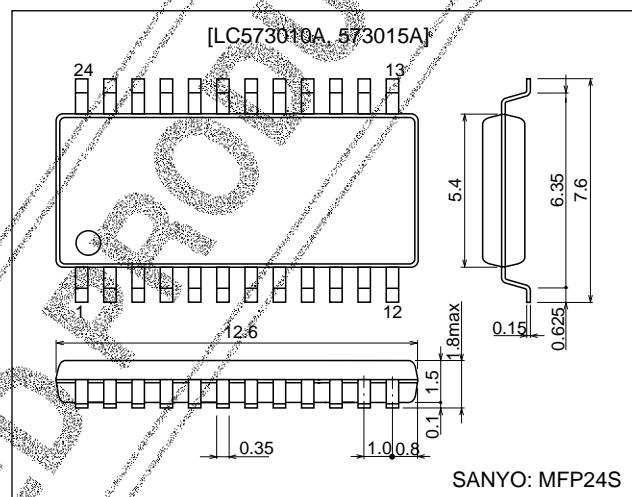
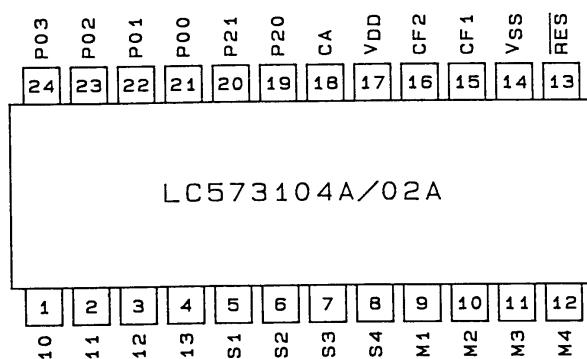
Current drain	System clock generator	Oscillation frequency	Supply voltage
80 $\mu$ A typ	CR oscillation	455 kHz	3.0 V
300 $\mu$ A typ	CR oscillation	455 kHz	5.0 V

HOLD mode

Leakage current	Condition	Oscillation frequency	Supply voltage
0.1 $\mu$ A typ	When CR oscillation is at STOP mode	455 kHz	5.0 V

**Package Dimensions**

unit: mm

**3112-MFD24S****Pin Assignment**

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**SANYO Electric Co.,Ltd. Semiconductor Business Headquarters**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

82198RM (OT) No. 5899-1/12

- Port

- Input port (S port, M port) : 2-port (8 pins) [Key scan input port]
- Input/Output port : 3-port (10 pins)
  - P0 port, P1 port 2-port (8 pins) [Key scan output port]
  - P2 port 1-port (2 pins) [Key scan expansion port]  
[LED direct drivable port]

- Infrared remote control carrier generation circuit

- Software-controllable remote control carrier output ON/OFF.
- Software-controllable carrier frequency and duty ratio.  
<38 kHz-1/3 duty, 38 kHz-1/2 duty, 57 kHz-1/2 duty>  
(When fixed carrier signal is output, it is specified by mask option)
- 1 kHz to 200 kHz infrared remote control transmission carrier frequency,  
(When carrier output is selected by timer at mask option, and when 455 kHz CR oscillator is used)
- Infrared carrier output-dedicated terminal built-in (CA terminal).
- 108 ms HALT-mode cancel signal output.

- Timer

- 16-bit software-controllable timer
  - Timer input clock : Ceramic (CR) oscillation frequency (455 kHz)
  - 108 ms HALT release request signal generation timer (Free running timer)
  - Watchdog timer (changed over between USED/UNUSED by mask option)

- Sub-routine stack level

- 2 levels

- Oscillation circuit

- Ceramic (CR) oscillation circuit : 455 kHz (for System clock generation), feedback resistor built-in.

- Standby function

- HALT mode

HALT mode used to reduce current drain.

HALT mode suspends program execution.

Following shows how to release the HALT mode.

(A) System reset

(B) HALT mode release request signal

- HOLD mode

HOLD mode stops ceramic resonator (CR). The HOLD mode can be released in two ways.

(A) System reset

(B) Apply H level input to S port pin or M port pin. (However, it is necessary to set S port or M port HOLD mode release permission flag beforehand.)

- Form of shipment

- MFP-24S (1.0 mm pitch)

Note : When dipping in solder to mount the MFP package on board, contact SANYO for instructions.

## The Application Development System for the LC573100 Series.

### Manual

- (1) Users Manual : LC573100 Series Users Manual
- (2) Development Tool Manual : LC573100 Series Development Tool Manual

### Development Tools

- Tools for application development of the LC573100 Series
  - (1) Personal computer (MS-DOS based)
  - (2) Cross assembler (LC573100.EXE)
  - (3) Mask option generator (SU573100.EXE)
- Tools to evaluate application development of the LC573100 Series.
  - (1) EVA chip (LC5797)

Note : 1 As RAM capacity differs between EVA chip (LC5797) and the LC573100 Series, always check before programming and debugging.

LC573010A/LC573015S :  $64 \times 4$  bits

LC5797 :  $256 \times 4$  bits

Note : 2 Always keep the DPH value in mind when programming. Only DPH '0' to '3' may be used as the RAM address.

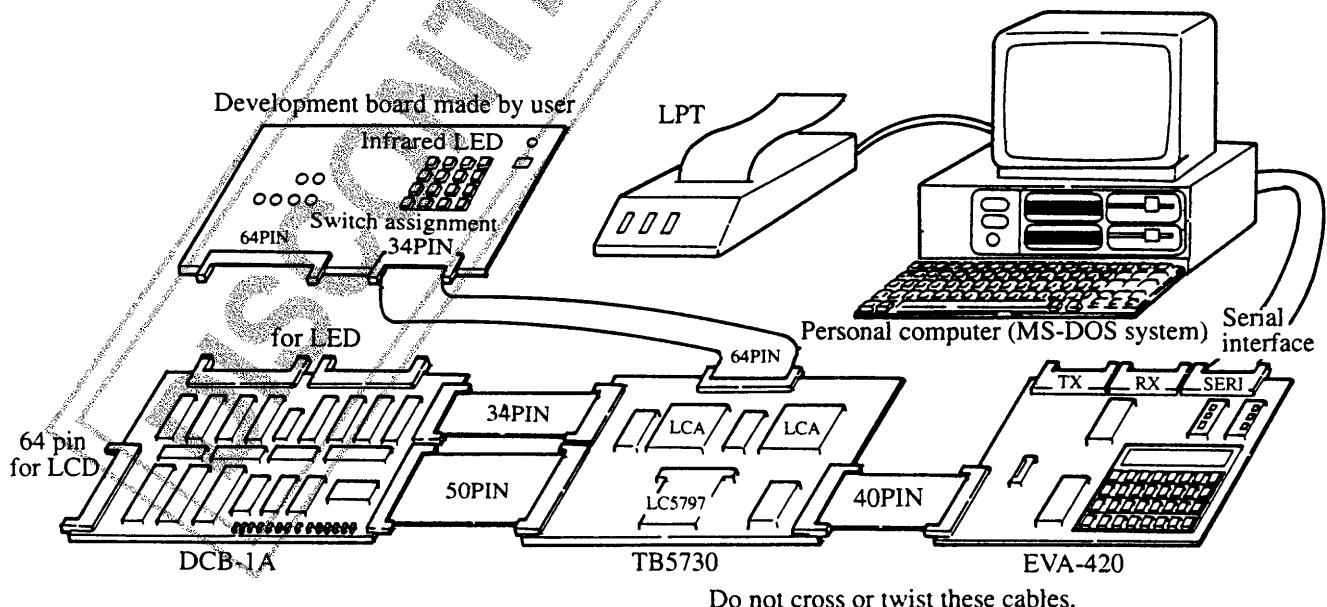
If DPH other than '0' to '3' is used as RAM address when programming, SANYO will not be liable for any trouble caused.

(2) EVA chip board (TB5730)

Note : The application evaluation board is the evaluation board made by the user.

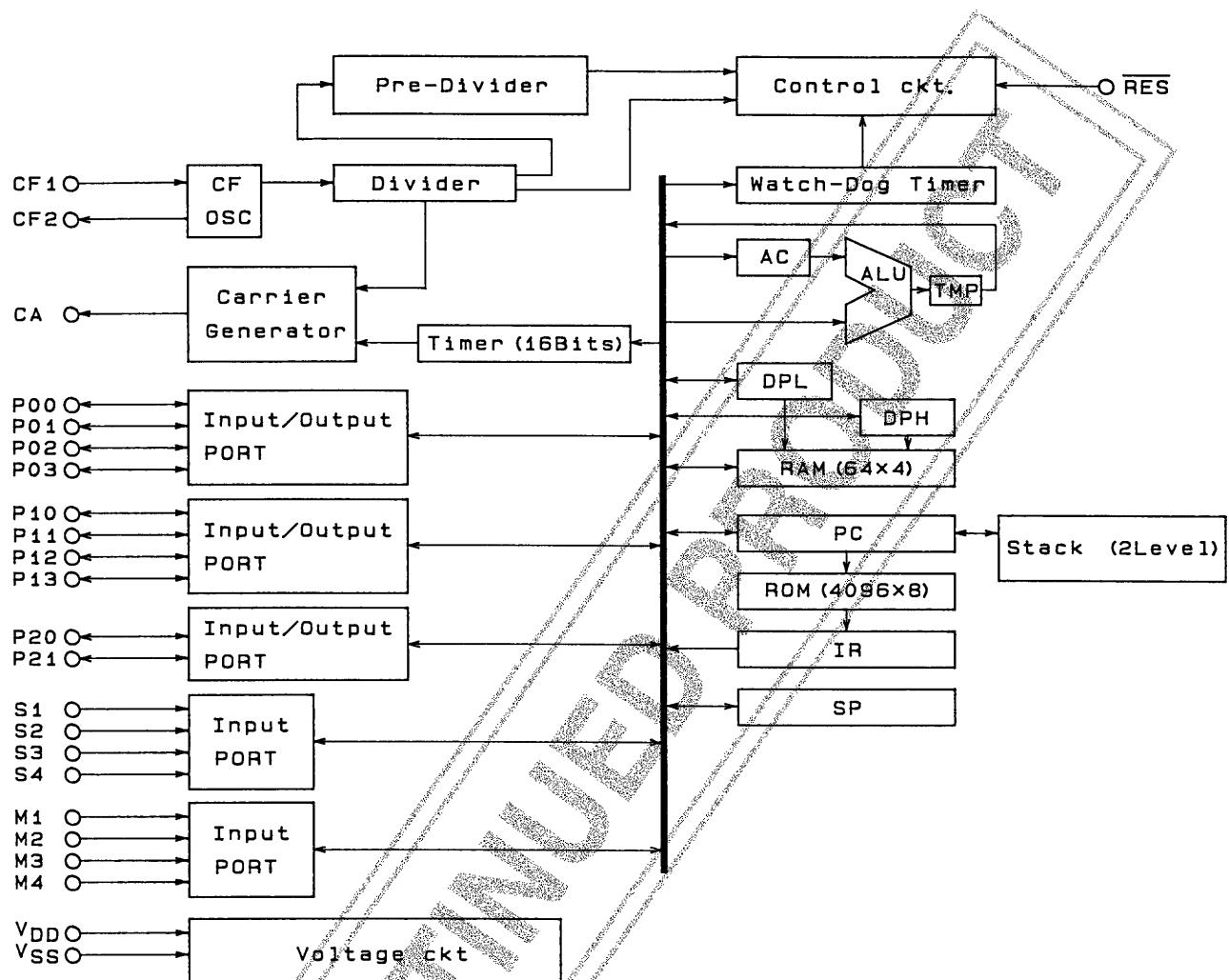
(3) Evaluation board [EVA420 (Monitor ROM : ER-573000)]

(4) Display and mask option data control board [DCB-1A (REV3.6)]

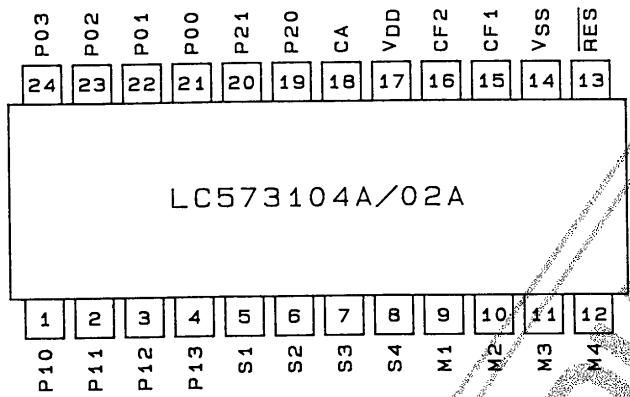


## Development Support System Outline

## Block Diagram



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**Pin Assignment****Pin Functions**

MFP24S Pin no.	Pin name	Input/ output	Function description	Option	Reset status
17	V <sub>DD</sub>	—	Supply voltage. See Figure 1.		
14	V <sub>SS</sub>	—	Ground. See Figure 1.		
15	CF1	Input	Used for system clock oscillation • 455 kHz ceramic resonator is connected between CF1 and CF2 for oscillation.		
16	CF2	Output	• Stops oscillation when receiving CR oscillation stop command.		
5 6 7 8	S1 S2 S3 S4	Input	Input port S. • LSI system is reset by charging V <sub>DD</sub> to S1 to S4 simultaneously. (Mask option) • Data is loaded in accumulator.	(1) Low level HOLD Tr YES/NO (2) Reset by S1 to S4.	• Pull-down resistor ON • Reset signal ENABLE
9 10 11 12	M1 M2 M3 M4	Input	Input port M. Data loaded in accumulator	Low level HOLD Tr YES/NO	• Pull-down resistor ON
21 22 23 24	P00 P01 P02 P03	Input/ output	Input/output port • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch open drain output)		
1 2 3 4	P10 P11 P12 P13	Input/ output	Input/output port • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch open drain output)		
19 20	P20 P21	Input/ output	Input/output port • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch open drain output) • LED direct drivable pin		
18	CA	Output	Remote control carrier output.	Fixed carrier output/carrier output by timer	• At reset low level • At fixed carrier output 38 kHz- 1/3 duty
13	RES	Input	Reset input. Internal pull-up resistor.		

Supply Connections

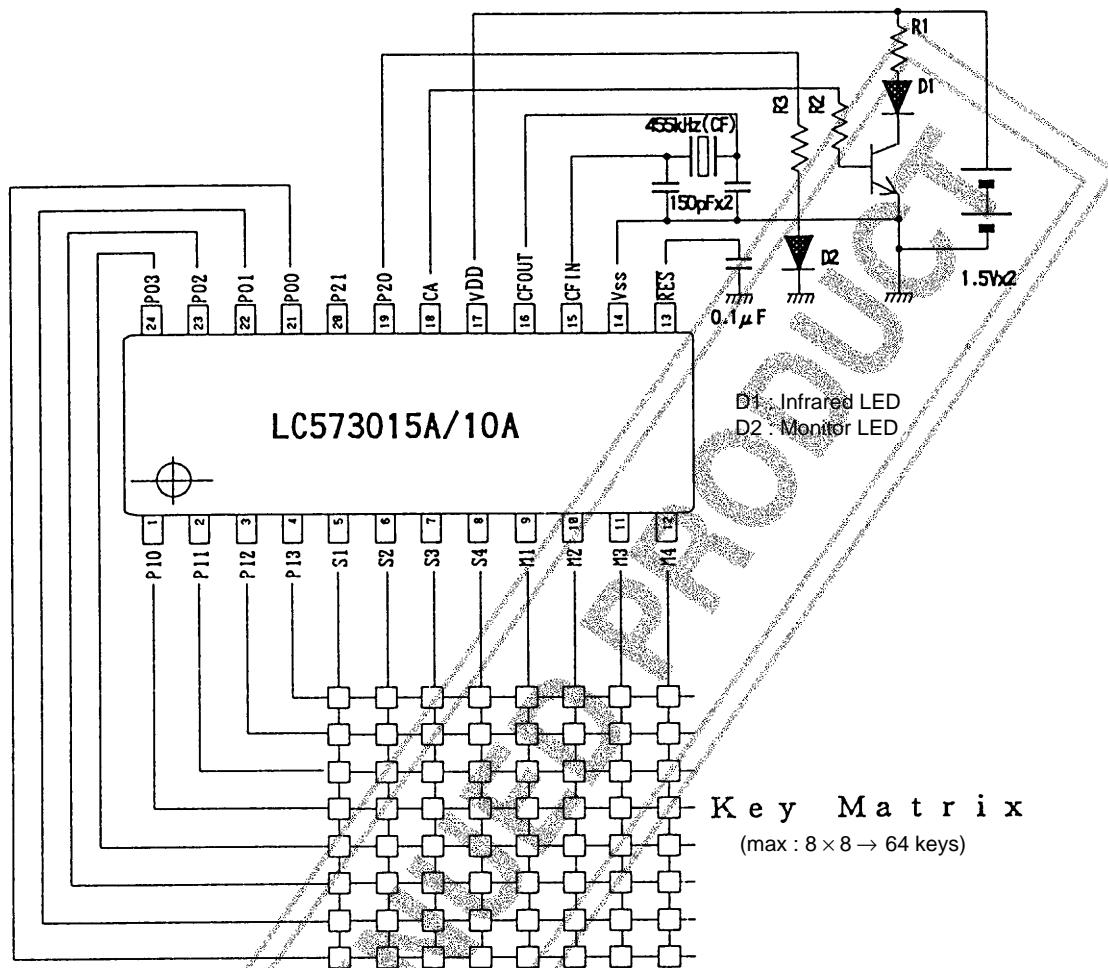


Figure 1 Supply Connections

**Mask Option**

Input port option

Option	Circuit	Remarks
Low level hold Tr selection	<p>The circuit shows a logic inverter with its output connected to one terminal of a switch. The other terminal of the switch is connected to ground through a resistor. The control terminal of the switch is labeled "'L' level Hold Tr'. A dashed box highlights the switch and its control logic.</p>	<p>Next port switches over in sequence</p> <ul style="list-style-type: none"> <li>• S1 to S4, M1 to M4 Input signal level Hold Tr selection</li> <li>• Low level hold Tr used</li> <li>• Low level hold Tr not used</li> </ul> <p>A00433</p>

Reset signal option by S port

Option	Circuit	Remarks
Resetting IC by S port	<p>The circuit includes a resistor and a diode connected to the RES pin. The RES pin is connected to the inputs of two inverters. The outputs of these inverters are connected to the inputs of a 4-to-1 multiplexer. The select inputs of the multiplexer are S1, S2, S3, and S4. The output of the multiplexer is connected to the IC system reset pin. A label 'Mask option' points to the multiplexer. A label 'Turn power ON to reset' points to a logic inverter.</p>	<p>Selects signal for resetting IC system by simultaneously charging High level to S1 to S4.</p> <ul style="list-style-type: none"> <li>• Allow</li> <li>• Prohibit</li> </ul>

Carrier standard clock generation circuit option for remote control

Option	Circuit	Remarks
38/57 kHz	<p>The circuit shows a control register 4 interface with bits CRSEL1 and CRSEL0. These bits control three parallel carrier generation paths. Each path consists of a 38kHz-1/3Duty carrier generation circuit, a 38kHz-1/2Duty carrier generation circuit, and a 57kHz-1/2Duty carrier generation circuit. The outputs of these three paths are combined via an OR gate. This signal, along with a Mask option signal, controls a CARRIER ON/OFF CONTROL logic. The output of this logic is the CA pin. Below the main logic, a Timer 8-bit counter, Comparison circuit, and Timer counter setting register are shown. A 1/2 divider is also present.</p>	<p>Software-controllable carrier frequency and duty.</p> <ul style="list-style-type: none"> <li>• Following carrier frequency and duty may be selected by setting control register 4.             <ul style="list-style-type: none"> <li>(1) 38 kHz-1/3 duty</li> <li>(2) 38 kHz-1/2 duty</li> <li>(3) 57 kHz-1/2 duty</li> </ul> </li> </ul>
Timer 8-bit overflow	<p>This row provides a detailed view of the timer circuit. It shows the Timer counter setting register, Comparison circuit, and Timer 8-bit counter. The output of the Timer 8-bit counter is fed into a 1/2 divider. The output of the 1/2 divider is connected to the Comparison circuit. The output of the Comparison circuit is connected to the Mask option input of the main carrier generation logic.</p>	<p>Timer 8-bit overflow signal generates carrier signal for infrared remote control. Fixed 1/2 duty</p>

## Watchdog timer circuit option

Option	Circuit	Remarks
Watchdog timer selection		Watchdog timer used/unused selection

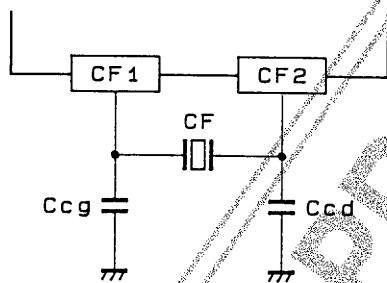
## Specifications

Absolute Maximum Ratings at  $T_a = \pm 25 + 2^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$ 

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	$V_{DD}$		-0.3 to +7.0	V
Input voltage range	$V_{IN}$	S1 to S4, M1 to M4, RES, P00 to P03, P10 to P13, P20, P21, CF1 (P00 to P03, P10 to P13, P20, P21 are input mode)	-0.3 to $V_{DD} + 0.3$	V
Output voltage range	$V_{OUT}$	CA, P00 to P03, P10 to P13, P20, P21, CF2 (P00 to P03, P10 to P13, P20, P21 are output mode)	-0.3 to $V_{DD} + 0.3$	V
Output current (Per 1 pin)	$I_{OUT1}$	CA (per 1 pin)	25	mA
	$I_{OUT2}$	P00 to P03, P10 to P13 (per 1 pin)	500	$\mu\text{A}$
	$I_{OUT3}$	P20, P21 (per 1 pin)	10	mA
	$I_{OUT4}$	Output pins other than listed above (per 1 pin)	500	$\mu\text{A}$
Total output current of all pins except CA	$I_{ALL}$	All pins totalled (except for CA pin)	25	mA
Operating temperature range	$T_{opr}$		-30 to +70	$^\circ\text{C}$
Storage temperature range	$T_{stg}$		-40 to +125	$^\circ\text{C}$

**Recommended Operating Range at  $T_a = -30$  to  $+70^\circ\text{C}$ ,  $V_{SS} = 0 \text{ V}$** 

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$		2.3		6.0	V
Input high level voltage	$V_{IH1}$	S1 to S4, M1 to M4, P00 to P03, P10 to P13, P20, P21 (P0, P1, P2 ports are input mode)	$0.7V_{DD}$		$V_{DD}$	V
Input low level voltage	$V_{IL1}$		$V_{SS}$		$0.3V_{DD}$	V
Input high level voltage	$V_{IH2}$	$\overline{\text{RES}}$	$0.75V_{DD}$		$V_{DD}$	V
Input low level voltage	$V_{IL2}$		0		$0.25V_{DD}$	V
Operation frequency	$f_{OPG}$	At CR oscillation, Figure.2	380	455	500	kHz

**Figure.2 : CR Oscillation Circuit**

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## LC573010A, 573015A

### Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input impedance	$R_{IN1A}$	$V_{DD} = 2.9 \text{ V}$ , $V_{IL} = 0.4 \text{ V}$ , S1 to S4, M1 to M4: Low level hold Tr, Figure 3	150	300	1000	$\text{k}\Omega$
	$R_{IN1B}$	$V_{DD} = 2.9 \text{ V}$ , $V_{IL} = 0.4 \text{ V}$ , S1 to S4, M1 to M4: Low level pull-down Tr, Figure 3	30	50	100	$\text{k}\Omega$
	$R_{IN2}$	$V_{DD} = 2.9 \text{ V}$ , $V_{IH} = V_{DD}$ , $\bar{R}_{ES}$	10		300	$\text{k}\Omega$
Output high level voltage	$V_{OH1}$	$V_{DD} = 2.9 \text{ V}$ , $I_{OH} = -450 \mu\text{A}$ , P00 to P03, P10 to P13	$V_{DD} - 0.45$			V
Output off-leak current	$ I_{OFF1} $	$V_{DD} = 2.9 \text{ V}$ , P00 to P03, P10 to P13	$V_{IN} = V_{SS}$		1.0	$\mu\text{A}$
	$ I_{OFF1} $		$V_{IN} = V_{DD}$		1.0	$\mu\text{A}$
Output high level voltage	$V_{OH2}$	$V_{DD} = 2.9 \text{ V}$ , $I_{OH} = -10 \text{ mA}$ , P20, P21	$V_{DD} - 1.5$			V
Output off-leak current	$ I_{OFF1} $	$V_{DD} = 2.9 \text{ V}$ , P20, P21	$V_{IN} = V_{SS}$		1.0	$\mu\text{A}$
	$ I_{OFF1} $		$V_{IN} \neq V_{DD}$		1.0	$\mu\text{A}$
Output current (H)	$I_{OH1}$	$V_{DD} = 3.0 \text{ V}$ , $V_{OH} = V_{DD} - 1.5 \text{ V}$ , CA		-12	-6	$\text{mA}$
Output current (L)	$I_{OL1}$	$V_{DD} = 3.0 \text{ V}$ , $V_{OH} = 0.9 \text{ V}$ , CA	2	5		$\text{mA}$
HALT-mode supply current	$I_{DD1}$	$V_{DD} = 3.0 \text{ V}$ , 455 kHz CR oscillation, $C_{cd} = C_{cg} = 150 \text{ pF}$ , $T_a \leq 50^\circ\text{C}$ , Figure 5		80	300	$\mu\text{A}$
Operating Current	$I_{DD2}$	$V_{DD} = 3.0 \text{ V}$ , 455 kHz CR oscillation, $C_{cd} = C_{cg} = 150 \text{ pF}$ , $T_a \leq 50^\circ\text{C}$ , Figure 5		150	500	$\mu\text{A}$
Supply leak current 1	$I_{LEAK1}$	$V_{DD} = 3.0 \text{ V}$	$T_a = 25^\circ\text{C}$		0.2	$\mu\text{A}$
Supply leak current 2	$I_{LEAK2}$		$T_a = 50^\circ\text{C}$		1	5 $\mu\text{A}$
Oscillator start-up voltage	$V_{ST}$	$C_{cd} = C_{cg} = 150 \text{ pF}$ , 455 kHz CR oscillation, Figure 4			2.3	V
Oscillator sustaining voltage	$V_{SUS}$			2.0		V
Oscillator start-up time	$t_{ST}$		$V_{DD} = 2.3 \text{ V}$ , $C_{cd} = C_{cg} = 150 \text{ pF}$ , 455 kHz CR oscillation, Figure 4		30	ms

### Recommended Oscillators

Oscillator	Manufacturer	Part number	$C_{cg}$	$C_{cd}$
455 kHz ceramic oscillator	Kyocera	KRB-455BK/Y	150 pF	150 pF
	Murata	CSB455E	150 pF	150 pF
	Fuji Ceramics	POE-455	150 pF	150 pF

## LC573010A, 573015A

### Electrical Characteristics at $T_a = -30$ to $+70^\circ\text{C}$ , $V_{SS} = 0 \text{ V}$

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Input impedance	$R_{IN1A}$	$V_{DD} = 5.0 \text{ V}$ , $V_{IL} = 0.4 \text{ V}$ , S1 to S4, M1 to M4: Low level hold Tr, Figure 3	70	200	300	$\text{k}\Omega$
	$R_{IN1B}$	$V_{DD} = 5.0 \text{ V}$ , S1 to S4, M1 to M4: Low level pull-down Tr, Figure 3	30	50	100	$\text{k}\Omega$
	$R_{IN2}$	$V_{DD} = 5.0 \text{ V}$ , $\overline{\text{RES}}$	10	300	300	$\text{k}\Omega$
Output high level voltage	$V_{OH1}$	$V_{DD} = 5.0 \text{ V}$ , $I_{OH} = -750 \mu\text{A}$ , P00 to P03, P10 to P13	$V_{DD} = 0.75$			V
Output off-leak current	$ I_{OFF1} $	$V_{DD} = 5.0 \text{ V}$ , P00 to P03, P10 to P13	$V_{IN} = V_{SS}$		1.0	$\mu\text{A}$
	$ I_{OFF1} $		$V_{IN} = V_{DD}$		1.0	$\mu\text{A}$
Output high level voltage	$V_{OH2}$	$V_{DD} = 5.0 \text{ V}$ , $I_{OH} = -10 \text{ mA}$ , P20, P21	$V_{DD} = 0.5$			V
Output off-leak current	$ I_{OFF1} $	$V_{DD} = 5.0 \text{ V}$ , P20, P21	$V_{IN} = V_{SS}$		1.0	$\mu\text{A}$
	$ I_{OFF1} $		$V_{IN} = V_{DD}$		1.0	$\mu\text{A}$
Output current (H)	$I_{OH1}$	$V_{DD} = 5.0 \text{ V}$ , $V_{OH} = V_{DD} - 2.5 \text{ V}$ , CA	10	20		$\text{mA}$
Output current (L)	$I_{OL1}$	$V_{DD} = 5.0 \text{ V}$ , $V_{OL} = 0.9 \text{ V}$ , CA	2			$\text{mA}$
HALT-mode supply current	$I_{DD1}$	$V_{DD} = 5.0 \text{ V}$ , 455 kHz CR oscillation, $C_{cd} = C_{cg} = 150 \text{ pF}$ , $T_a \leq 50^\circ\text{C}$ , Figure 5		300	400	$\mu\text{A}$
Operating current	$I_{DD2}$	$V_{DD} = 5.0 \text{ V}$ , 455 kHz CR oscillation $C_{cd} = C_{cg} = 150 \text{ pF}$ , $T_a \leq 50^\circ\text{C}$ , Figure 5		400	500	$\mu\text{A}$
Supply leak current 1	$I_{LEAK1}$	$V_{DD} = 5.0 \text{ V}$	$T_a = 25^\circ\text{C}$		0.2	$\mu\text{A}$
Supply leak current 2	$I_{LEAK2}$		$T_a \leq 50^\circ\text{C}$		1	5 $\mu\text{A}$
Oscillator start-up voltage	$V_{ST}$	$C_{cd} = C_{cg} = 150 \text{ pF}$ , 455 kHz CR oscillation, Figure 4			2.3	V
Oscillator sustaining voltage	$V_{SUS}$			2.0		V
Oscillator start-up time	$t_{ST}$	$V_{DD} = 2.3 \text{ V}$ , $C_{cd} = C_{cg} = 150 \text{ pF}$ , 455 kHz CR oscillation, Figure 4			30	ms

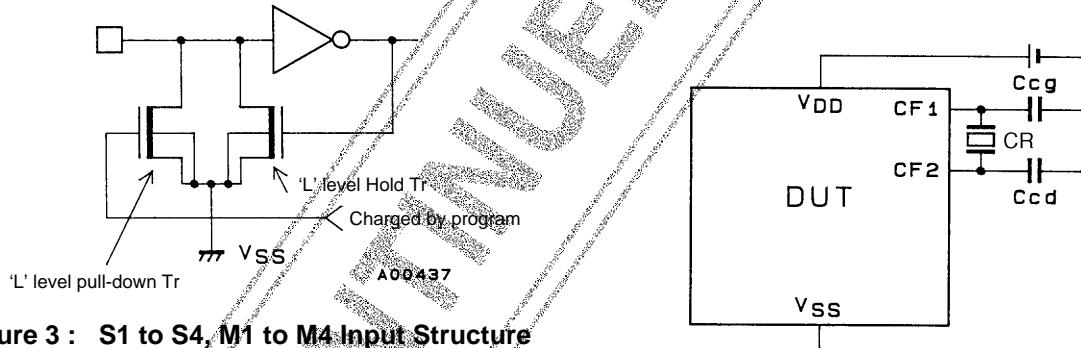


Figure 3 : S1 to S4, M1 to M4 Input Structure

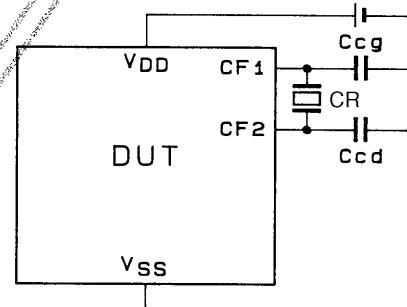


Figure4 : Oscillator Start-Up Voltage, Oscillator Sustaining Voltage, and Oscillator Start-Up Time Measuring Circuit

Note : CR is 455 kHz, S-PORT: M-PORT: Input Pull-down transistor is on.  $\overline{\text{RES}}$  terminal has resistor built-in and is open. I/O-port is set at output mode and data is high.

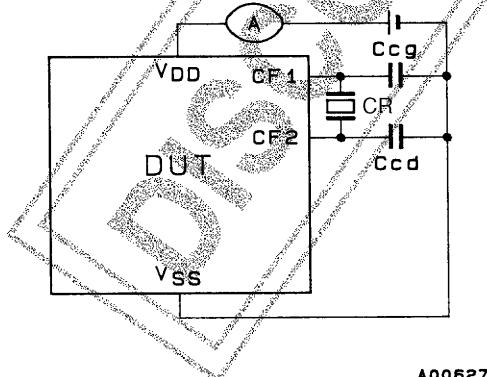
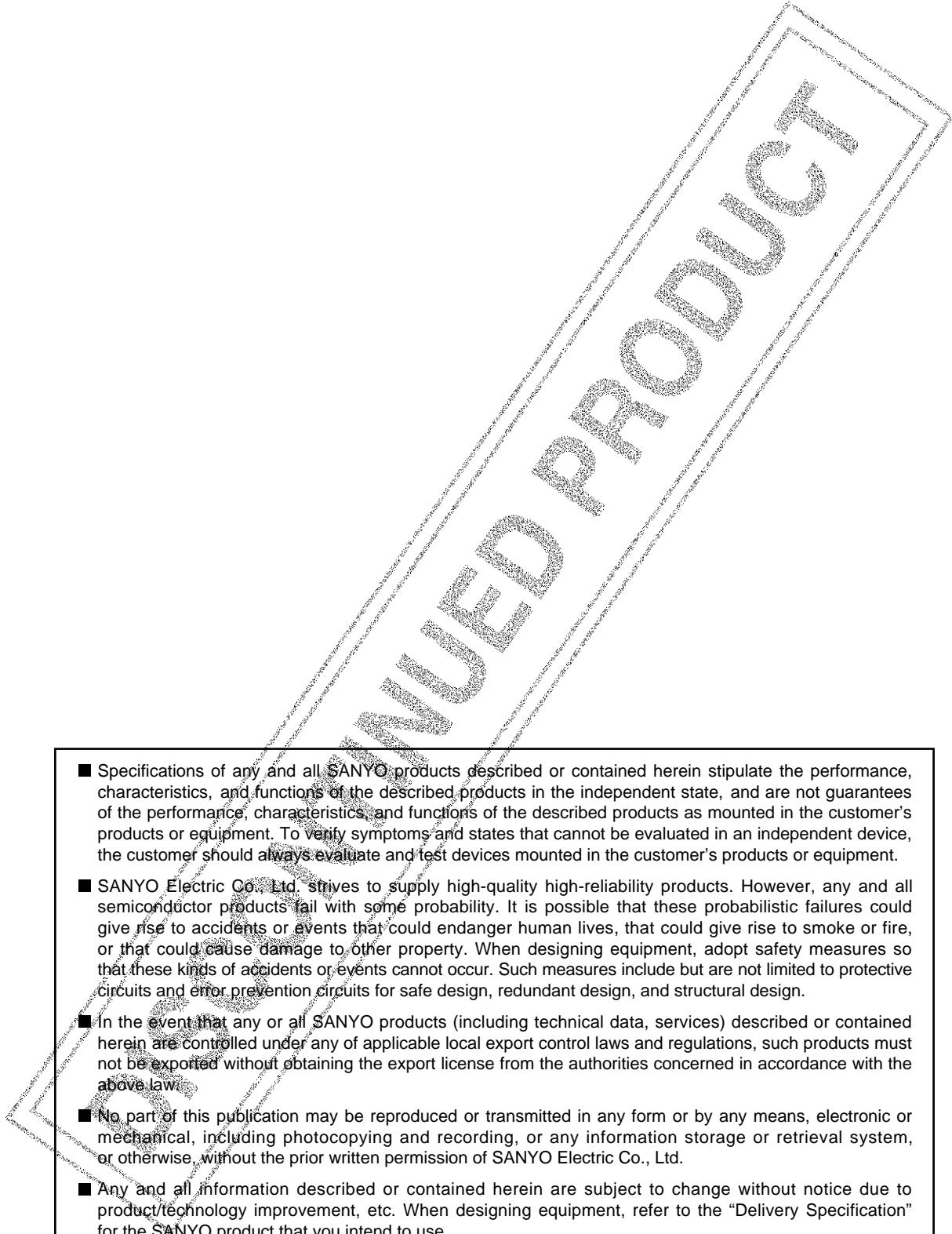


Figure 5 : Supply Current Measuring Circuit

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