Ordering number : ENN*6790

CMOS IC

LC4104C-T2A

LCD Dot Matrix Segment Driver for STN Displays

Preliminary

Overview

The LC4104C-T2A is a segment driver IC for large-scale dot matrix LCD displays. The LC4104C-T2A latches 160-bits of display data transferred from the controller over a 4- or 8-bit parallel interface and generates the LCD drive signals. In conjunction with the LC4102C-T2A common driver, the LC4104C-T2A forms a chip set that can drive large-screen LCD panels.

Features

- High-voltage CMOS (P-sub) process
- LCD drive voltage: 36 V
- Logic system power-supply voltage: 2.7 to 5.5 V
- Maximum fcp: 12 MHz (V_{DD} = 5 V ±10%),
  10 MHz (V_{DD} = 2.7 to 4.5 V)
- Parallel input circuit can be switched between 4 and 8 bits.
- Output directionality switching
- DISPOFF function (Holds the LCD drive voltage at a fixed level.)
- Display duty ratios: 1/160 to 1/480
- Package: TCP (Tape Carrier Package)

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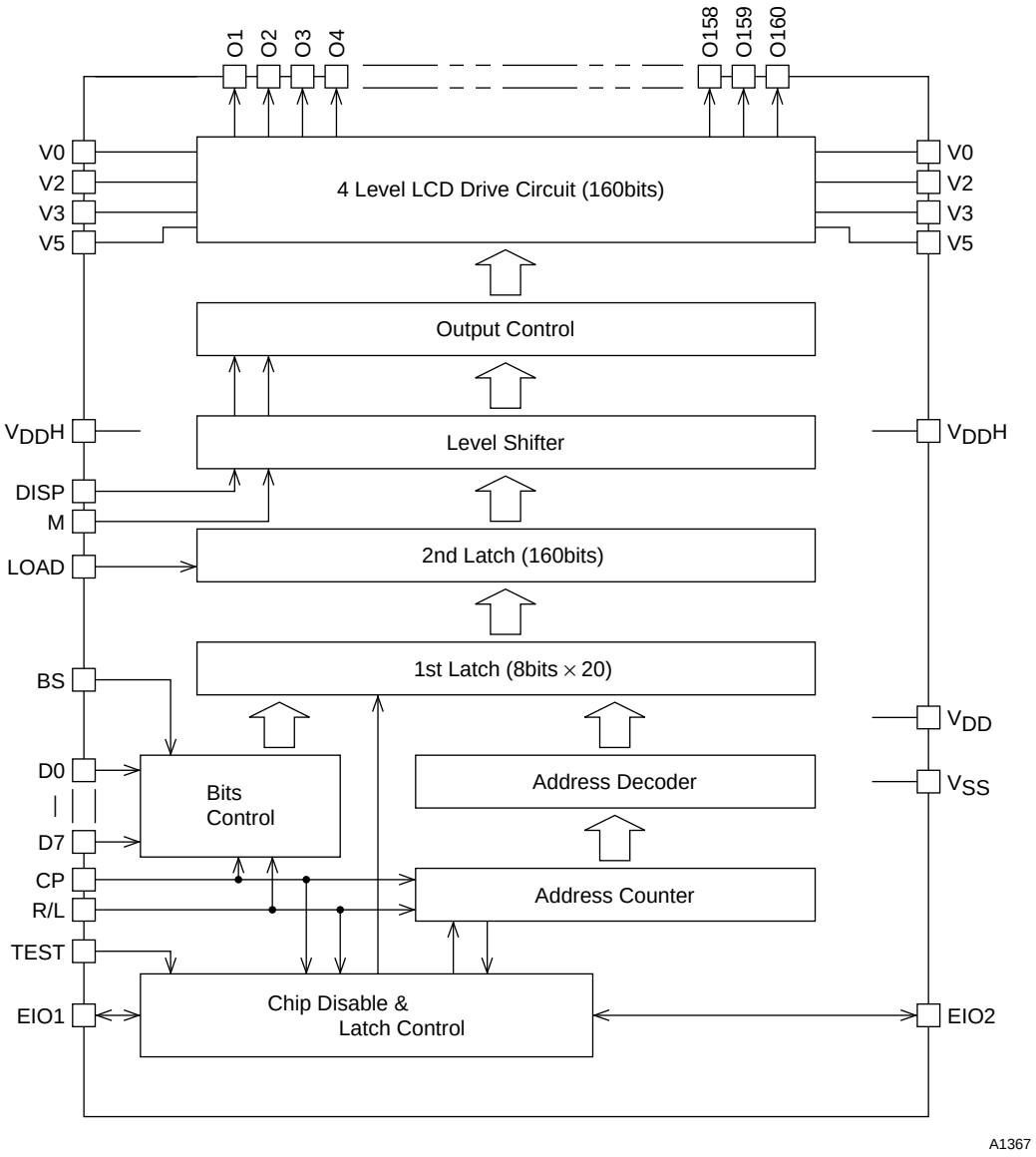
Block Diagram



Specifications

The following electrical characteristics apply when sealed in a SANYO standard PGA-208 package.

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7	V
Maximum supply voltage	V_{DDH} max		–0.3 to +40	V
Maximum supply voltage	V_{SS} max		–0.3 to +0.3	V
Input voltage	V_{IN}	D0 to D7, LOAD, CP, R/L, TEST, DISP, M, EIO1, EIO2, BS	–0.3 to V_{DD} + 0.3	V
Input voltage	V0, V2	V0, V2	V_{DDH} – 7 to V_{DDH} + 0.3	V
Input voltage	V3	V3	–0.3 to V_{SS} + 7	V
Input voltage	V5	V5	–0.3 to +0.3	V
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Note: V0, V2, V3, and V5 must obey the following relationships: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7$ V, and $7 \text{ V} \geq V3 \geq V5 \geq V_{SS}$.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7		5.5	V
Supply voltage	V_{DDH}		14		36	V
Supply voltage	V_{SS}			0		V
Input high-level voltage	V_{IH}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	0.8 V_{DD}		V_{DD}	V
Input low-level voltage	V_{IL}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	0		0.2 V_{DD}	V
Input voltage	V0, V2	V0, V2	V_{DDH} – 7		V_{DDH}	V
Input voltage	V3	V3	0		V_{SSH} + 7	V
Input voltage	V5	V5		0		V

Note: V0, V2, V3, and V5 must obey the following relationships: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7$ V, and $7 \text{ V} \geq V3 \geq V5 \geq V_{SS}$.
At power on: First turn on the logic system power supply and then turn on the high-voltage system power supply; alternatively, turn both on at the same time.
At power off: First turn off the high-voltage system power supply and then turn off the logic system power supply; alternatively, turn both off at the same time.

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	fcp	CP			12	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	20			ns
Low-level clock pulse width	tw (cpL)	CP	20			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	10			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	10			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	24			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

① : $\text{tr, tf} < \dfrac{\dfrac{1}{\text{fcp}} - \text{tw (cph)} - \text{tw (cpl)}}{2}$

② : $\text{tr, tf} \leq 50$ ns

Allowable Operating Ranges at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	fcp	CP			10	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	37			ns
Low-level clock pulse width	tw (cpL)	CP	37			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	35			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	35			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	30			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

① : $\text{tr, tf} < \dfrac{\dfrac{1}{\text{fcp}} - \text{tw (cph)} - \text{tw (cpl)}}{2}$

② : $\text{tr, tf} \leq 50$ ns

Electrical Characteristics at Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$: D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, EIO2, BS, TEST			5	µA
Input low-level current	$I_{IL}1$	$V_{IN} = V_{SS}$: D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, EIO2, BS	–5			µA
	$I_{IL}2$	$V_{IN} = V_{SS}$: TEST	–500			
Output high-level voltage	V_{OH}	I_O = –0.4 mA: EIO1, EIO2	V_{DD} – 0.4		V_{DD}	V
Output low-level voltage	V_{OL}	I_O = 0.4 mA: EIO1, EIO2	V_{SS}		0.4	V
Output on resistance	R_{OUT}	V_{DDH} = 36 V*1, V0 – V_O = 0.5 V, V2 – V_O = 0.5 V, V_O – V3 = 0.5 V, V_O – V5 = 0.5 V: O1 to O160		1	3	kΩ
Current drain	I_{DD}	V_{DD} = 2.7 to 5.5 V			5.0	mA
	I_{DDH}	V_{DD} = 2.7 to 5.5 V, V_{DDH} = 32 V*2,			2.0	mA
		V_{DD} = 5 V ± 10%, V_{DDH} = 36 V			2.0	mA
	I_{ST}	*3			500	µA

Note: 1. V_O is the voltage applied for an on output, V0 = V_{DDH}, V2 = 18/20 (V_{DDH} – V_{SS}), V3 = 2/20 (V_{DDH} – V_{SS}), V5 = V_{SS}
2. LOAD = 28 kHz, CP = 10 MHz, M = 75 Hz
Alternatively: No output load and with the inputs $V_{IH} = V_{DD}$ and $V_{IL} = V_{SS}$.
3. The current drain in standby mode. Note that the EIOn pins must be held at V_{DD}.

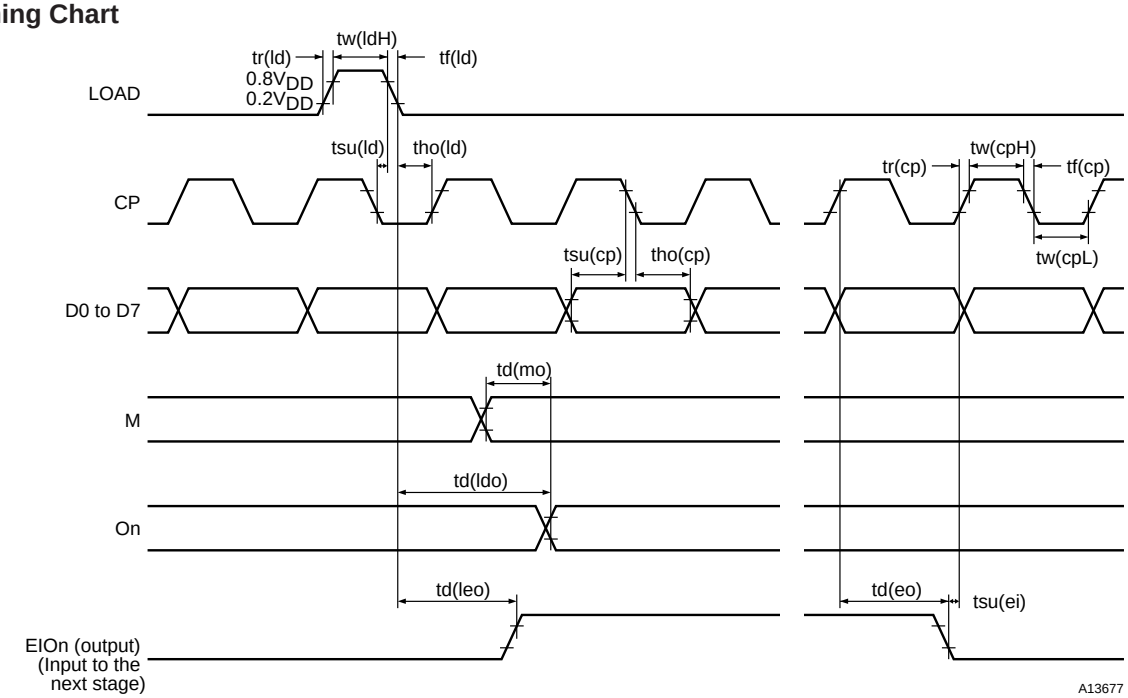
Switching Characteristics at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 5 V ± 10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	td (eo)	30 pF capacitive load: CP, EIO1, EIO2			40	ns
LD/EIO output delay time	td (leo)	30 pF capacitive load: LOAD, EIO1, EIO2			70	ns
LOAD/on delay time	td (ldo)	100 pF capacitive load: LOAD, O1 to O160			3	µs
M/on delay time	td (mo)	100 pF capacitive load: M, O1 to O160			3	µs

Switching Characteristics at Ta = –20 to +75°C, V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	td (eo)	30 pF capacitive load: CP, EIO1, EIO2			80	ns
LD/EIO output delay time	td (leo)	30 pF capacitive load: LOAD, EIO1, EIO2			130	ns
LOAD/on delay time	td (ldo)	100 pF capacitive load: LOAD, O1 to O160			3	µs
M/on delay time	td (mo)	100 pF capacitive load: M, O1 to O160			3	µs

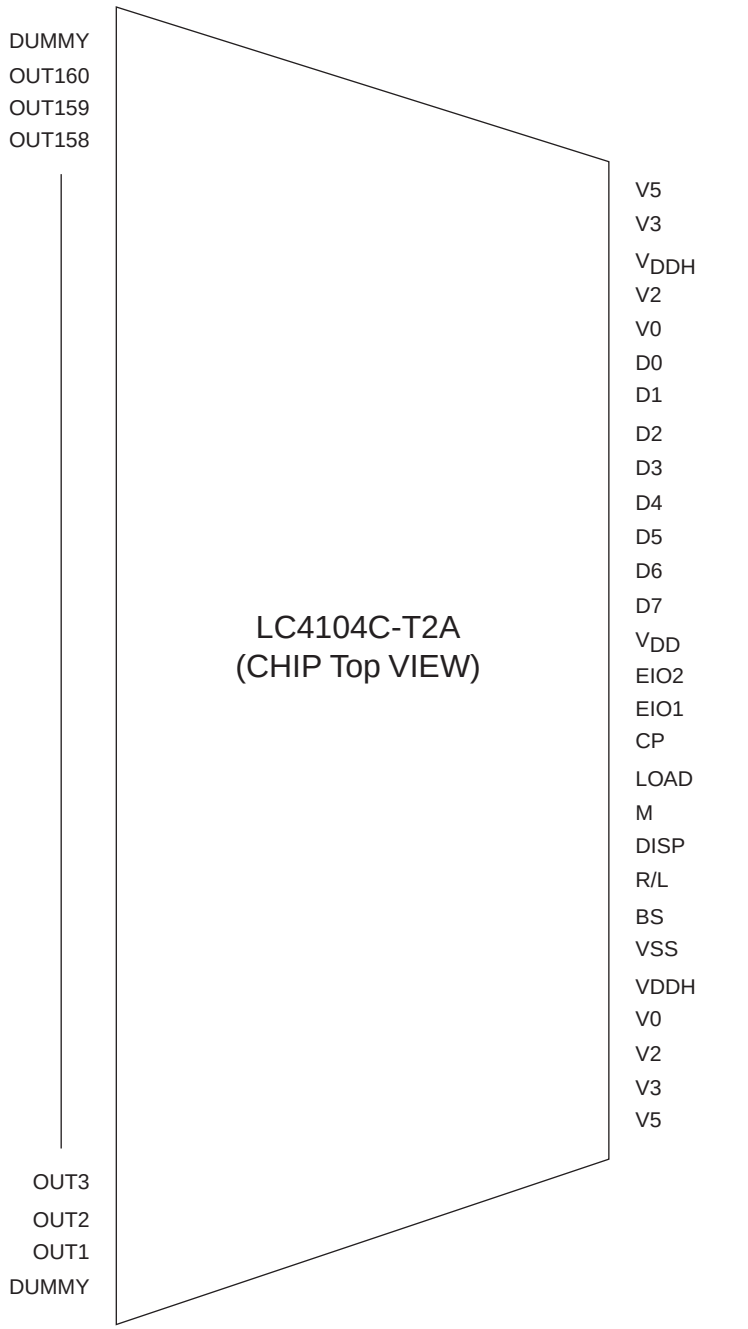
Timing Chart



Pin Functions

<table>
<tr><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>O1 to O160</td><td>O</td><td>LCD drive outputs
<table>
<tr><th>M</th><th>Data</th><th>DISP</th><th>On</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V5</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V5</td></tr>
</table>
*: Don’t care.</td></tr>
<tr><td>V0</td><td>I</td><td>V0 level drive voltage supply (selected level)</td></tr>
<tr><td>V2</td><td>I</td><td>V2 level drive voltage supply (unselected level)</td></tr>
<tr><td>V3</td><td>I</td><td>V3 level drive voltage supply (unselected level)</td></tr>
<tr><td>V5</td><td>I</td><td>V5 level drive voltage supply (selected level)</td></tr>
<tr><td>V_{DDH}</td><td>—</td><td>High-voltage system power supply.</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Logic system power supply.</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>GND</td></tr>
<tr><td>DISP</td><td>I</td><td>LCD off function. All outputs go to the V5 level when this pin is low.</td></tr>
<tr><td>M</td><td>I</td><td>Alternation signal input</td></tr>
<tr><td>EIO1
EIO2</td><td>I/O
I/O</td><td>Enable I/O
<table>
<tr><th>R/L</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>In</td><td>Out</td></tr>
<tr><td>H</td><td>Out</td><td>In</td></tr>
</table>
Enable input: The enable input at the first stage is fixed at V_{SS}. For succeeding stages, the enable input is connected to the enable output from the preceding stage.
Enable output: Connected to the enable input of the next stage when cascode connection is used.</td></tr>
<tr><td>CP</td><td>I</td><td>Data acquisition clock (falling edge)</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data load clock (falling edge)</td></tr>
<tr><td>TEST</td><td>I</td><td>Test input. Must be tied high in normal use.*</td></tr>
<tr><td>R/L</td><td>I</td><td>Data shift direction setting
<table>
<tr><th>R/L</th><th>BS</th><th colspan="10">O1 to O160 outputs</th></tr>
<tr><td>L</td><td rowspan="2">H</td><td>O1
↑
D7</td><td>O2
↑
D6</td><td>O3
↑
D5</td><td>O4
↑
D4</td><td>→ . . .</td><td>O157
↑
D3</td><td>O158
↑
D2</td><td>O159
↑
D1</td><td>O160
↑
D0</td></tr>
<tr><td>H</td><td>O1
↑
D0</td><td>O2
↑
D1</td><td>O3
↑
D2</td><td>O4
↑
D3</td><td>. . .←</td><td>O157
↑
D4</td><td>O158
↑
D5</td><td>O159
↑
D6</td><td>O160
↑
D7</td></tr>
<tr><td>L</td><td rowspan="2">L</td><td>O1
↑
D3</td><td>O2
↑
D2</td><td>O3
↑
D1</td><td>O4
↑
D0</td><td>→ . . .</td><td>O157
↑
D3</td><td>O158
↑
D2</td><td>O159
↑
D1</td><td>O160
↑
D0</td></tr>
<tr><td>H</td><td>O1
↑
D0</td><td>O2
↑
D1</td><td>O3
↑
D2</td><td>O4
↑
D3</td><td>. . .←</td><td>O157
↑
D0</td><td>O158
↑
D1</td><td>O159
↑
D2</td><td>O160
↑
D3</td></tr>
</table></td></tr>
<tr><td>D0 to D7</td><td>I</td><td>Parallel data inputs</td></tr>
<tr><td>BS</td><td>I</td><td>Input bus setting. Set high for 8-bit input, low for 4-bit input. For 4-bit input, D0 to D3 are used for data input and D4 to D7 must be tied to ground.</td></tr>
</table>

Pin Assignment



Note: This figure shows the chip pattern surface as seen from abobe.
This figure dose not stipulate the TCP package.

Package Dimensions

unit: mm

LC4104C-T2A