

**LC4104C-T2A****LCD Dot Matrix Segment Driver for STN Displays****Preliminary****Overview**

The LC4104C-T2A is a segment driver IC for large-scale dot matrix LCD displays. The LC4104C-T2A latches 160-bits of display data transferred from the controller over a 4- or 8-bit parallel interface and generates the LCD drive signals. In conjunction with the LC4102C-T2A common driver, the LC4104C-T2A forms a chip set that can drive large-screen LCD panels.

Features

- High-voltage CMOS (P-sub) process
- LCD drive voltage: 36 V
- Logic system power-supply voltage: 2.7 to 5.5 V
- Maximum fcp: 12 MHz ($V_{DD} = 5\text{ V} \pm 10\%$),
10 MHz ($V_{DD} = 2.7\text{ to }4.5\text{ V}$)
- Parallel input circuit can be switched between 4 and 8 bits.
- Output directionality switching
- DISPOFF function (Holds the LCD drive voltage at a fixed level.)
- Display duty ratios: 1/160 to 1/480
- Package: TCP (Tape Carrier Package)

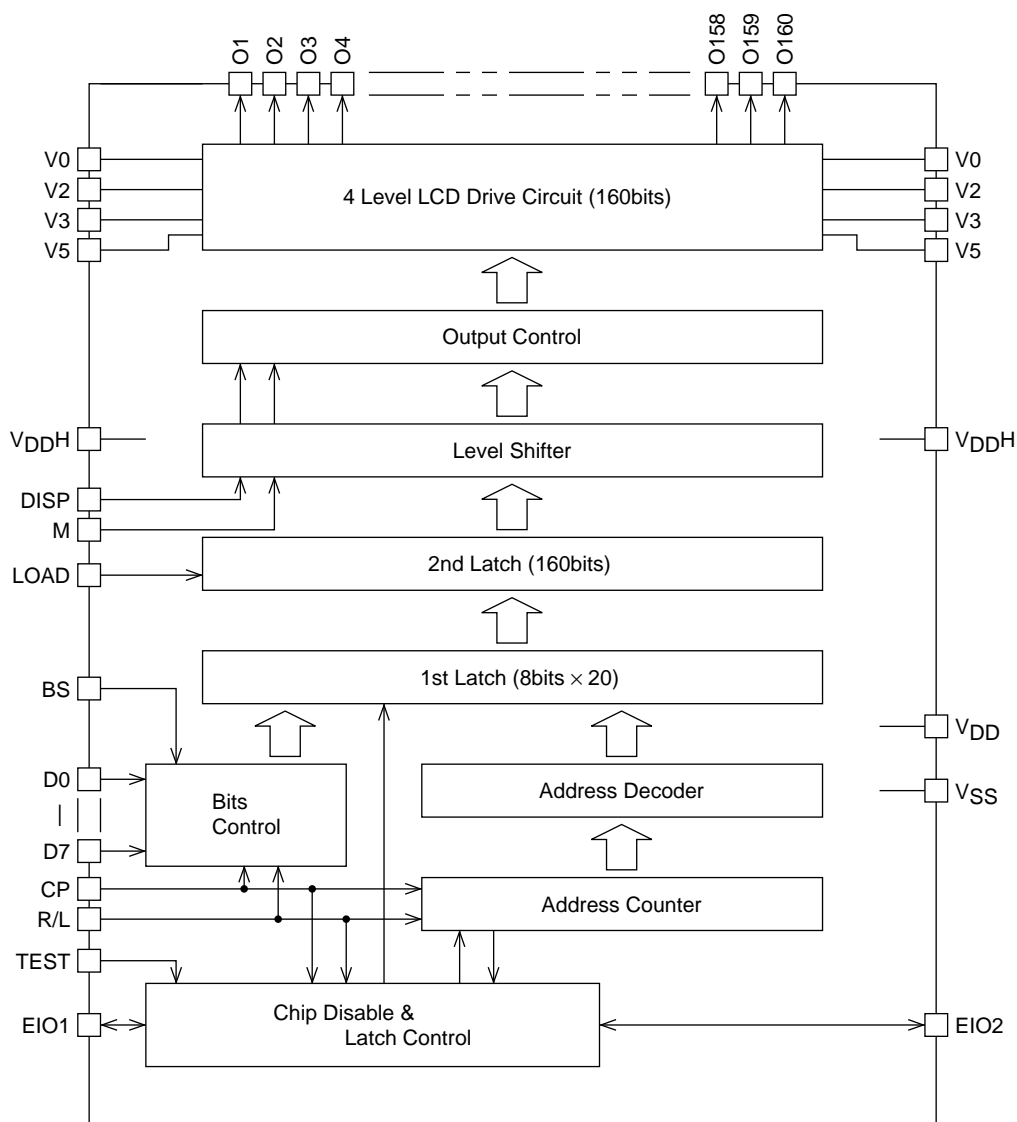
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Block Diagram



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Specifications

The following electrical characteristics apply when sealed in a SANYO standard PGA-208 package.

Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +7	V
Maximum supply voltage	$V_{DDH\text{ max}}$		-0.3 to +40	V
Maximum supply voltage	$V_{SS\text{ max}}$		-0.3 to +0.3	V
Input voltage	V_{IN}	D0 to D7, LOAD, CP, R/L, TEST, DISP, M, EIO1, EIO2, BS	-0.3 to $V_{DD} + 0.3$	V
Input voltage	V0, V2	V0, V2	$V_{DDH} - 7$ to $V_{DDH} + 0.3$	V
Input voltage	V3	V3	-0.3 to $V_{SS} + 7$	V
Input voltage	V5	V5	-0.3 to +0.3	V
Operating temperature	T_{opr}		-20 to +75	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note: V0, V2, V3, and V5 must obey the following relationships: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7\text{ V}$, and $7\text{ V} \geq V3 \geq V5 \geq V_{SS}$.

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Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7		5.5	V
Supply voltage	V_{DDH}		14		36	V
Supply voltage	V_{SS}			0		V
Input high-level voltage	V_{IH}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	$0.8 V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL}	D0 to D7, LOAD, CP, R/L, M, TEST, DISP, BS, EIO1, EIO2	0		$0.2 V_{DD}$	V
Input voltage	V0, V2	V0, V2	$V_{DDH} - 7$		V_{DDH}	V
Input voltage	V3	V3	0		$V_{SSH} + 7$	V
Input voltage	V5	V5		0		V

Note: V0, V2, V3, and V5 must obey the following relationships: $V_{DDH} \geq V0 \geq V2 \geq V_{DDH} - 7$ V, and 7 V $\geq V3 \geq V5 \geq V_{SS}$.

At power on: First turn on the logic system power supply and then turn on the high-voltage system power supply; alternatively, turn both on at the same time.

At power off: First turn off the high-voltage system power supply and then turn off the logic system power supply; alternatively, turn both off at the same time.

Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 5$ V $\pm 10\%$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	fcp	CP			12	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	20			ns
Low-level clock pulse width	tw (cpL)	CP	20			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	10			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	10			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	24			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

$$\textcircled{1}: tr, tf < \frac{\frac{1}{fcp} - tw(cph) - tw(cpl)}{2}$$

$$\textcircled{2}: tr, tf \leq 50 \text{ ns}$$

Allowable Operating Ranges at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 2.7$ to 4.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
CP clock frequency	fcp	CP			10	MHz
High-level load pulse width	tw (ldH)	LOAD	50			ns
High-level clock pulse width	tw (cpH)	CP	37			ns
Low-level clock pulse width	tw (cpL)	CP	37			ns
LOAD/CP setup time	tsu (ld)	LOAD, CP	100			ns
LOAD/CP hold time	tho (ld)	LOAD, CP	200			ns
DATA/CP setup time	tsu (cp)	CP, D0 to D7	35			ns
DATA/CP hold time	tho (cp)	CP, D0 to D7	35			ns
EIO input setup time	tsu (ei)	CP, EIO1, EIO2	30			ns
Clock rise time	tr	LOAD, CP*			50	ns
Clock fall time	tf	LOAD, CP*			50	ns

Note: * The clock rise time (tr) and fall time (tf) must obey inequalities ① and ② below.

$$\textcircled{1}: tr, tf < \frac{\frac{1}{fcp} - tw(cph) - tw(cpl)}{2}$$

$$\textcircled{2}: tr, tf \leq 50 \text{ ns}$$

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Electrical Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 2.7$ to 5.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$: D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, EIO2, BS, TEST			5	μA
Input low-level current	I_{IL1}	$V_{IN} = V_{SS}$: D0 to D7, LOAD, CP, R/L, M, DISP, EIO1, EIO2, BS	-5			μA
	I_{IL2}	$V_{IN} = V_{SS}$: TEST	-500			
Output high-level voltage	V_{OH}	$I_O = -0.4$ mA: EIO1, EIO2	$V_{DD} - 0.4$		V_{DD}	V
Output low-level voltage	V_{OL}	$I_O = 0.4$ mA: EIO1, EIO2	V_{SS}		0.4	V
Output on resistance	R_{OUT}	$V_{DDH} = 36$ V ¹ , $V_0 - V_O = 0.5$ V, $V_2 - V_O = 0.5$ V, $V_O - V_3 = 0.5$ V, $V_O - V_5 = 0.5$ V: O1 to O160		1	3	k Ω
Current drain	I_{DD}	$V_{DD} = 2.7$ to 5.5 V			5.0	mA
	I_{DDH}	$V_{DD} = 2.7$ to 5.5 V, $V_{DDH} = 32$ V ² ,			2.0	mA
		$V_{DD} = 5$ V $\pm 10\%$, $V_{DDH} = 36$ V			2.0	mA
	I_{ST}	*3			500	μA

Note: 1. V_O is the voltage applied for an on output, $V_0 = V_{DDH}$, $V_2 = 18/20 (V_{DDH} - V_{SS})$, $V_3 = 2/20 (V_{DDH} - V_{SS})$, $V_5 = V_{SS}$
 2. LOAD = 28 kHz, CP = 10 MHz, M = 75 Hz
 Alternatively: No output load and with the inputs $V_{IH} = V_{DD}$ and $V_{IL} = V_{SS}$.
 3. The current drain in standby mode. Note that the EIO pins must be held at V_{DD} .

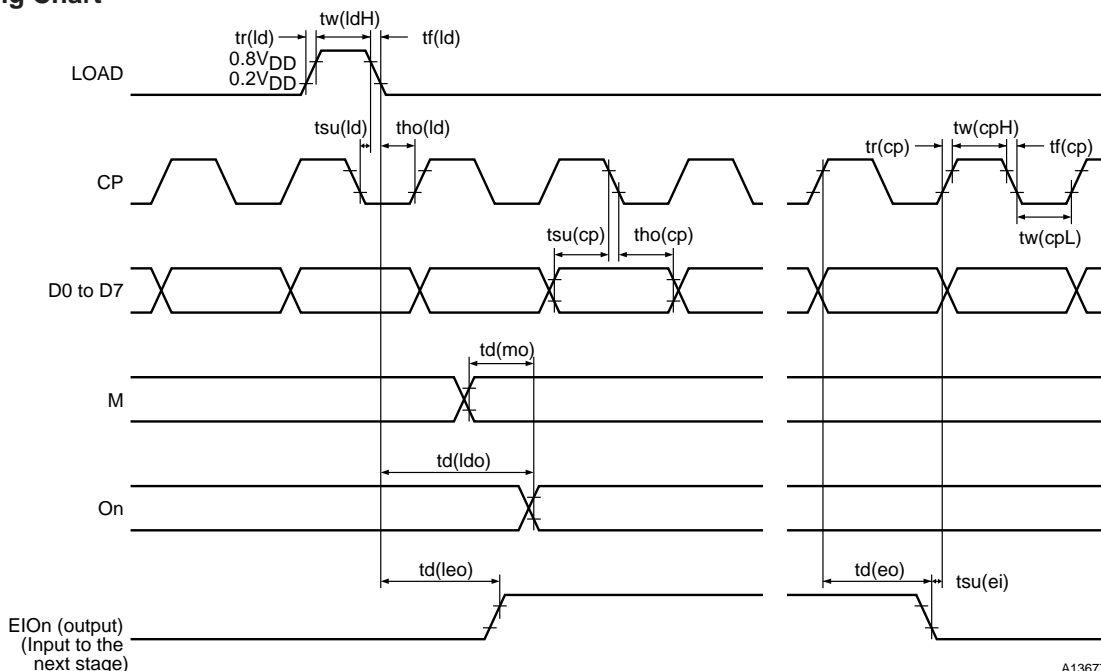
Switching Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 5$ V $\pm 10\%$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	$t_d(\text{eo})$	30 pF capacitive load: CP, EIO1, EIO2			40	ns
LD/EIO output delay time	$t_d(\text{leo})$	30 pF capacitive load: LOAD, EIO1, EIO2			70	ns
LOAD/on delay time	$t_d(\text{ldo})$	100 pF capacitive load: LOAD, O1 to O160			3	μs
M/on delay time	$t_d(\text{mo})$	100 pF capacitive load: M, O1 to O160			3	μs

Switching Characteristics at $T_a = -20$ to $+75^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 2.7$ to 4.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
EIO output delay time	$t_d(\text{eo})$	30 pF capacitive load: CP, EIO1, EIO2			80	ns
LD/EIO output delay time	$t_d(\text{leo})$	30 pF capacitive load: LOAD, EIO1, EIO2			130	ns
LOAD/on delay time	$t_d(\text{ldo})$	100 pF capacitive load: LOAD, O1 to O160			3	μs
M/on delay time	$t_d(\text{mo})$	100 pF capacitive load: M, O1 to O160			3	μs

Timing Chart



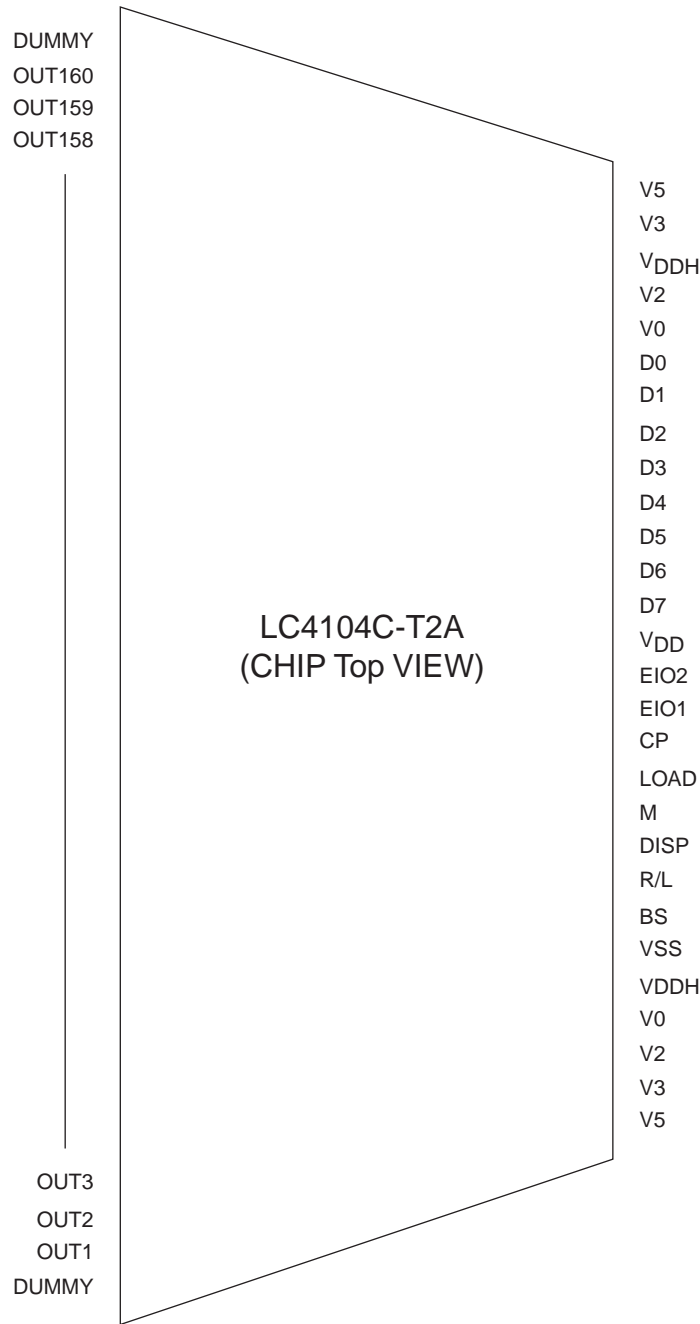
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Pin Functions

Symbol	I/O	Function																																																				
O1 to O160	O	LCD drive outputs																																																				
		<table><tr><td>M</td><td>Data</td><td>DISP</td><td>On</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V0</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>L</td><td>H</td><td>V3</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V5</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V5</td></tr></table>	M	Data	DISP	On	H	H	H	V0	H	L	H	V2	L	L	H	V3	L	H	H	V5	*	*	L	V5																												
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		L	L	H	V3																																																	
		L	H	H	V5																																																	
*	*	L	V5																																																			
*: Don't care.																																																						
V0	I	V0 level drive voltage supply (selected level)																																																				
V2	I	V2 level drive voltage supply (unselected level)																																																				
V3	I	V3 level drive voltage supply (unselected level)																																																				
V5	I	V5 level drive voltage supply (selected level)																																																				
V _{DDH}	—	High-voltage system power supply.																																																				
V _{DD}	—	Logic system power supply.																																																				
V _{SS}	—	GND																																																				
DISP	I	LCD off function. All outputs go to the V5 level when this pin is low.																																																				
M	I	Alternation signal input																																																				
EIO1 EIO2	I/O I/O	Enable I/O																																																				
<table><tr><td>R/L</td><td>EIO1</td><td>EIO2</td></tr><tr><td>L</td><td>In</td><td>Out</td></tr><tr><td>H</td><td>Out</td><td>In</td></tr></table>			R/L	EIO1	EIO2	L	In	Out	H	Out	In																																											
R/L	EIO1	EIO2																																																				
L	In	Out																																																				
H	Out	In																																																				
Enable input: The enable input at the first stage is fixed at V _{SS} . For succeeding stages, the enable input is connected to the enable output from the preceding stage.																																																						
Enable output: Connected to the enable input of the next stage when cascode connection is used.																																																						
CP	I	Data acquisition clock (falling edge)																																																				
LOAD	I	Data load clock (falling edge)																																																				
TEST	I	Test input. Must be tied high in normal use.*																																																				
R/L	I	Data shift direction setting																																																				
<table><tr><td>R/L</td><td>BS</td><td colspan="10">O1 to O160 outputs</td></tr><tr><td rowspan="2">L</td><td rowspan="2">H</td><td>O1 ↑ D7</td><td>O2 ↑ D6</td><td>O3 ↑ D5</td><td>O4 ↑ D4</td><td>→ ...</td><td>O157 ↑ D3</td><td>O158 ↑ D2</td><td>O159 ↑ D1</td><td>O160 ↑ D0</td></tr><tr><td>O1 ↑ D0</td><td>O2 ↑ D1</td><td>O3 ↑ D2</td><td>O4 ↑ D3</td><td>...←</td><td>O157 ↑ D4</td><td>O158 ↑ D5</td><td>O159 ↑ D6</td><td>O160 ↑ D7</td></tr><tr><td rowspan="2">L</td><td rowspan="2">L</td><td>O1 ↑ D3</td><td>O2 ↑ D2</td><td>O3 ↑ D1</td><td>O4 ↑ D0</td><td>→ ...</td><td>O157 ↑ D3</td><td>O158 ↑ D2</td><td>O159 ↑ D1</td><td>O160 ↑ D0</td></tr><tr><td>O1 ↑ D0</td><td>O2 ↑ D1</td><td>O3 ↑ D2</td><td>O4 ↑ D3</td><td>...←</td><td>O157 ↑ D0</td><td>O158 ↑ D1</td><td>O159 ↑ D2</td><td>O160 ↑ D3</td></tr></table>			R/L	BS	O1 to O160 outputs										L	H	O1 ↑ D7	O2 ↑ D6	O3 ↑ D5	O4 ↑ D4	→ ...	O157 ↑ D3	O158 ↑ D2	O159 ↑ D1	O160 ↑ D0	O1 ↑ D0	O2 ↑ D1	O3 ↑ D2	O4 ↑ D3	...←	O157 ↑ D4	O158 ↑ D5	O159 ↑ D6	O160 ↑ D7	L	L	O1 ↑ D3	O2 ↑ D2	O3 ↑ D1	O4 ↑ D0	→ ...	O157 ↑ D3	O158 ↑ D2	O159 ↑ D1	O160 ↑ D0	O1 ↑ D0	O2 ↑ D1	O3 ↑ D2	O4 ↑ D3	...←	O157 ↑ D0	O158 ↑ D1	O159 ↑ D2	O160 ↑ D3
R/L	BS	O1 to O160 outputs																																																				
L	H	O1 ↑ D7	O2 ↑ D6	O3 ↑ D5	O4 ↑ D4	→ ...	O157 ↑ D3	O158 ↑ D2	O159 ↑ D1	O160 ↑ D0																																												
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L	L	O1 ↑ D3	O2 ↑ D2	O3 ↑ D1	O4 ↑ D0	→ ...	O157 ↑ D3	O158 ↑ D2	O159 ↑ D1	O160 ↑ D0																																												
		O1 ↑ D0	O2 ↑ D1	O3 ↑ D2	O4 ↑ D3	...←	O157 ↑ D0	O158 ↑ D1	O159 ↑ D2	O160 ↑ D3																																												
D0 to D7	I	Parallel data inputs																																																				
BS	I	Input bus setting. Set high for 8-bit input, low for 4-bit input. For 4-bit input, D0 to D3 are used for data input and D4 to D7 must be tied to ground.																																																				

Pin Assignment



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Note: This figure shows the chip pattern surface as seen from above.
This figure dose not stipulate the TCP package.

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