Ordering number : ENN*6789

CMOS IC

LC4102C-T2A

LCD Dot Matrix Common Driver for STN Displays

Preliminary

Overview

The LC4102C-T2A is a common driver for large-scale dot matrix LCD panels. It includes a 160-bit bidirectional shift register and 4-level LCD driver circuits. The number of bits can be further increased by using the provided input and output pins to connect multiple LC4102C-T2A in cascade. The LC4102C-T2A and the LC4104C-T2A LCD dot matrix segment driver IC form a large-screen LCD panel driver chip set.

Features

- Fabricated in a CMOS (P-sub) high-voltage process.
- LCD drive voltage: 36 V
- Logic system power-supply voltage: 2.7 to 5.5 V
- fcp max: 2.5 MHz
- Bidirectional shift register
- The shift register can be split into two 80-bit registers. (Two screens drivable)
- DISPOFF function that locks the drive voltages output to the LCD at fixed levels.
- Display duty: 1/160 to 1/480
- Package: TCP (Tape Carrier Package)

Specifications

The electrical characteristics values shown below are for devices packaged in the SANYO standard PGA-208 package.

Absolute Maximum Ratings at V_{SS} = 0

Parameter	Symbol	Applicable pins	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{EE} max	V_{EE}	–0.3 to +40.0	V
	V_{SSH} max	V_{SSH}	–0.3 to +0.3	V
Input voltage	V_{IN}	*1	–0.3 to V_{DD} + 0.3	V
	V0, V1	V0, V1 *2	V_{EE} – 7.0 to V_{EE} + 0.3	V
	V4	V4 *2	–0.3 to V_{SS} + 7.0	V
	V5	V5 *2	–0.3 to +0.3	V
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Note: 1. LOAD, RS/LS, DISP, DF, DIO1, DIO160, DMIN and MODE
2. The voltages V0, V1, V4, and V5 must obey the relationships $V_{EE} \geq V0 \geq V1 \geq V_{EE} - 7$ V, and $7 V \geq V4 \geq V5 \geq V_{SSH}$.

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Allowable Operating Ranges at V_{SS} = 0, Ta = –20 to +75°C

Parameter	Symbol	Applicable pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		5.5	V
	V_{EE}	V_{EE}	14		36	V
	V_{SSH}	V_{SSH}		0		V
Input high-level voltage	V_{IH}	*1	$0.8 \times V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL}	*1	0		$0.2 \times V_{DD}$	V
Input voltage	V0, V1	V0, V1 *2	$V_{EE} - 7.0$		V_{EE}	V
	V4	V4 *2	0		$V_{SSH} + 7.0$	V
	V5	V5 *2		0		V

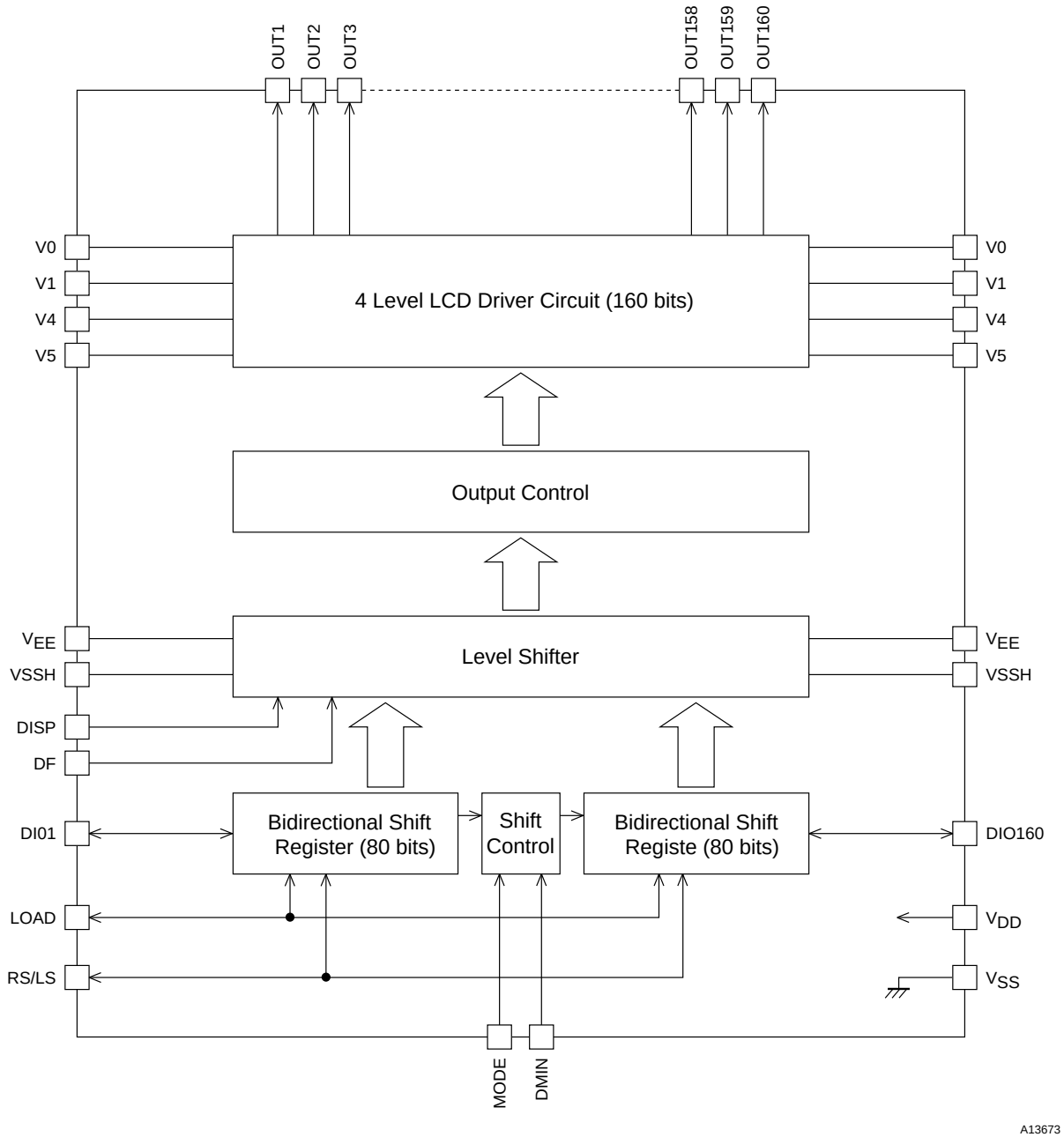
Note: 1. LOAD, RS/LS, DISP, DF, DIO1, DIO160, DMIN and MODE
2. The voltages V0, V1, V4, and V5 must obey the relationships $V_{EE} \geq V0 \geq V1 \geq V_{EE} - 7$ V, and $7 \text{ V} \geq V4 \geq V5 \geq V_{SSH}$.
When turning on the power supplies, first turn on the logic system power supply and then turn on the high-voltage system power supply; alternatively, turn both on at the same time.
When turning off the power supplies, first turn off the high-voltage system power supply and then turn off the logic system power supply; alternatively, turn both off at the same time.

Electrical Characteristics at Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Applicable pins	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH}	$V_{IN} = V_{DD}$*1			1	µA
Input low-level current	I_{IL}	$V_{IN} = V_{SS}$*1	–1			
Output high-level voltage	V_{OH}	I_{OH} = –0.4 mA, DIO1, DIO160	$0.8 \times V_{DD}$		V_{DD}	V
Output low-level voltage	V_{OL}	I_{OL} = 0.4 mA, DIO1, DIO160	V_{SS}		$0.2 \times V_{DD}$	
Output on resistance	RON0	V_{OUT} = V0 – 0.5 V *2, OUT1 to 160			1000	Ω
	RON1	V_{OUT} = V1 – 0.5 V *2, OUT1 to 160			1000	
	RON4	V_{OUT} = V4 + 0.5 V *2, OUT1 to 160			1000	
	RON5	V_{OUT} = V5 + 0.5 V *2, OUT1 to 160			1000	
Current drain 1	I_{DD}	V_{DD}*3			200	µA
Current drain 2	I_{DDH}	V_{DD}*4			500	

Note: 1. LOAD, RS/LS, DISP, DF, DIO1, DIO160, DMIN and MODE
2. V_{OUT} is the voltage applied by on-state outputs. V0 = V_{EE}, V1 = 19/20 ($V_{EE} - V_{SSH}$), V4 = 1/20 ($V_{EE} - V_{SSH}$), V5 = V_{SSH}, $V_{SSH} = V_{SS}$
3. V_{DD} = 2.7 to 5.5 V, f_{CP} = 50 kHz
4. f_{DF} = 100 Hz, with no output load, V_{EE} = 36 V, for a single data shift

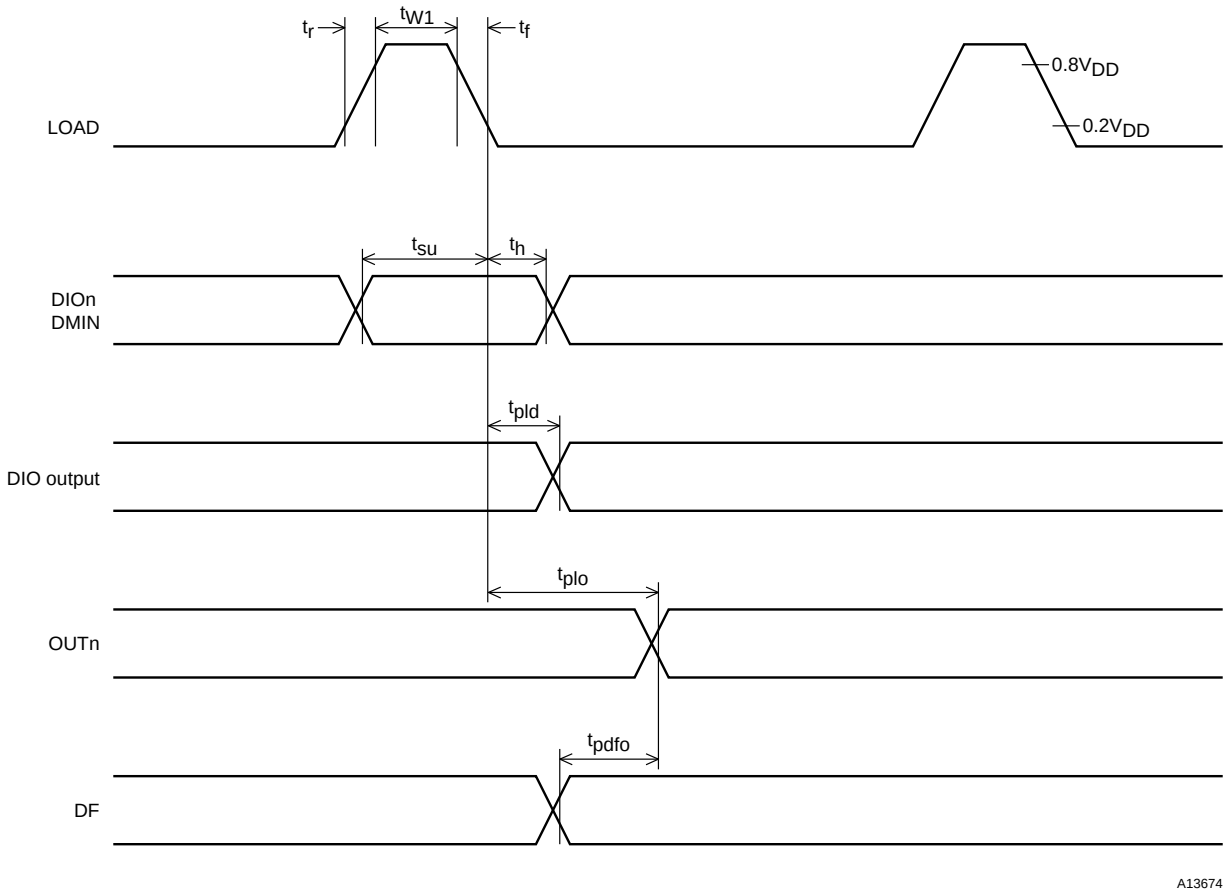
Block Diagram



Switching Characteristics at Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock frequency	fload	LOAD			2.5	MHz
High-level clock pulse width	twl	LOAD	100			ns
Input setup time	tsu	LOAD, DIOn, DMIN	100			
Input hold time	th	LOAD, DIOn, DMIN	30			
LOAD rising time	tr	LOAD			30	
LOAD falling time	tf	LOAD			30	
DIO output delay time	tpld	LOAD, DIOn: 30 pF capacitance load			200	
LOAD-on delay time	tplo	LOAD, OUTn: 100 pF capacitance load			1.0	µs
DF-on delay time	tpdfo	DF, OUTn: 100 pF capacitance load			1.0	

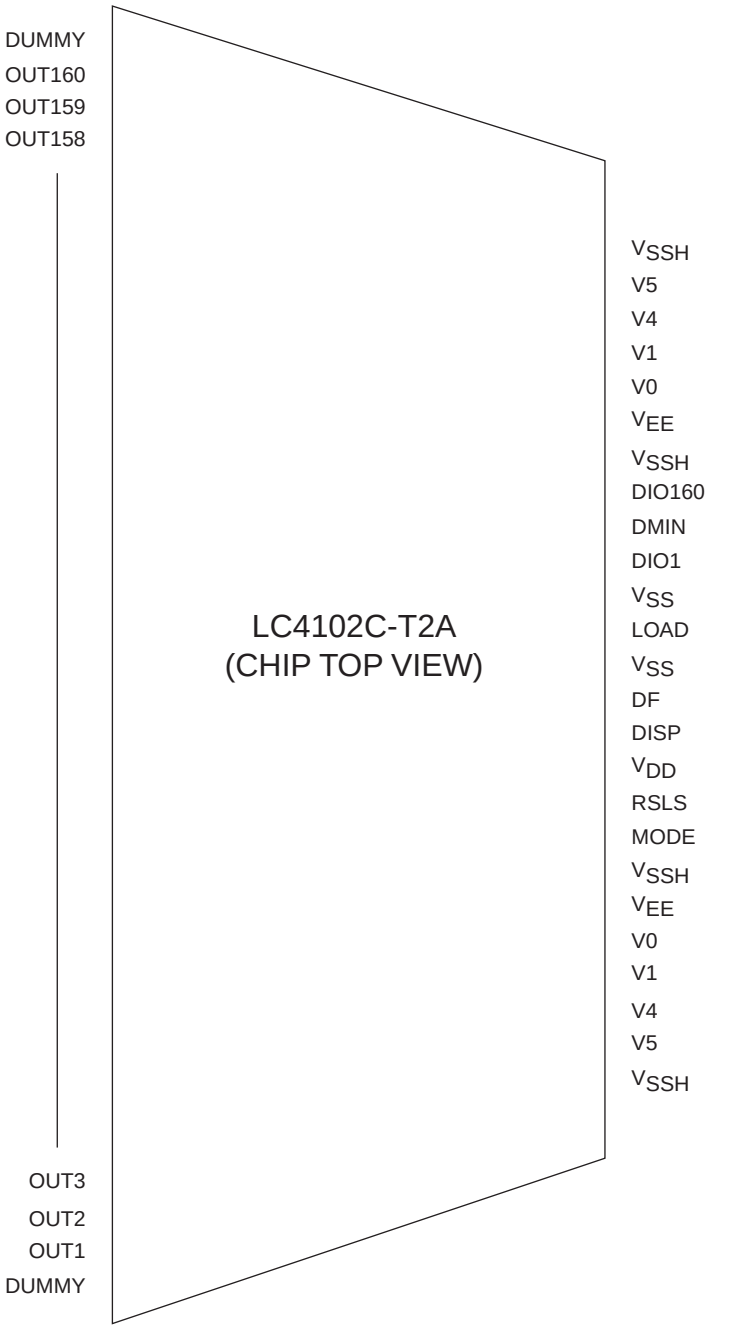
Switching Characteristics



Pin Functions

<table>
<tr><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>OUT1 to
OUT160</td><td>O</td><td>LCD drive outputs
<table>
<tr><th>DF</th><th>Data</th><th>DISP</th><th>OUTn</th></tr>
<tr><td>L</td><td>H</td><td>H</td><td>V0</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V4</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V5</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V5</td></tr>
</table>
*: don’t care</td></tr>
<tr><td>V0</td><td>I</td><td>V0 level drive voltage input</td></tr>
<tr><td>V1</td><td>I</td><td>V1 level drive voltage input</td></tr>
<tr><td>V4</td><td>I</td><td>V4 level drive voltage input</td></tr>
<tr><td>V5</td><td>I</td><td>V5 level drive voltage input</td></tr>
<tr><td>V_{EE}</td><td>–</td><td>High-voltage block power supply</td></tr>
<tr><td>V_{SSH}</td><td>–</td><td>High-voltage block ground</td></tr>
<tr><td>DISP</td><td>I</td><td>LCD off function. All outputs will be held at a fixed V5 level when this pin is low.</td></tr>
<tr><td>DF</td><td>I</td><td>Alternation input</td></tr>
<tr><td>LOAD</td><td>I</td><td>Data shift pulse input (falling edge)</td></tr>
<tr><td>MODE</td><td>I</td><td rowspan="4">Data shift direction specification input
<table>
<tr><th>MODE</th><th>RS/LS</th><th>Shift direction</th><th>DIO1</th><th>DIO160</th><th>DMIN</th></tr>
<tr><td>L</td><td>L</td><td>OUT160 → OUT1</td><td>OUT</td><td>IN</td><td>*</td></tr>
<tr><td>L</td><td>H</td><td>OUT1 → OUT160</td><td>IN</td><td>OUT</td><td>*</td></tr>
<tr><td>H</td><td>L</td><td>OUT160 → OUT81
OUT80 → OUT1</td><td>OUT</td><td>IN</td><td>IN</td></tr>
<tr><td>H</td><td>H</td><td>OUT1 → OUT80
OUT81 → OUT160</td><td>IN</td><td>OUT</td><td>IN</td></tr>
</table>
*: don’t care (Must be fixed at low or high.)</td></tr>
<tr><td>RS/LS</td><td>I</td></tr>
<tr><td>DIO1
DMIN
DIO160</td><td>I/O
I
I/O</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Logic system power supply</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Logic system ground</td></tr>
</table>

Pin Assignment



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Note: This figure shows the chip pattern surface as seen from abobe.
This figure dose not stipulate the TCP package.

Package Dimensions

unit: mm

LC4102C-T2A