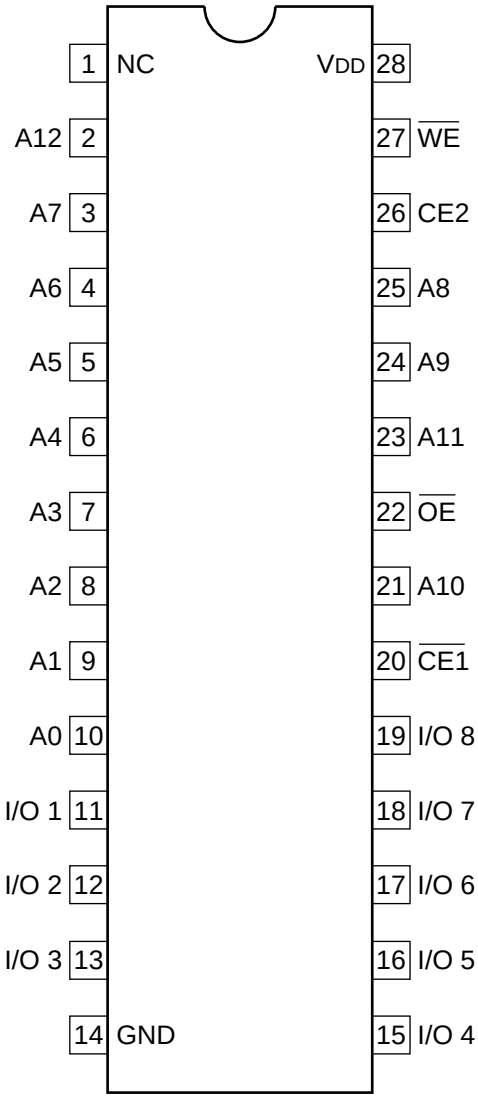
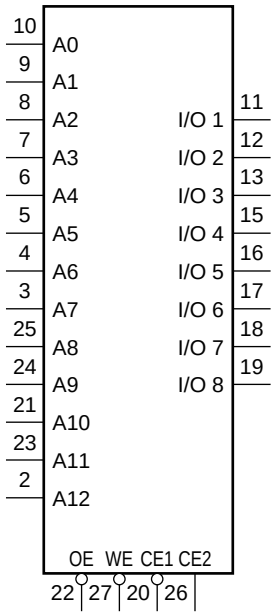
C-MOS 64 K (8192 × 8)-BIT SRAM

—TOP VIEW—





A0 - A12 ; ADDRESS INPUTS
$\overline{CE1}$, CE2 ; CHIP ENABLE INPUT
I/O 1 - I/O 8 ; DATA INPUT/OUTPUT
$\overline{OE}$; OUTPUT ENABLE INPUT
$\overline{WE}$; WRITE ENABLE INPUT

CE1	CE2	OE	WE	MODE	I/O TERMINAL
1	×	×	×	NOT SELECT	HIGH IMPEDANCE
×	0	×	×	NOT SELECT	HIGH IMPEDANCE
0	1	1	1	OUTPUT DISABLE	HIGH IMPEDANCE
0	1	0	1	READ	OUTPUT DATA
0	1	×	0	WRITE	INPUT DATA

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE