



LB1619M

3-Phase Brushless Motor Driver

Applications

The LB1619M is a 3-phase brushless motor driver IC ideally suited for use in VCR capstan motor driver, drum motor driver applications.

Features

- 120° voltage linear type.
- Speed control based on motor voltage control.
- Soft switching type eliminating noises caused by current switching and making the values of external capacitors smaller (comparable to those of chip capacitors).
- On-chip torque ripple compensation circuit.
- On-chip thermal shutdown circuit.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		16	V
Maximum supply voltage	V _S max		V _{CC}	V
Output current	I _O		1.5	A
Hall supply current	I _H		20	mA
Allowable power dissipation	P _d max		1.0	W
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		6 to 16	V

(Design Notes) It should be noted that dielectric breakdown is liable to occur between pin 11 and other pins.

Electrical Characteristics at Ta = 25°C, V_{CC}=12V, V_S=3V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	I _{CC}	V _{BR} =5V		18	23	mA
Supply current 2	I _S	V _{BR} =5V		5.0	7.0	mA
Supply standby current	I _{CCOQ}	V _{STBY} =0V			180	μA
Output saturation voltage	V _{O(sat)}	I _O =1.0A, sink+source			2.3	V

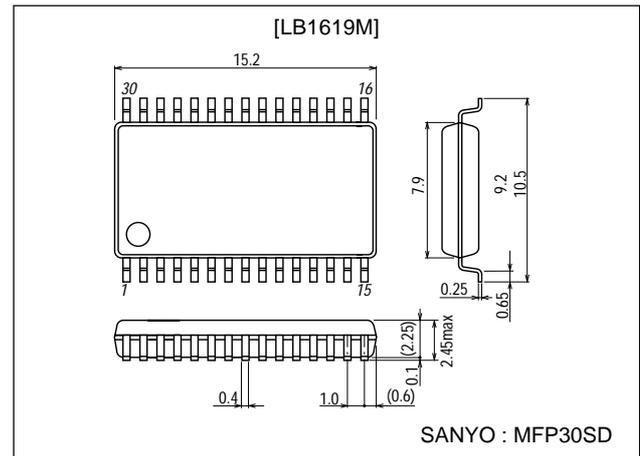
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Package Dimensions

unit:mm

3073B-MFP30SD



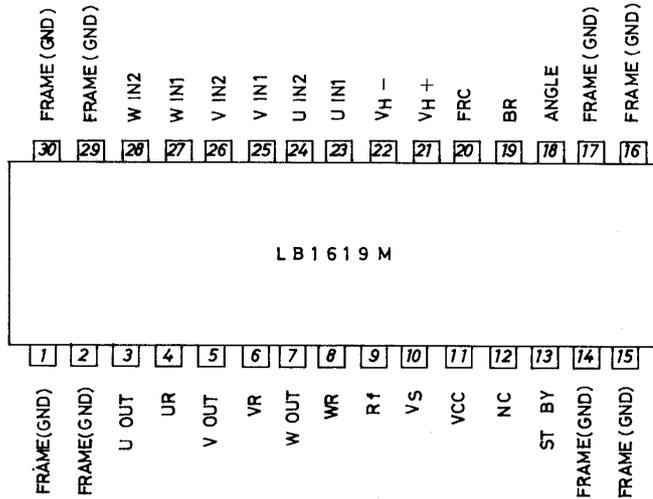
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output transistor breakdown voltage	$V_{O(sus)}$	$I_{OUT}=20mA$ *	16			V
Output standby voltage	V_{OQ}	$V_{BR}=5V$	1.43	1.53	1.63	V
Hall amplifier input offset voltage	$V_{HOFFset}$	*	-5		+5	mV
Hall amplifier common-mode input voltage range	V_{HCOM}		1.4		2.8	V
Hall input-output voltage gain	G_{VHO}	Under specified circuit conditions	31.5	34.5	37.5	dB
Brake pin high-level voltage			2.0			V
Brake pin low-level voltage					0.8	V
Brake pin input current					100	μA
Brake pin leak current					-30	μA
FRC pin high-level voltage			2.8			V
FRC pin low-level voltage					1.2	V
FRC pin input current					100	μA
FRC pin leak current					-30	μA
Hall supply voltage	V_H	$I_H=10mA$ $V_{H(+)}-V_{H(-)}$	0.8	1.0	1.5	V
Upper residual voltage	V_{XH}	$I_{OUT}=100mA$	0.40	0.6	0.75	V
Lower residual voltage	V_{XL}	$I_{OUT}=100mA$	0.5	0.6	0.7	V
Residual voltage inflection point				2.0		V
Overlap amount		$V_{CC}=12V$, $V_S=3.5V$	60	70	80	%
Operating temperature of thermal shutdown circuit		*	150	180	210	$^{\circ}C$
Hysteresis of thermal shutdown circuit		*		15		$^{\circ}C$
Standby operating voltage					0.1	V
Standby bias current		Pin GND			10	μA
V_S OFF-state IC flow-out/in current		Number of revolutions : 1260rpm			0.8	A

Note) * : Values shown are design targets only. No measurements have been taken.
 Overlap amount : Value measured at the time of shipment.

Pin Assignment



Note : All FRAME pins are connected to GND.

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Truth Table

	Source	sink	Input			Forward/Reverse Control
			U	V	W	
1	W phase → V phase		H	H	L	L
	V phase → W phase		H	H	L	H
2	W phase → U phase		H	L	L	L
	U phase → W phase		H	L	L	H
3	V phase → W phase		L	L	H	L
	W phase → V phase		L	L	H	H
4	U phase → V phase		L	H	L	L
	V phase → U phase		L	H	L	H
5	V phase → U phase		H	L	H	L
	U phase → V phase		H	L	H	H
6	U phase → W phase		L	H	H	L
	W phase → U phase		L	H	H	H

Input :

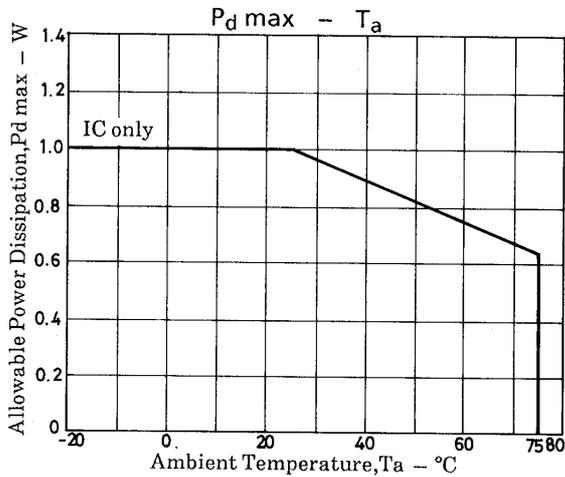
H : High level. One of the inputs should have a potential at least 0.2V higher than the other.

L : Low level. One of the inputs should have a potential at least 0.2V lower than the other.

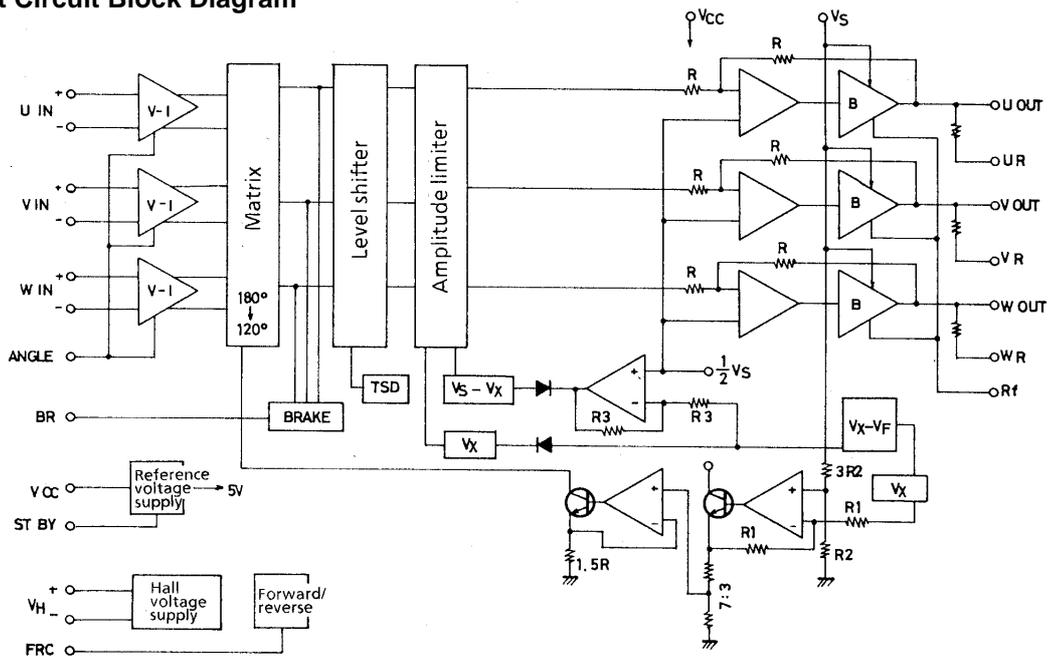
Forward/reverse control :

H : 2.8 to 5V

L : 0 to 1.2V



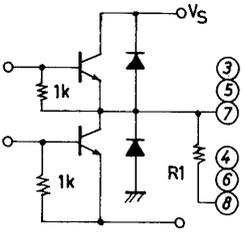
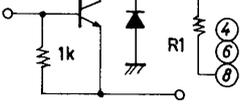
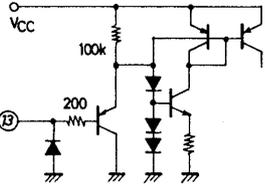
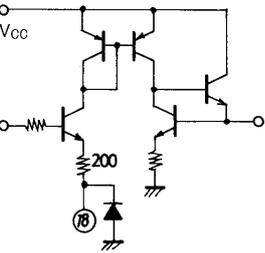
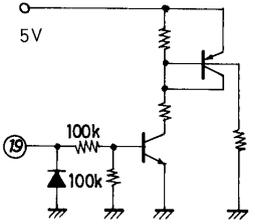
Equivalent Circuit Block Diagram



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Pin Function

Unit (resistance : Ω)

Pin No.	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
1, 2 14, 15 16, 17 29, 30	FRAME (GND)			GND for other than output.
3 5 7	U_{out} V_{out} W_{out}			Output pins.
4 6 8	U_R V_R W_R			Output pins with resistor of 2Ω .
9	R_f			GND for output transistor.
10	V_S	$<V_{CC2}$		Power supply pin for fixing the output amplitude. Must be lower than V_{CC2} voltage.
11	V_{CC}			Power supply pin for power amplifier circuit other than motor driver transistor.
13	ST, BY	L : 0.1V max H : 2.0V min		When this pin is grounded, all the circuitry stops operating. In this case, the supply current is approximately $100\mu A$. In the normal operation mode, this pin is left open or made to be at a potential of more than 2V.
18	ANGLE			The hall input-output gain (slope of motor waveform) can be changed by changing the resistance connected across this pin and GND. $\approx 10k\Omega$.
19	BR	H : 2.0V min L : 0.8V max		Pin for stopping the motor L level : Motor drive (Less than 0.8V). H level : Motor stop (More than 2.0V).

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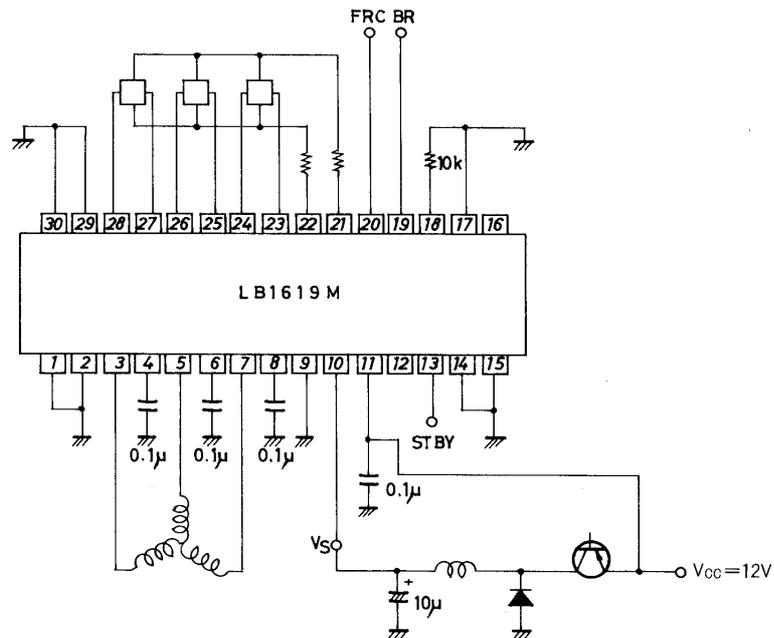
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Unit (resistance : Ω)

Pin No.	Pin Symbol	Pin Voltage	Equivalent Circuit	Pin Description
20	FRC	H : 2.8V min L : 1.2V max		Pin for forward/reverse control of motor. L level : Forward (Less than 1.2V). H level : Reverse (More than 2.8V).
21 22	V _H ⁺ V _H ⁻			Pin for supplying the hall bias current. A voltage of approximately 1V is developed across (V _H ⁺) and (V _H ⁻).
23 24 25 26 27 28	U _{IN} 1 U _{IN} 2 V _{IN} 1 V _{IN} 2 W _{IN} 1 W _{IN} 2	1.4V min 2.8V max		U phase hall element input pin. Logic "H" : U _{IN} 1 > U _{IN} 2 V phase hall element input pin. Logic "H" : V _{IN} 1 > V _{IN} 2 W phase hall element input pin. Logic "H" : W _{IN} 1 > W _{IN} 2

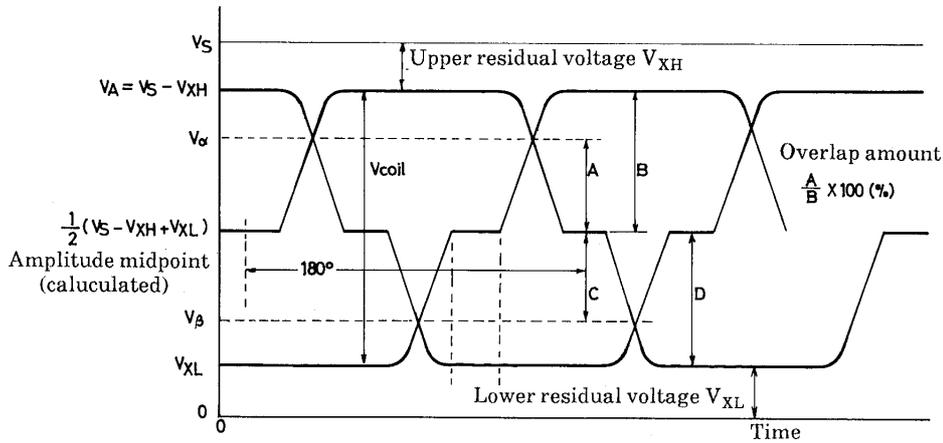
Note) Pin 12 (NC pin) must be left open.

Sample Application Circuit



Unit (resistance: Ω , capacitance: F)

Output Voltage Waveform



$$\text{Upper overlap} = (2V\alpha - V_A - V_{XL}) / (V_A - V_{XL}) \times 100[\%]$$

$$\text{Lower overlap} = (V_A + V_{XL} - 2V\beta) / (V_A - V_{XL}) \times 100[\%]$$

1. Upper overlap

DC voltage of upper amplitude : $V_S - V_{XH} = V_A$

DC voltage of lower amplitude : V_{XL}

Let the DC voltage at the intersection of two phases of the upper waveform be $V\alpha$:

From the drawing shown above

At upper overlap amount = $A/B \times 100[\%]$

$$A = V\alpha - 1/2(V_S - V_{XH} + V_{XL}) = V\alpha - 1/2(V_A + V_{XL})$$

$$B = (V_S - V_{XH}) - 1/2(V_S - V_{XH} + V_{XL}) = 1/2(V_A + V_{XL})$$

* Upper overlap

$$= (2V\alpha - V_A - V_{XL}) / (V_A - V_{XL}) \times 100[\%]$$

2. Lower overlap

DC voltage of upper amplitude : $V_S - V_{XH} = V_A$

DC voltage of lower amplitude : V_{XL}

Let the DC voltage at the intersection of two phases of the upper waveform be $V\beta$:

From the drawing shown above

At lower overlap amount = $C/D \times 100[\%]$

$$C = 1/2(V_S - V_{XH} + V_{XL}) - V\beta = 1/2(V_A + V_{XL}) - V\beta$$

$$D = 1/2(V_S - V_{XH} + V_{XL}) - V_{XL} = 1/2(V_A - V_{XL})$$

* Lower overlap

$$= (V_A - V_{XL} - 2V\beta) / (V_A - V_{XL}) \times 100[\%]$$

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