Ordering number : ENN7131

Monolithic Linear IC

LA9239T

48× CD-ROM Digital Servo RF IC

Overview

The LA9239T is a CD-ROM digital servo RF IC that supports high-speed CD-ROM drive replay of up to 48×. It also supports RW disks by featuring an on-chip servo VCA and gain switch.

Features

The LA9239T is an IC that features on-chip functions for improved playability and an RF equalizer, resulting in superior performance and a reduced need for external components.

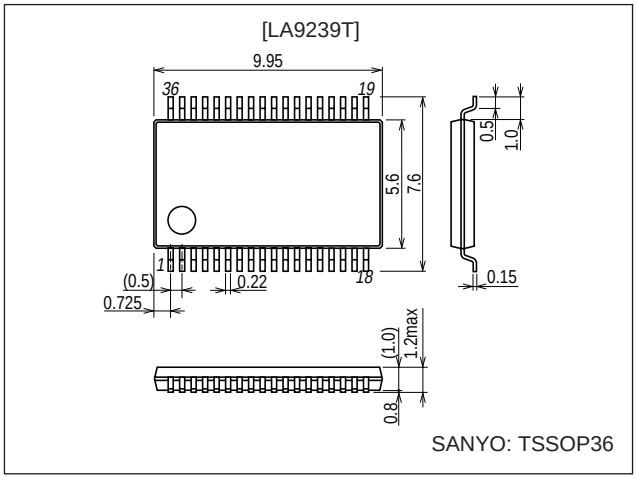
Functions

- RF amplifier (with AGC)
- RF gain amplifier (supporting CD-RW disk replay)
- RF equalizer (7 modes)
- RF hold function
- PH/BH detection
- 3T extraction circuit
- FE amplifier (built-in balance adjustment VCA)
- TE amplifier (built-in balance adjustment VCA)
- servo signal VCA circuit
- APC circuit (with laser power-up function)
- sleep function

Package Dimensions

unit: mm

3253-TSSOP36



Specifications

Maximum Ratings at Ta = 25°C, Pins 4 and 31 = GND

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V_{CC} max		7	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–25 to +70	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended power supply voltage	V_{CC}		5	V
Allowable operating voltage range	V_{CC} op		4.5 to 5.5	V

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Operating Characteristics at Ta = 25°C, V_{CC} (Pins 23, 34) = 5 V, GND (Pins 4, 31) = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	No signal	18	30	42	mA
Current drain (during sleep)	I_{CCS}	No signal, EQS = 0 V	2	6	10	mA
Reference voltage	Vref		2.3	2.5	2.7	V
Preamplifier offset	RFAOost	Difference with VR in RFA0	–120	0	+120	mV
RF no-signal voltage	RFSM	FIN1, FIN2 = VR	1.5	1.8	2.3	V
RF gain max	RFG1	GHS = 0 V	19	21	23	dB
RF gain min	RFG2	GHS = 0 V	4	6	8	dB
RF gain UP	RFGUP	GHS = 5 V	12.5	14	15.5	dB
RFEQ normal	RFEQN	RFSM difference when FIN1, 2: 350 mVp-p, f = 1 MHz and 350 mVp-p, f = 100 kHz, EQS = 5 V, BHC = 2.45 V, PHC = 2.8 V	1.5	3.5	5.5	dB
RFEQ CAV1	RFEQ1	RFSM difference when FIN1, 2: 350 mVp-p, f = 2.4 MHz and 350 mVp-p, f = 100 kHz, EQS = 4.1 V, BHC = 2.45 V, PHC = 2.8 V	1	3	5	dB
RFEQ CAV2	RFEQ2	RFSM difference when FIN1, 2: 350 mVp-p, f = 4.4 MHz and 350 mVp-p, f = 100 kHz, EQS = 3.4 V, BHC = 2.45 V, PHC = 2.8 V	1	3	5	dB
RFEQ CAV3	RFEQ3	RFSM difference when FIN1, 2: 350 mVp-p, f = 6 MHz and 350 mVp-p, f = 100 kHz, EQS = 2.8 V, BHC = 2.45 V, PHC = 2.8 V	1	3	5	dB
RFEQ CAV4	RFEQ4	RFSM difference when FIN1, 2: 350 mVp-p, f = 8 MHz and 350 mVp-p, f = 100 kHz, EQS = 2.2 V, BHC = 2.45 V, PHC = 2.8 V	1	3	5	dB
RFEQ CAV5	RFEQ5	RFSM difference when FIN1, 2: 350 mVp-p, f = 12 MHz and 350 mVp-p, f = 100 kHz, EQS = 1.6 V, BHC = 2.45 V, PHC = 2.8 V	1	3	5	dB
RFEQ CAV6	RFEQ6	RFSM difference when FIN1, 2: 350 mVp-p, f = 30 MHz and 350 mVp-p, f = 100 kHz, EQS = 0.9 V, BHC = 2.45 V, PHC = 2.8 V	0.5	2.5	4.5	dB
RF hold	RFHLD	FIN1, 2: 700 mVp-p, f = 100 kHz, RHLD = 5 V	–13.5	–11	–8.5	dB
PH	PH	RFSM = 1.7 Vp-p	2.7	3.3	3.9	V
3T extraction	3TON	Difference with RFSM for 3TON = 5 V, PH	–20	–16.5	–13	dB
BH	BH	RFSM = 1.7 Vp-p	1.3	1.6	1.9	V
BH band switch	BHH	f = 100 kHz, RHH = 5 V	7	9	11	dB
REFL offset	REFLost	Difference with VR for REFL	–120	0	+120	mV
REFL gain 1	REFL1	FIN1 = Vin, FIN2 = VR, SGC = 2 V	9	11	13	dB
REFL gain 2	REFL2	FIN1 = Vin, FIN2 = VR, SGC = 3 V	14.5	16.5	18.5	dB
FE offset	FEost	Difference with VR for FE	–120	0	+120	mV
FE gain 1	FEG1	FIN1 = Vin, FIN2 = VR, SGC = 2 V, FBAL = VR	5	7	9	dB
FE gain 2	FEG2	FIN1 = Vin, FIN2 = VR, SGC = 3 V, FBAL = VR	10	12	14	dB
FE balance 1	FBAL1	FIN1 = Vin, FIN2 = VR, SGC = VR, FBAL = 2 V	10.5	12.5	14.5	dB
FE balance 2	FBAL2	FIN1 = Vin, FIN2 = VR, SGC = VR, FBAL = 3 V	7.5	9.5	11.5	dB
TE offset	TEost	Difference with VR for TE	–120	0	+120	mV
TE gain 1	TEG1	E = Vin, F = VR, SGC = 2 V, TBAL = VR	13.5	15.5	17.5	dB
TE gain 2	TEG2	E = Vin, F = VR, SGC = 3 V, TBAL = VR	19	21	23	dB
TE balance 1	TBAL1	E = Vin, F = VR, SGC = VR, TBAL = 2 V	20	22	24	dB
TE balance 2	TBAL2	E = Vin, F = VR, SGC = VR, TBAL = 3 V	16	18	20	dB
TS offset	TSost	Difference with VR for TS	–120	0	+120	mV
TS gain 1	TSG1	GHS = 0 V, TBAL = VR	13	15	17	dB
TS gain 2	TSG2	GHS = 5 V, TBAL = VR	25	27	29	dB
TS band 1	TSHL	TE-TE- = 82 P, TSH = 0 V	16	20	24	kHz
TS band 2	TSHH	TE-TE- = 82 P, TSH = 5 V	240	300	360	kHz
APC reference voltage 1	LDSL	LSD voltage for LDD = 3 V, LDON = 0 V	175	190	205	mV
APC reference voltage 2	LDSH	LSD voltage for LDD = 3 V, LDON = 5 V	215	230	245	mV
APC off voltage	LDD	LDON = VR	4	4.3	5	V

Explanation of Operation

(1) RF amplifier

The RF signal is generated by inputting (A+C) from FIN2 (pin 8) and (B+D) from FIN1 (pin 7) and adding the two. The EFM signal is output from the RFSM (pin 33) via the preamplifier, gain switch, RFAGC circuit, and 3T compensation circuit. The RFSUM output D range is 1 to 4 V. 3T compensation can be done according to the band through the EQS (pin 18) control pin.

The gain switch enables replay of CD and CD-RW disks, and when GHS (pin 16) level is made Hi (CD-RW mode), a gain of 14 dB can be obtained. In the CD mode, the gain is 0 dB.

The on-chip AGC circuit has a variable range of ±6 dB. The peak level controls the RFAGC level, and the bottom level controls the DC level of RF. The respective frequency response characteristics can be changed with the external capacitors connected to PHC (pin 2) and BHC (pin 1).

The response frequency is proportional to the capacitance of the PHC and BHC capacitors.

When a defect is detected in the DSP, AGC control can be changed to the hold status (by making RHLD (pin 32) Hi) to prevent the RF signal from becoming unstable.

(2) Focus error amplifier

The focus error signal is generated by inputting (A+C) to FIN2 (pin 8) and (B+D) to FIN1 (pin 7), passing these signals through the focus balance adjustment VCA, and extracting the difference between the two ((B+D)–(A+C)). The FE signal is gain controlled by FE-VCA and output to FE (pin 28). The FE signal gain can be set with the resistor connected between FE and FE- (pin 29).

The focus balance adjustment VCA is controlled by FBAL (pin 21), and FE-VCA is controlled by SGC (pin 19). A gain of +12 dB for the FE signal gain is obtained in the RW mode by making the GS level Hi.

Note: The polarity of the FE output in relation to the FIN1 input is common-mode output.

(3) Tracking error amplifier

The tracking error signal is generated through input to E (pin 9) and F (pin 10), passing the signals through the tracking balance adjustment VCA, and detecting their difference. The TE signal is gain controlled at TE-VCA and output from TE (pin 26). The TE signal gain can be set with the resistor connected between TE and TE- (pin 27). The tracking balance adjustment VCA is controlled by TBAL (pin 20), and TE-VCA is controlled by SGC (pin 19).

The TE signal for the TES comparator is output from TS (pin 23). The TS signal level must meet the TES comparator level in the DSP. Setting of this level is performed with the pickup output and the resistor between the E and F inputs. In the RW mode, a gain of +12 dB for TE and TS signal gain is obtained by making the GHS (pin 16) level Hi (same as for RF). An on-chip band switch is also provided to support high-speed seek for the TS signal, which is controlled with TSH (pin 22). The band can be set with the capacitance between TSS (pin 25) and TS.

Note: The polarity of the TE output in relation to the E input is inverted output, and the polarity of the TS output in relation to the E input is also inverted output.

(4) APC (auto laser power control)

The APC controls the pickup laser power. Since CD-RW disks are also supported, a laser power-up (+20%) function is also provided. Laser ON/OFF and laser power-up control are performed with LDON (pin 15).

(5) REFL detection (reflected light detection) and focus detection

The reflected light amount signal from the disk is added to the FIN1 and FIN2 inputs (A+B+C+D) and fetched. It is then gain controlled at REFL-VCA and output from REFL (pin 30) to the DSP. This output signal is used to control SGC (pin 19) to secure the D range of the servo signal in relation to disk irregularities. The amount of light is judged by the DSP and SGC control is performed. REFL-VCA is controlled by SGC. During RW replay, the REFL gain is increased by 12 dB (GHS = Hi).

The REFL signal is also used as a signal for focus detection.

Note: The polarity of the REFL output in relation to the FIN1 input is common-mode output.

(6) BH (RF bottom hold signal)

The HFL (mirror) detection signal is generated at BH (pin 35), and HFL (mirror) is detected in the DSP. The DSP detects the track jump direction using the phase difference with TES. Moreover, this BH circuit has a band switching function that can be controlled with BHH (pin 17). (BHH = Hi for wide band)

(7) PH (RF peak hold signal)

The RF peak hold signal used for defect detection is output from PH. The DSP performs defect detection judgments based on this signal. Since the EFM signal level is not necessarily stable due to the influence of the disk's reflection factor, consideration must be paid to using as reference the PH signal level measured when there are no scratches, for defect judgment. Moreover, the PH circuit performs constant settings during PH demodulation according to the speed. This is controlled along with the RF equalizer by the EQS (pin 18) control pin.

The system is designed so that, during focus balance adjustment, the peak and bottom levels of the 3T component are detected and output as the error signal. During focus balance adjustment, 3T is extracted and output from PH and BH by setting 3TON (pin 6) to Hi.

(8) Sleep

The sleep status can be selected in order to reduce the current drain of the IC.
(Sleep is selected with EQS (pin 18) = GND.)

Usage Note

The level of the signals input to FIN1 (pin 7), FIN2 (pin 8), E (pin 9), and F (pin 10) must be set so that it is higher than the reference voltage (VREF).

Relationships between control pin voltages and operation modes

1. 3TON (pin 6)
   Extracts 3T and performs focus balance adjustment.

Mode	Min	Max	Extraction Frequency
3TON	3.0 V	5.0 V	10 MHz
3TOFF	0 V	2.0 V	—

2. LDON (pin 15)
   Laser ON and laser power-up (20%) switch control

Mode	Min	Max	Laser	Power Up
PUPH	3.5 V	5.0 V	ON	Hi
LDOF	2.0 V	3.0 V	OFF	Low
LDON+PUPL	0 V	1.5 V	ON	Low

3. GHS (pin 16)
   RF and TS gain-up (+14 dB) switch control

Mode	Min	Max	Gain Up
RW support	3.0 V	5.0 V	Hi
CD support	0 V	2.0 V	Low

4. BHH (pin 17)
   Reduces the time constant during bottom hold when the access speed is slow.

Mode	Min	Max	Band (fc)
Hi (during normal operation)	3.0 V	5.0 V	450 kHz
Low (when access speed is slow)	0 V	2.0 V	80 kHz

5. TSH (pin 22)
   TS filter setting pin for TES signal

TSH	Min	Max	TS Band
Hi (during seek)	3.0 V	5.0 V	300 kHz
Low (other than seek)	0 V	2.0 V	20 kHz (between pins 24 and 25: 80P)

6. EQS (pin 18)
   RF equalizer, PH detection time constant control (7 modes), and sleep switch control
   PH time constant switching is done according to the equalizer switch.

Mode	Min	Max	+2 dB Boost Frequency	11T Frequency
Normal	4.5 V	5.0 V	Approx. 1.0 MHz	Approx. 200 kHz
CAV1	3.9 V	4.3 V	Approx. 2.4 MHz	Approx. 2.4 MHz
CAV2	3.2 V	3.6 V	Approx. 4.3 MHz	Approx. 3.5 MHz
CAV3	2.6 V	3.0 V	Approx. 6.0 MHz	Approx. 3.9 MHz
CAV4	2.0 V	2.4 V	Approx. 8.0 MHz	Approx. 4.7 MHz
CAV5	1.4 V	1.8 V	Approx. 11 MHz	Approx. 5.9 MHz
CAV6	0.8 V	1.2 V	Approx. 30 MHz	Approx. 9.4 MHz
Sleep	0 V	0.5 V	—	—

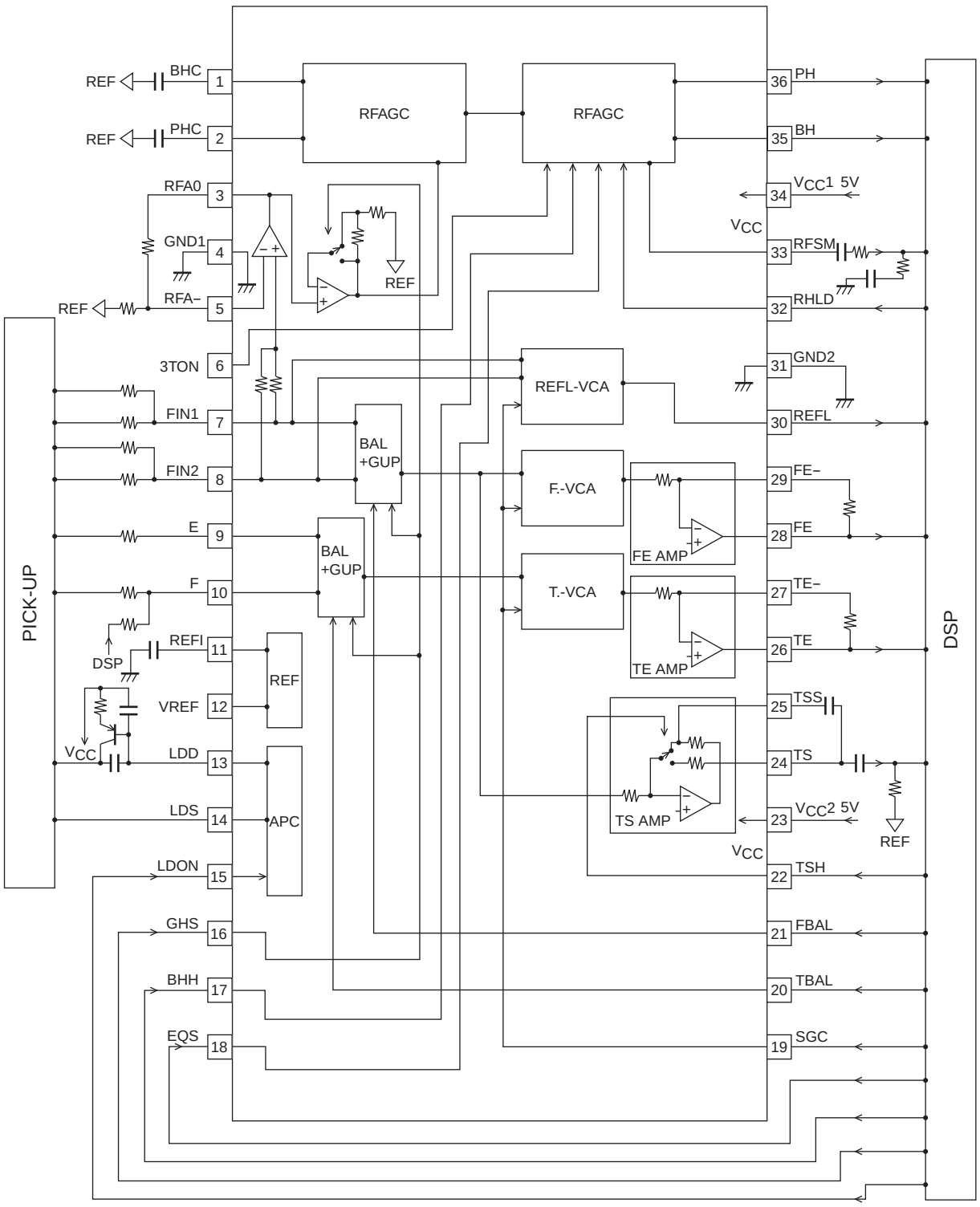
7. RHLD (pin 32)

RHLD	Min	Max
Hi (during defect detection)	3.0 V	5.0 V
Low (during normal operation)	0 V	2.0 V

Pin Description

Pin No.	Pin Name	Description
1	BHC	Bottom hold capacitor connection pin for RF AGC detection
2	PHC	Peak hold capacitor connection pin for RF AGC detection
3	RFAO	RF preamplifier output pin
4	GND1	RF signal GND pin
5	RFA–	RF preamplifier minus input pin
6	3TON	3T extraction circuit control pin
7	FIN1	Pickup voltage output connection pin. The RF signal and mirror signal are generated by adding FIN1 to FIN2, and the FE signal is generated by subtracting FIN1 from FIN2.
8	FIN2	Pickup voltage output connection pin
9	E	Pickup voltage output connection pin. The TE signal is generated by subtracting E from F.
10	F	Pickup voltage output connection pin
11	REFI	Reference voltage bus capacitor connection pin
12	VREF	Reference voltage output pin
13	LDD	APC circuit output pin
14	LDS	APC circuit input pin
15	LDON	Laser ON/OFF, laser power-up control pin
16	GHS	RF, TS signal gain switch pin (0 dB/+14 dB)
17	BHH	BH response switch pin
18	EQS	RF equalizer, PH detection control pin
19	SGC	Servo gain control pin (FE, TE, REFL signals)
20	TBAL	TE balance adjustment pin
21	FBAL	FE balance adjustment pin
22	TSH	TS signal band control pin
23	VCC2	Servo signal VCC pin
24	TS	TS signal (TES signal source) output pin (→ DSP)
25	TSS	TS signal band setting pin
26	TE	TE signal output pin (→ DSP)
27	TE–	TE signal gain setting pin
28	FE	FE signal output pin (→ DSP)
29	FE–	Servo signal GND pin
30	REFL	Reflection signal output pin (→ DSP)
31	GND2	Servo signal GND pin
32	RHLD	RF hold control pin
33	RFSM	EFM signal output pin (→ DSP)
34	VCC1	RF signal VCC pin
35	BH	RF bottom hold signal output pin (→ DSP)
36	PH	RF peak hold signal output pin (→ DSP)

Block Diagram



Test Circuit