Ordering number : EN4702

Monolithic Linear IC

LA7156

Video and Audio Switch for PAL-SECAM 21-Pin Interface

Overview

The LA7156 is a switching IC for use with the PAL and SECAM 21-pin connector interface. The LA7156 integrates video and audio switches in a single chip, and allows significant block reorganization and integration by providing function switching outputs with current limiters, 75 Ω video drivers, muting and other functions. The LA7156 provides a diverse set of functions, including support for single-wire serial bus control that allows complex logic to be handled by microprocessor software.

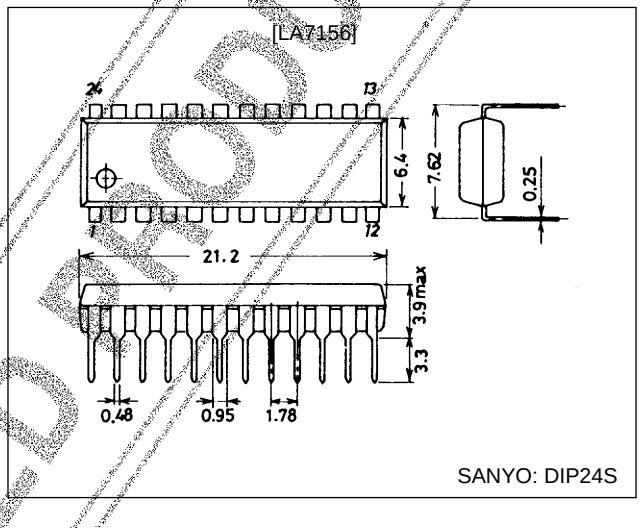
Functions and Features

- Three audio and three video switching systems
- Audio output and video decoder output muting function
- Video input sync chip clamp
- Two 6 dB video amplifier plus 75 Ω driver systems
- VPS decoder output
- FSS output with current limiting
- 5 V regulator built-in
- Serial control

Package Dimensions

unit: mm

3067-DIP24S



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		15	V
Allowable power dissipation	Pd max	Ta ≤ 65°C	800	mW
Operating temperature	Topr		–20 to +65	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		9, 12	V
Operating supply voltage range	V_{CC} op		8 to 13	V

Operating Characteristics at Ta = 25°C, V_{CC} = 9 V and 12 V

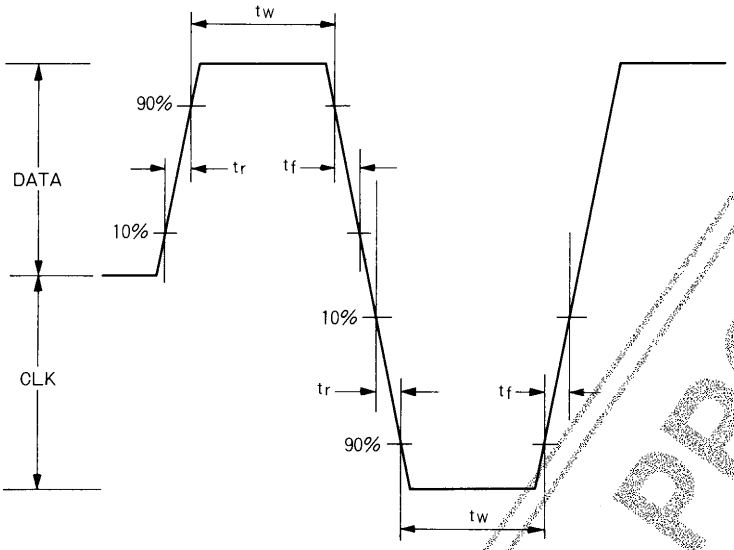
Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{CC}	No input	32	40	48	mA
FSS output high level voltage 1	VHFSS1	V_{CC} = 9 V, load resistance: 10 kΩ	7.5	8.9	9.0	V
FSS output low level voltage 1	VLFSS1	V_{CC} = 9 V, load resistance: 10 kΩ		0	0.5	V
FSS output high level voltage 2	VHFSS2	V_{CC} = 12 V, load resistance: 10 kΩ	10.5	11.9	12.0	V
FSS output low level voltage 2	VLFSS2	V_{CC} = 12 V, load resistance: 10 kΩ		0	0.5	V
FSS output cutoff current 1	$I_{CUTOFF}1$	V_{CC} = 9 V, the outflow current when the FSS output is grounded		9.3	40.0	mA
FSS output cutoff current 2	$I_{CUTOFF}2$	V_{CC} = 12 V, the outflow current when the FSS output is grounded		9.8	40.0	mA
[Audio Switch Block]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, R_{OUT} = ∞		0.02	1	%
Maximum output voltage	V_O max	The output level when f = 1 kHz and THD = 2%	2	3		Vrms
Output noise voltage	V_{NO}	Rg = 600 Ω, DIN audio filter		–100	–90	dBV
Voltage gain A	VG_A	The TP6 and TP8 output levels when V_{IN} = 1 Vrms and f = 1 kHz	1.1	1.8	2.5	dB
Interchannel crosstalk A	CTA	V_{IN} = 1 Vrms, f = 1 kHz		–90	–70	dB
Muting attenuation A	VmuteA	V_{IN} = 1 Vrms, f = 1 kHz		–90	–70	dB
Output offset voltage	Vof	The offset voltage when the switch has changed state		0	20	mV
Input impedance A	Z_{IN}A		40	50	60	kΩ
[Video Switch Block]						
Voltage gain V	VG_V	The TP2 and TP5 output levels when V_{IN} = 1 Vp-p and f = 4.43 MHz	–1	0	+1	dB
Frequency characteristics	Vf	V_{IN} = 1 Vp-p, f = 100 k/7 MHz	–1.5	–0.5	+0.5	dB
Second harmonic	H2	V_{IN} = 1 Vp-p, f = 4.43 MHz		–45	–40	dB
Third harmonic	H3	V_{IN} = 1 Vp-p, f = 4.43 MHz		–50	–45	dB
Interchannel crosstalk V	CTV	V_{IN} = 1 Vp-p, f = 4.43 MHz		–50	–40	dB
Muting attenuation V	VmuteV	V_{IN} = 1 Vp-p, f = 4.43 MHz		–50	–40	dB
Output voltage	V_{OUT}	The TP5 DC voltage with no input		0.7	1.0	V
[Control Block]						
Serial control input high level	Vsh		4		5	V
Serial control input middle level	Vsm		2		3	V
Serial control input low level	Vsl		0		1	V
Pin 2 input high level	V2H		4		V_{CC}	V
Pin 2 input low level	V2L	*1	0		2	V
Pin 20 input high level	V20H		4		V_{CC}	V
Pin 20 input middle level	V20M	*2	2		3	V
Pin 20 input low level	V20L		0		1	V
Pin 7 output high level	V7H	The TP9 DC voltage when SW3 is in the A position	4.5	5.0	5.5	V
Pin 7 output low level	V7L	The TP9 DC voltage when SW3 is in the B position	0		1	V

Note: In the operating characteristics listed above, characteristics items that do not differ between V_{CC} = 9 V and 12 V are listed as the same item.

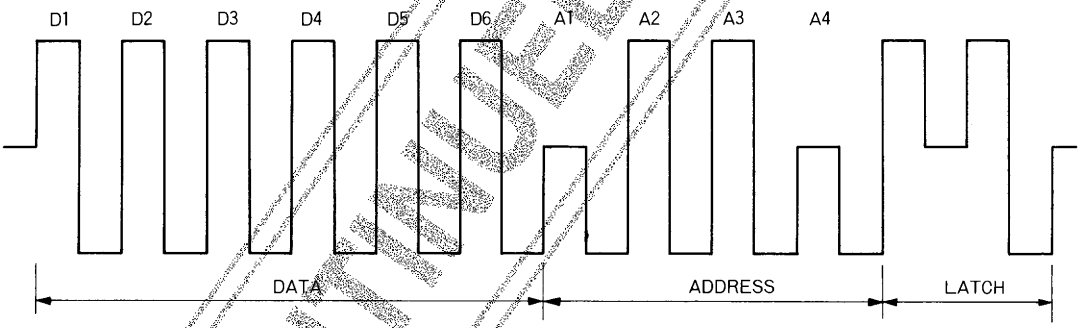
1. Forced to low when pin 2 is open.
2. Forced to the middle level when pin 20 is open.

Timing Characteristics

Parameter	Symbol	Conditions	min	typ	max	Unit
Minimum input pulse width	t_W		2			µs
Rise time	tr				20	µs
Fall time	tf				20	µs



Serial Control Input Specifications



LA7156 Command Address

Address	A1	A2	A3	A4
State	L	H	H	L

Switch Logic Values Table

The LA7156 provides the following switching control with control of pin 20.

1. Normal mode (when pin 20 is high)
   In this mode, the LA7156 functions, including switching, FSS output and muting, can be controlled from the six bits of serial data transferred from the microprocessor. However, note that the video and audio system switch operate at the same time in this mode.

DATA1		Switch state	Note
H		A.SW1-A, V.SW1-A	1, 2
L		A.SW1-B, V.SW1-B	1, 2
DATA2	DATA3	Switch state	Note
H	L	A.SW2-A, V.SW2-A	1, 2
L	L	A.SW2-B, V.SW2-B	1, 2
—	H	A.SW2-C, V.SW2-C	1, 2

DATA4	Switch state	Note
H	A.SW3-A, V.SW3-A, pin 7 high	1, 2
L	A.SW3-B, V.SW3-B, pin 7 low	1, 2
DATA5	FSS output state	Note
H	Output high	
L	Output low	
DATA6	Muted state	Note
H	Muted	
L	Mute released	

Note: 1. All the audio switch and the video SW3 outputs are forcibly muted when DATA6 is high or in muting mode.
2. A.SW indicates the audio system switches and V.SW indicates the video system switches.

2. Preset mode (when pin 20 is middle or low)
   This mode uses the LA7156 internally set up logic and the six bits of data are allocated to the VCR operating states to allow the switch states to be changed.

Serial Data

DATA No.	Item	H	L
D1	Power on/off	On	Off
D2	VCR/TV	VCR	TV
D3	Pay CH/Normal CH	Pay	Normal
D4	EXT/Tuner	EXT	Tuner
D5	PB/EE	PB	EE
D6	Mute on/off	On	Off

External Input Data

Pin No.	Item	H	L
P2	Decoder in	Scramble	Normal

Truth Table

Pin 20: Open or Middle

D1	D2	D3	D4	D5	P2	A.V.SW1	A.V.SW2	A.V.SW3	FSS out	Pin 7 out
L	—	—	—	—	H	A	C	A	L	H
L	—	—	—	—	L	A	C	A	L	H
H	L	—	L	L	H	A	A	A	L	H
H	L	—	L	L	L	A	C	A	L	H
H	H	—	L	L	H	A	A	A	H	H
H	H	—	L	L	L	A	C	A	H	H
H	L	—	H	L	H	A	B	A	L	H
H	L	—	H	L	L	A	B	A	L	H
H	H	—	H	L	H	A	B	A	H	H
H	H	—	H	L	L	A	B	A	H	H
H	—	—	—	H	H	A	*	A	H	H
H	—	—	—	H	L	A	*	A	H	H

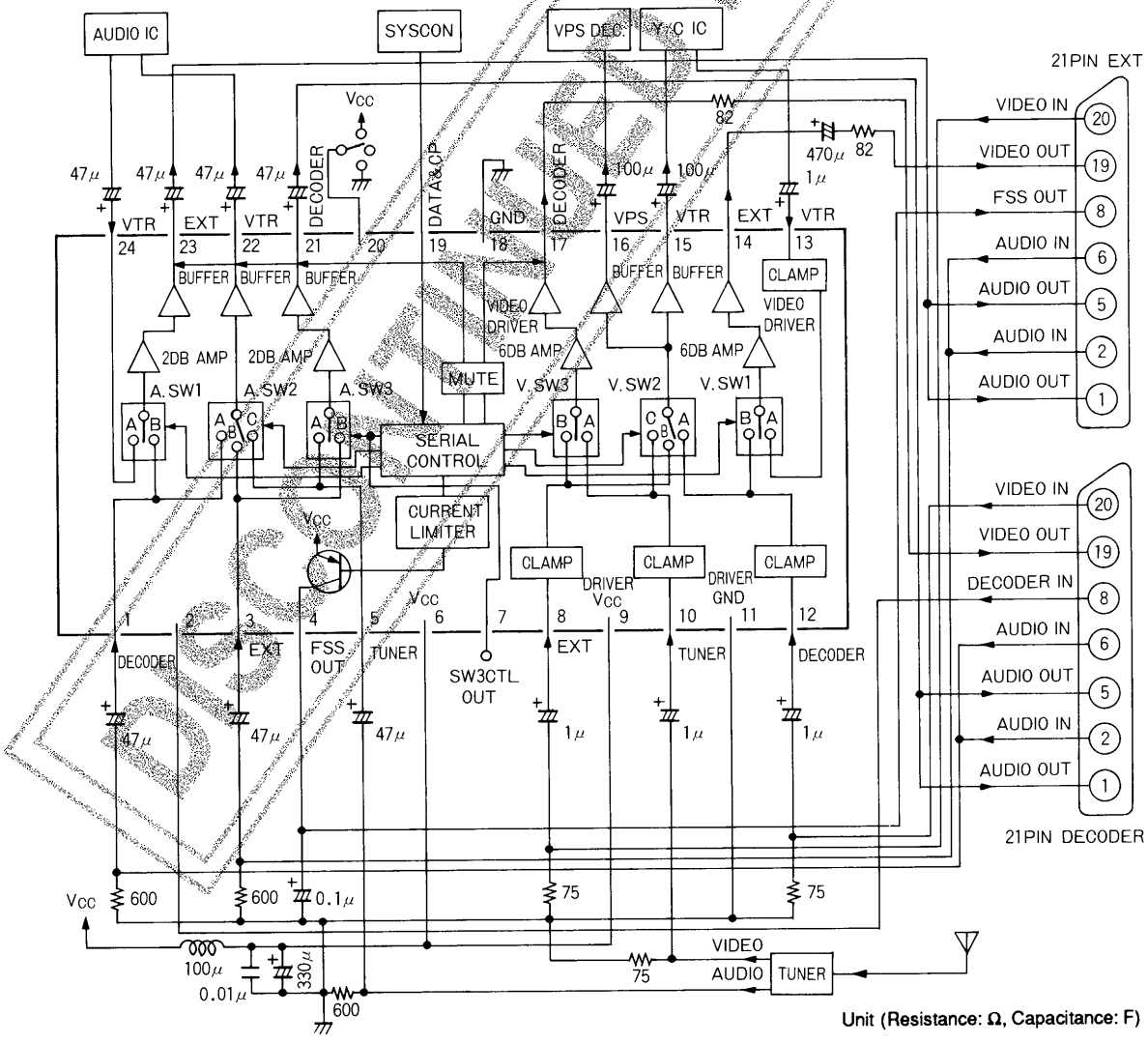
Note: The previous state is retained even if another switch is changed.

Pin 20: Low

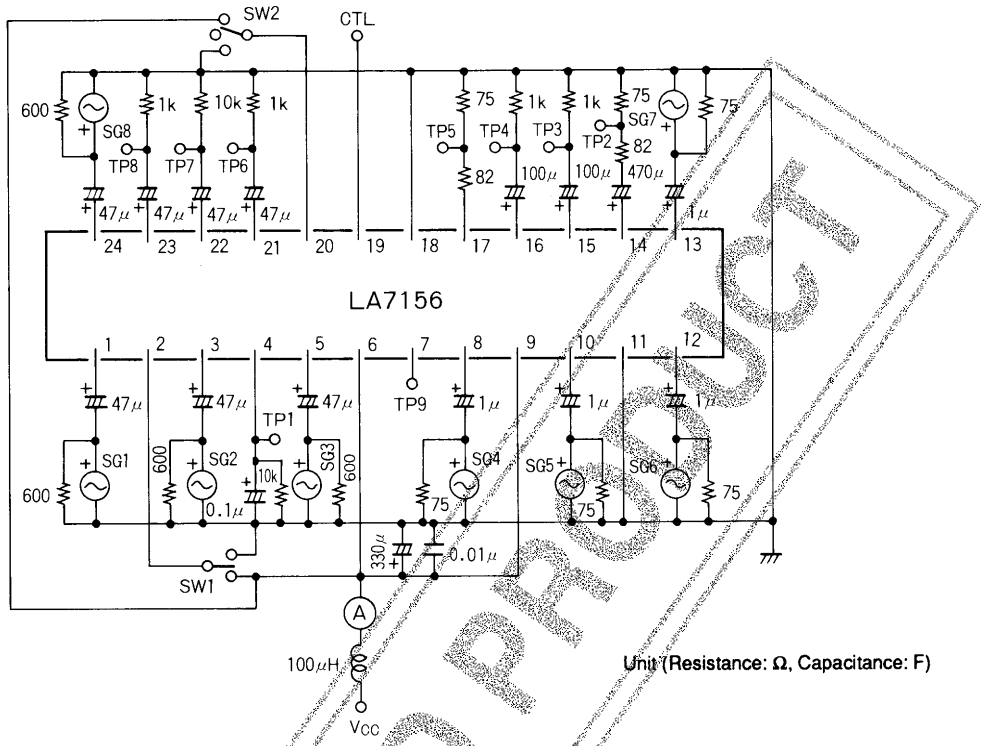
D1	D2	D3	D4	D5	P2	A.V.SW1	A.V.SW2	A.V.SW3	FSS out	Pin 7 out
L	—	—	—	—	H	B	A	B	H	L
L	—	—	—	—	L	B	A	B	L	L
H	L	L	L	L	H	B	C	B	H	L
H	L	L	L	L	L	A	C	B	L	L
H	H	L	L	L	H	A	C	A	H	H
H	H	L	L	L	L	A	C	A	H	H
H	L	H	L	L	H	A	A	A	L	H
H	L	H	L	L	L	A	C	A	L	H
H	H	H	L	L	H	A	A	A	H	H
H	H	H	L	L	L	A	C	A	H	H
H	L	—	H	L	H	A	A	B	H	L
H	L	—	H	L	L	A	B	B	L	L
H	H	—	H	L	H	A	A	B	H	L
H	H	—	H	L	L	A	B	B	H	L
H	—	—	—	H	H	A	*	*	H	*
H	—	—	—	H	L	A	*	*	H	*

Note: The previous state is retained even if another switch is changed.

Block Diagram and Recommended Circuit Diagram



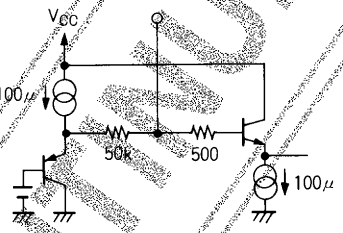
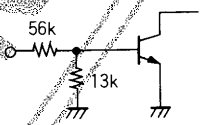
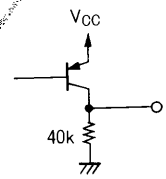
Test Circuit



Unit (Resistance: Ω, Capacitance: F)

Input and Output Pin Circuit Diagrams

Unit (Resistance: Ω, Current source: A)

Pin No.	Symbol	I/O circuit	DC voltage	Note
1 3 5 24	$A_{IN}1$ $A_{IN}2$ $A_{IN}3$ $A_{IN}4$		1/2 V_{CC} + 0.7 V	
2	DEC IN			
4	FSS OUT		V_{CC} – 0.2 V	
6	V_{CC}			

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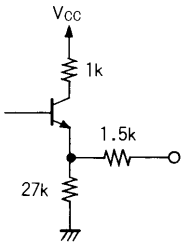
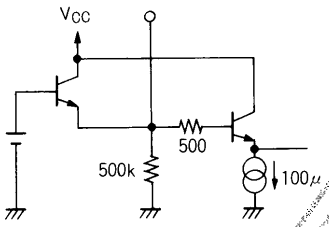
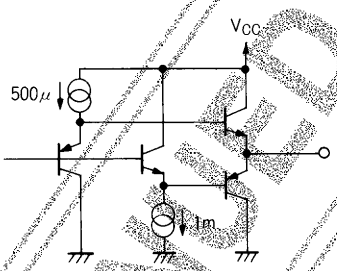
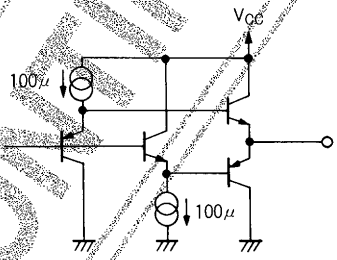
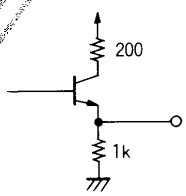
Unit (Resistance: Ω, Current source: A)

Pin No.	Symbol	I/O circuit	DC voltage	Note
7	SW3 CTL OUT		H: 5.0 V L: 0 V	
8 10 12 13	$V_{IN}1$ $V_{IN}2$ $V_{IN}3$ $V_{IN}4$		2.5 V	
9	DRIVER V_{CC}			
11	DRIVER GND			
14	$V_{OUT}1$		1.6 V	External connection
17	$V_{OUT}2$			
15	$V_{OUT}3$		1.6 V	Signal processing IC connection
16	$V_{OUT}4$		1.6 V	Signal processing IC connection
18	GND			

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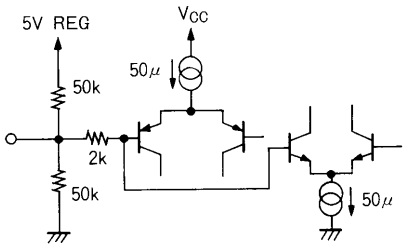
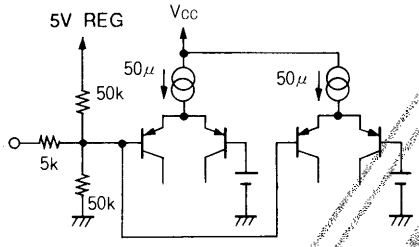
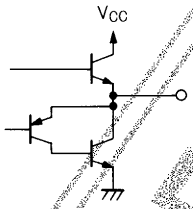
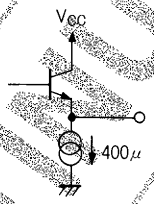
Unit (Resistance: Ω, Current source: A)

Pin No.	Symbol	I/O circuit	DC voltage	Note
19	D/C IN		2.5 V	
20	MODE CTL IN		2.5 V	
21	$A_{OUT}1$		1/2 V_{CC}	External connection
23	$A_{OUT}2$			
22	$A_{OUT}3$		1/2 V_{CC}	Signal processing IC connection