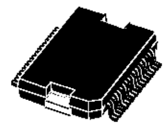
SGS-THOMSON MICROELECTRONICS

L9942

SUPER SMART MOTOR BRIDGE DRIVER

PRODUCT PREVIEW

- TWO 200mΩ RDSON INDEPENDENT HALF BRIDGES
- FULL PROTECTION AGAINST OVERTEMPERATURE, OVERCURRENT AND OVERVOLTAGE CONDITIONS
- NOMINAL 12 V SUPPLY VOLTAGE
- INTERNAL 5 V VOLTAGE REGULATOR
- VERY LOW OPERATIVE CURRENT CONSUMPTION
- INTERNAL LOW POWER RC OSCILLATOR FOR STANDBY OPERATION
- 7 CONTACT MONITORS, WITH CONTACT CLEANING FEATURES. (DEBOUNCING BY SOFTWARE)
- ST6 MICROCONTROLLER CORE
- 4K bytes ROM
- 128 bytes RAM
- 4 STANDARD CMOS I/O LINES
- DIGITAL WATCHDOG TIMER
- 8 BIT GENERAL PURPOSE TIMER WITH 7 BIT PRESCALER
- CAN CONTROLLER INCLUDING BUS LINE INTERFACE



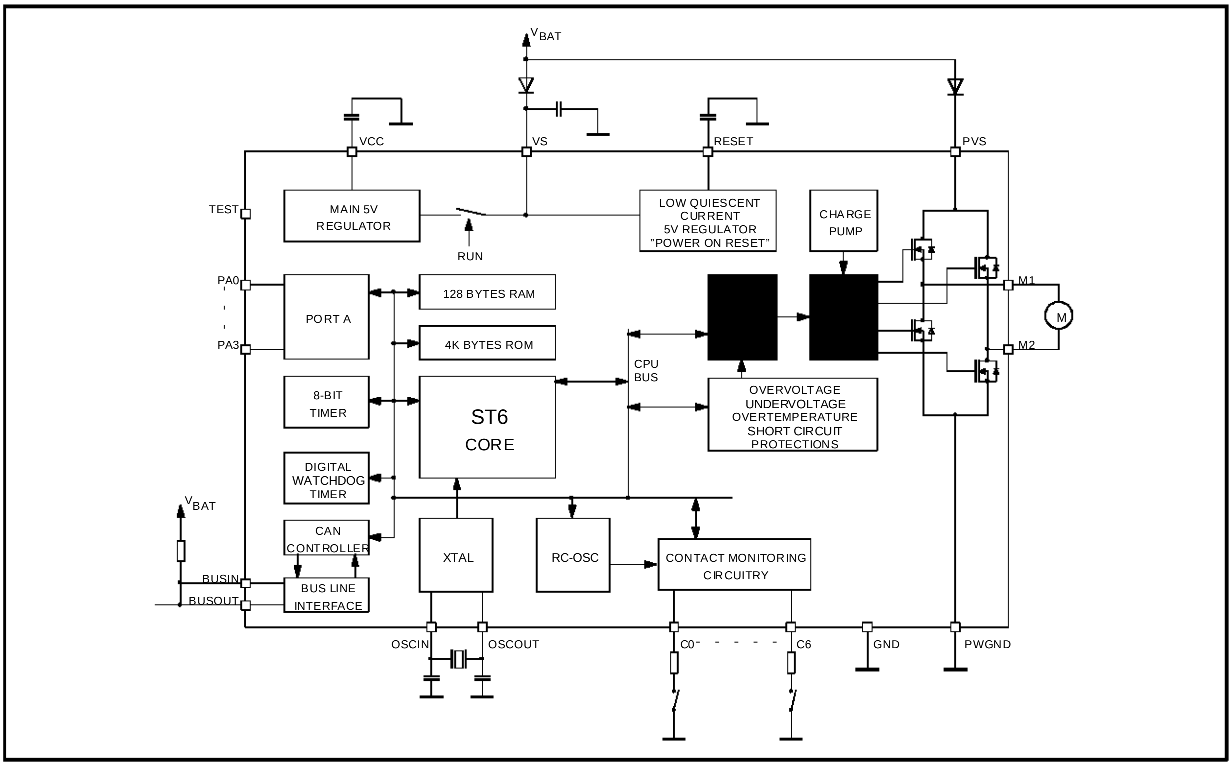
PowerSO36

ORDERING NUMBER:

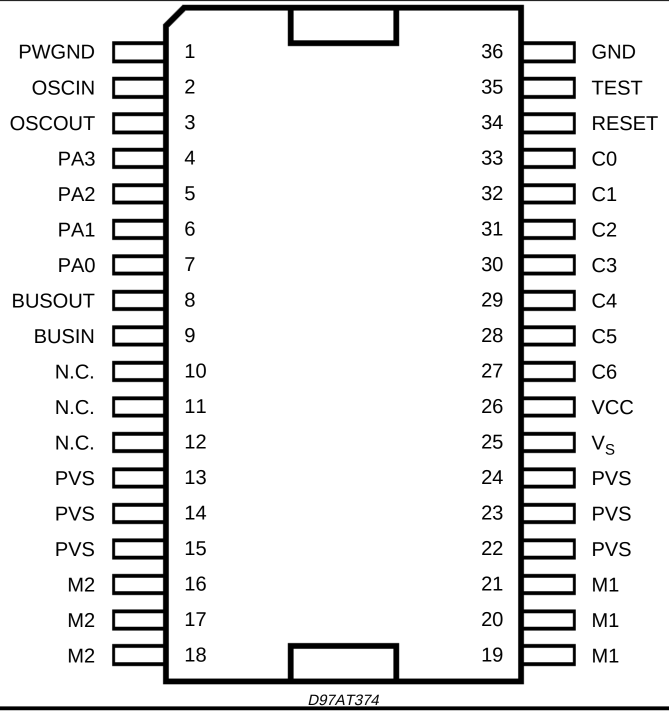
DESCRIPTION

The L9942 is a Super Smart Power device using BCD60III mixed technology combining an 8bit ST6 microcontroller and its periphery with a high current motor bridge, a voltage regulator, a 2.0A CAN bus (protocol handler and bus interface).

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTIONS

N.	Name	Function
1	PWGND	Power ground
2	OSCIN	XTAL oscillator input
3	OSCOUT	XTAL oscillator output
4 - 7	PA3 to PA0	Standard ST6-like CMOS I/O lines
8	BUSOUT	CAN output line. This output is connected to the CAN bus line interface.
9	BUSIN	CAN input line. This input is connected to the CAN bus line interface
13 - 15 22 - 24	PVS	Power supply for bridge
19 - 21 16 - 18	M1 M2	Half bridge 1, Half bridge 2 power outputs
25	VS	Power supply, connected to VBATT+ through reverse battery protection diode.
26	VCC	5V regulator output. Maximum external load supply current is 50mA
33 - 27	C0 to C6	Contact monitor inputs
34	RESET	Chip reset input/output, active low
35	TEST	Test mode input
36	GND	Digital ground

Quick Reference

The microcontroller is equipped with a 4K program ROM which can also be used for data table storage (shared with user program), a data RAM of 128 bytes, a watchdog with 64 different programmable reset times, a standard 8 bit timer with 7 bit programmable prescaler, a basic CAN controller plus line interface, a dynamic contact monitor with wake up facility for up to seven ground contacts, a standard digital 4 bit input/output port. Each digital I/O pin can individually be defined by software to work in one of the following modes:

opendrain output, push-pull output, input, input with pull-up or interrupt input with pull-up. The I/O port can be connected to the CAN module by software configuration.

The power section of the device consists of a DMOS full bridge (200mW each DMOS), directly controlled by the microcontroller. The power transistors are protected against short circuit, overvoltage, overtemperature. A charge pump without external components provides the gate voltage for the high side switches of the bridge.

The microcontroller and its periphery is supplied by a 5V regulator with low standby current which also generates a proper reset signal at power on/off.

A low power 32kHz RC oscillator provides a clock signal for the contact monitor circuitry as well as a real time wakeup counter. The clock signal for the CPU and the peripheral devices like timer, watchdog, CAN controller etc. is generated by a XTAL clock generator.

Description

The power part of the device consists of two identical independent DMOS half bridges. It is suited to drive resistive and inductive loads.

An integrated charge pump generates the high voltage required by the gate driving circuit for the upper DMOS transistors.

The Rdson of each of the 4 DMOS transistors is 200mW at room temperature.

The nominal current is 3.5A. A maximum current of 6A can be supplied.

A thermal sensing circuit issues one thermal warning flag at 130°C junction temperature and a second one at 150°C.

The ST6-core controls all operations of the power stage. Undervoltage, overvoltage short circuit and overtemperature conditions are reported to the CPU using dedicated error flags.

Overvoltage and short circuit conditions switch off the bridge immediately without CPU intervention. At overtemperature the CPU has to switch off the bridge by software.

The function of the flags is independent of the operation mode of the bridge (sink, source, Z).

POWER SUPPLY

DC Electrical characteristics. (T_{amb} = -40 to +85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VSsup	Operating supply voltage		8		24	V
IsSTOP	Supply current with microcontroller in STOP mode	No external loads, all switches open, RC oscillator running.		70	200	µA
IsRUN	Supply current with microcontroller in RUN mode.	No external loads, all switches open.			50	mA

Voltage regulator characteristics.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vsmin	Minimum input (VS) voltage		8			V
VoRUN	VCC Output voltage	Micro in RUN mode	4.75	5	5.25	V
IoRUN	Max output current from pin VCC	No loads connected to PORTA, micro in RUN mode	50			mA
VoSTOP	VCC Output voltage	Micro in STOP mode	4.5	5	5.5	V
IoSTOP	Max output current from pin VCC	Micro in STOP mode			1	mA
Imax	Current limitation	Micro in RUN mode	100			mA

POWER SUPPLY (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{Reset\ UD}$	Vcc for Reset undefined	Below this voltage Reset is not defined			1.5	V
$V_{Reset\ ON}$	Vcc low threshold for Reset on		4.5			V
$V_{Reset\ OFF}$	Vcc high threshold for Reset off				VCC-0.1	V

NOTE:
The IoRUN current is the maximum amount of current that the voltage regulator can deliver to external loads when the micro is not in STOP mode.
This means:
(current sunk from VCC pin) + (current sunk from PORT A pins) <= 50 mA.

Power section characteristics. (T_{amb} = -40 to +85°C; 8 < V_S < 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RdsON	Output resistance	Measured on M1 and M2 pins T_{amb} = 85°C, T_j = 150°C			360	mΩ
RdsON 25°C		Measured on M1 and M2 pins T_{amb} = 25°C, T_j = 25°C			200	mΩ
V_{smax}	Overvoltage protection threshold	Voltage measured on VS pin	16	17.5	19	V
V_{smin}	Undrvoltage protection threshold		7	7.5	8	V
tovi	Overvoltage protection intervention time			50		µs
I_{SHC}	Short circuit current	Short to VS, GND; load shorted	10			A
t_{SCPI}	Short circuit protection intervention time			10		µs
Thw1	Thermal warning threshold 1	Hysteresis 20°C		130		°C
Thw2	Thermal warning threshold 2	Hysteresis 20°C		150		°C

Power section registers.

The power section is controlled by the microcontroller through the following two registers (note that PAES and BUSIE bits in BPCR register are not related to the power section control):

BPCR **BRIDGE/PORT Control Register** (Address: E2h, Read/write) Status after reset: 00000000		
D0	**EN1**	Half bridge #1 enable
D1	**EN2**	Half bridge #2 enable
D2	**IN1**	Half bridge #1 (M1 output) control bit
D3	**IN2**	Half bridge #2 (M2 output) control bit
D4	**PAES**	Polarity selection for PORT A interrupts.
D5	**BUSIE**	BUS interface enable for PORT A0, 1
D6		not used, read as zero
D7	**PIE**	Power section diagnostic interrupt enable.

POWER SUPPLY (continued)

IN2,IN1,EN2, EN1: These bits control the status of the M1 and M2 power outputs, according to the following table:

Control Bits		Output Status
EN1	IN1	M1
0	X	Z
1	0	SINK
1	1	SOURCE
EN2	IN2	M2
0	X	Z
1	0	SINK
1	1	SOURCE

NOTE:
Z = HSD OFF, LSD OFF
SOURCE = HSD ON, LSD OFF
SINK = HSD OFF,LSD ON

EN1 and EN2 are automatically cleared at overcurrent condition (SC of BSR is high) switching off the bridge. To switch the bridge on again these bits have to be set by software.

PAES: This bit is used to select the edge sensitivity for the interrupts coming from PORTA. When SET, the interrupts occur on rising edge, when RESET they occur on falling edge.

BUSIE: This bit is used to multiplex CAN input/output lines to PORTA0,1 pins (see Fig. 6). When set PA0,1 operate as CAN I/O, when reset they can be used as normal I/O pins.

PIE: This bit, when SET and bit4 of the **IOR** register is also SET, enables the interrupts coming from the power section, i.e. from **UNV**, **OVT1**, **OVT2**, **SC and OV** bits. When RESET, these interrupts are disabled.

BSR **BRIDGE Status Register** (Address: E3h, Read/write) Status after reset: 00000000		
D0	**-**	Not used, read as zero
D1	**-**	Not used, read as zero
D2	**-**	Not used, read as zero
D3	**SC**	Short circuit flag
D4	**OV**	Overvoltage flag
D5	**UNV**	Undervoltage flag.
D6	**OVT1**	Overtemperature flag. 1
D7	**OVT2**	Overtemperature flag. 1

SC: This bit is set as soon as one of the two outputs (or both) are shorted to battery, ground or if the two outputs are shorted together (load shorted). This bit is RESET by software only. The rising edge causes on interrupt request on the interrupt line #0. Short circuit protection is realized with one sensing resistor for each half bridge. The voltage drop at these resistors is monitored in order to switch off the complete bridge if the current exceeds ISHC. When bit SC is set, the bridge enable bits EN1 and EN2 of bridge/port control register BPCR are cleared and the bridge is switched off. This clear function is dominant over any write from data bus by software (i. e. as long as SC is set, the bridge cannot be switched on). The bridge can be switched on again only after clearing bit SC. For this purpose enable bits EN1 or EN2 of register BPCR have to be set again.

OV: This bit is set if the battery voltage raises above V_{smax}. This bit is RESET by software only. The ris-

POWER SUPPLY (continued)

ing edge causes an interrupt request on the interrupt line #0. If the overvoltage situation is still present, OV is SET again. The bridge is switched off automatically at overvoltage.

UNV: This bit is SET as soon as the voltage on VS pin falls below the undervoltage threshold V_{smin}. This rising edge causes a interrupt request on the interrupt line #0. This bit is RESET by software only. If the undervoltage situation is still present, UNV remains SET. The bridge is not switched off automatically at undervoltage.

OVT1: This bit is SET as soon as the temperature of the chip exceeds 130°C. This rising edge causes an interrupt request on the interrupt line #0. This bit is RESET by software only. If the overtemperature situation is still present, **OVT1** remains SET. The bridge is not switched off automatically at overtemperature.

OVT2: This bit is SET as soon as the temperature of the chip exceeds 150°C. This rising edge causes an interrupt request on the interrupt line #0. This bit is RESET by software only. If the overtemperature situation is still present, **OVT2** remains SET. The bridge is not switched off automatically at overtemperature.

Warning: All power bridge flags are ored to form one interrupt request which is connected to edge sensitive interrupt input #0 (see Fig. 11). The interrupt request is stored in a flipflop which is automatically cleared when the interrupt service routine is entered. If other interrupt flags of the power bridge become active before the flag which caused the interrupt is cleared by software, the new request is not stored in the flipflop. In order not to miss any interrupt request it is recommended to check all interrupt flags of the power bridge after clearing the first flag. Then the interrupt service routine may be left.

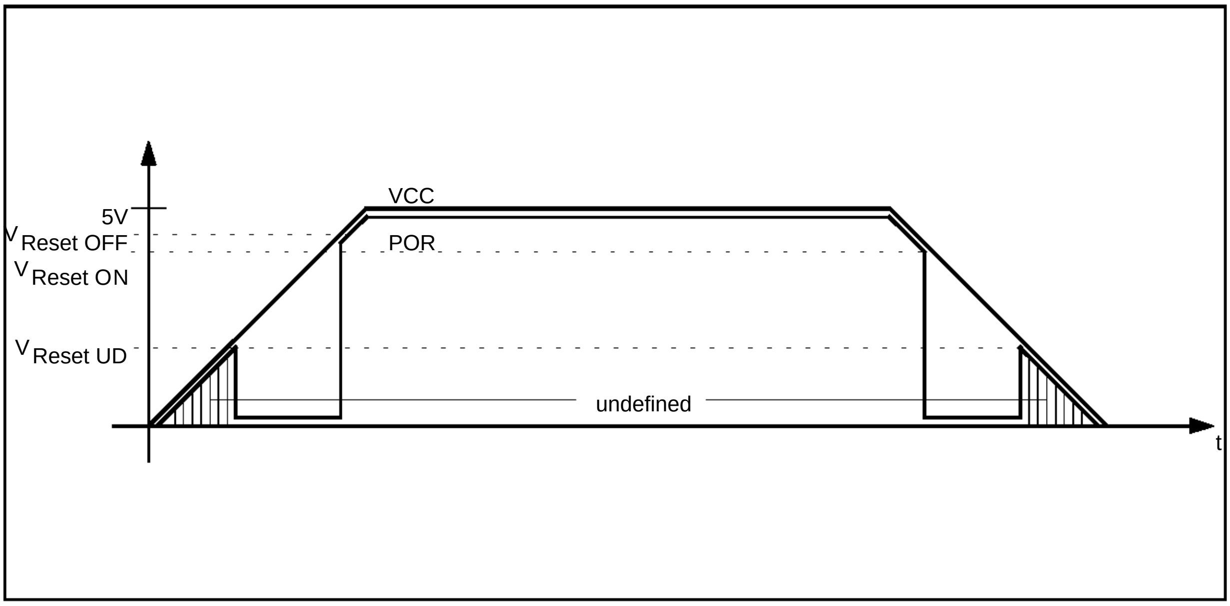
Voltage regulator

The on chip voltage regulator provides regulated 5V to supply the microcontroller and it's periphery. This voltage is available at pin VCC to supply external components and connect a capacitor to optimize EMI performance. The regulator has a normal and a standby operating mode. When the controller enters STOP mode, the regulator is switched to stand by operation. In this mode the power consumption as well as the ability to supply current (also to external devices) is drastically reduced. A return to RUN mode or a reset switches the regulator back to normal mode.

The voltage regulator also provides a reset signal POR at power up and power down to guarantee a well defined state of the device at undervoltage conditions (see Fig. 1).

POR activates the reset pull down transistor performing a complete chip reset. In the same way a reset

Figure 1. Power up/down characteristics

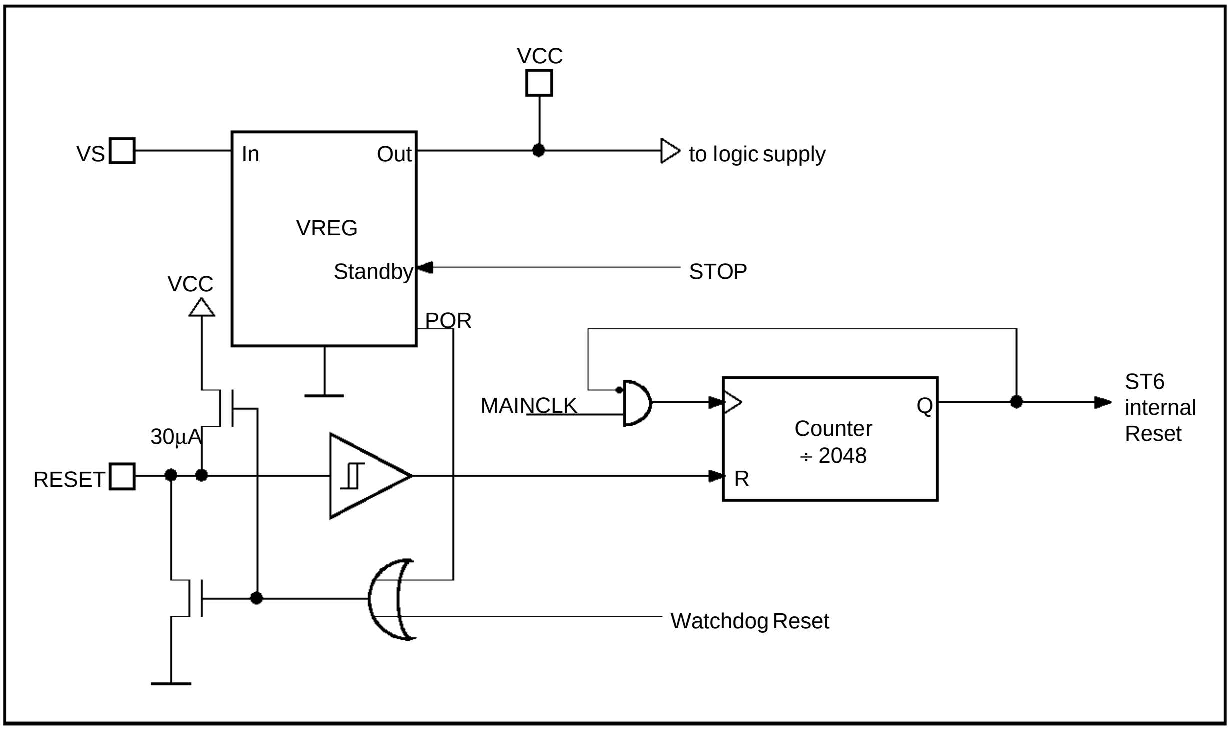


POWER SUPPLY (continued)

can be triggered by the watchdog or by external low level at RESET pin. If neither POR nor watchdog reset are activated, an internal current source of typ. 30µA is connected to the RESET pin. An external capacitor connected between RESET and ground can extend the power on reset period if required (see Fig. 2).

When the regulated power supply voltage VCC becomes sufficient at power up, the main oscillator starts

Figure 2. Voltage regulator and reset configuration.



to operate and generates the main clock signal MAINCLK. A counter provides a delay of 2048 clock cycles between the detection of high level at RESET pin and the release of the reset for the CPU and the peripheral logic modules. This is to allow the oscillator to be completely stabilized before the execution of the first instruction as well as a safe reset also for short pulses at RESET pin.

Reset characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{Reset\ L}$	Input low level voltage	RESET pin			$0.3V_{CC}$	V
$V_{Reset\ H}$	Input high level voltage	RESET pin	0.7VCC			V
$I_{Reset\ L,\ H}$	Input current	RESET pin $V_{CC} = 5V$ $V_{IN} = V_{CC1}$ $V_{IN} = V_{CC2}$ $V_{IN} = GND3$		 30	 1 1 50	 µA mA µA

1) Leakage current
2) Internal reset by watchdog or POR
3) Pull up current source

MICROCONTROLLER SECTION

General description

This section comprises the following macrocells:

ST6 CORE
128 bytes RAM
4 Kbytes ROM
8-BIT TIMER (TIMER1)
Digital WATCHDOG/TIMER
I/O PORT A (4 I/O lines)

For the explanation of the above mentioned blocks please refer to the following standard ST6 documentation (Note that any reference to external pins and electrical characteristics does not hold. In case of different information, the correct ones are those in this document.

Table 1. Data Memory Space.

DATA RAM		000h ± 03Fh
DATA ROM WINDOW AREA 2)		040h ± 07Fh
X REGISTER	X	080h
Y REGISTER	Y	081h
V REGISTER	V	082h
W REGISTER	W	083h
DATA RAM		084h ± 0BFh
RESERVED		0C0h
PORT A DATA REGISTER	DRA	0C1h
RESERVED		0C2h0C4h
PORT A DIRECTION REGISTER	DDRA	0C5h
RESERVED		0C6h,0C7h
INTERRUPT OPTION REGISTR 1)	IOR	0C8h
DATA ROM WINDOW REGISTER 1)	DWR	0C9h
RESERVED		0CA0 ± CCh
PORT A OPTION REGISTER	ORA	0CDh
RESERVED		0CEh ± 0D1h
TIMER 1 PRESCALER REGISTER	PSC1	0D2h
TIMER 1 COUNTER REGISTER	TCR1	0D3h
TIMER 1 STATUS/CONTROL REGISTER	TSCR1	0D4h
RESERVED		0D5h-0D7h
WATCHDOG REGISTER	DWDR	0D8h
RESERVED		0D9h
BUS INTERFACE REGISTER	BIR	0DCh
OSCILLATOR CONTROL REGISTER	OSCR	0DDh
RESERVED		0DEh-0DFh
CONTACT MONITORS BIASING REGISTER	CMBR	0E0h
CONTACT MONITORS STATUS REGISTER 2)	CMSR	0E1h
BRIDGE/PORT CONTROL REGISTER	BPCR	0E2h
BRIDGE STATUS REGISTER	BSR	0E3h
RESERVED		0E4h-0E7h
CONTACT MONITOR INTERRUPT REGISTER	CMIR	0E8H
CONTACT MONITOR COMPARE REGISTER	CMCR	0E9h
RESERVED		0EAh-0EFh
CAN TRANSMIT IDENTIFIER HIGH	TIDH	0F0h
CAN TRANSMIT IDENTIFIER LOW	TIDL	0F1H
CAN TRANSMIT DATA HIGH	TDH	0F2h
CAN TRANSMIT DATA LOW	TDL	0F3h
CAN RECEIVE IDENTIFIER HIGH	RIDH	0F4h
CAN RECEIVE IDENTIFIER LOW	RIDL	0F5h
CAN RECEIVE DATA HIGH	RDH	0F6h
CAN RECEIVE DATA LOW	RDL	0F7h
CAN IDENTIFIER MASK	IDM	0F8h
CAN IDENTIFIER FILTER	IDF	0F9h
CAN TRANSMIT ERROR COUNTER	TEC	0FAh
CAN RECEIVE ERROR COUNTER	REC	0FBh
CAN STATUS REGISTER	CSTR	0FCh
CAN CONTROL REGISTER	CCTR	0FDh
CAN TEST REGISTER	CTER	0FEh
ACCUMULATOR	A	0FFh

1) write only; 2) read only.

MICROCONTROLLER SECTION

Contact monitors (C0 ... C6)

The device provides 7 contact monitoring pins suited to sense the status of 7 switches to ground. An external resistor in series to the inputs is used to set the current level and protect the inputs from external EMI pulses. External series resistor should not be lower than 100Ω. The value of the series resistor has to be calculated using the following formula:

Example: V_S = 13.5V

I_O = 20mA ⇒ R_{prot} = 175Ω

with R_{DSON} = 500Ω

The maximum current (short circuit) for each contact monitor is 50mA (at V_S = 15V).

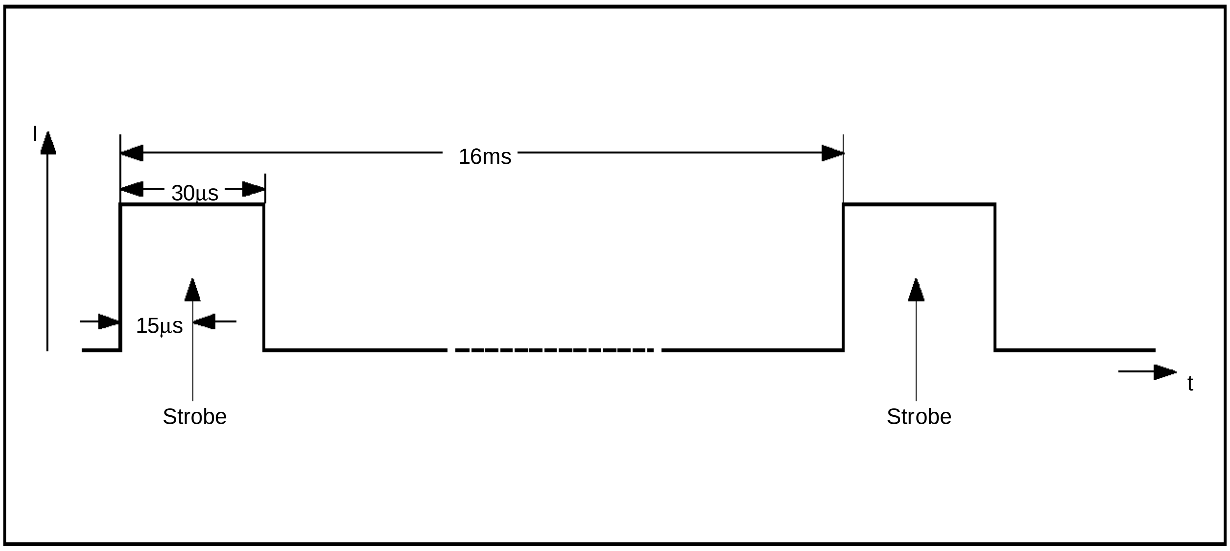
Contact Monitor characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CMSC}	Short circuit current	Short to GND, V_S = 15V	10	30	50	mA
I_{CMTH}	Input threshold current		0.5	1.5	2.5	mA
I_{CMHY}	Input threshold hysteresis		8	10	12	% of ICMTH

In order to reduce power consumption, a dynamic monitoring is implemented as described below:

The contact monitor consists of a strobe decoder, seven identical contact monitor channels, an interrupt logic. The contact monitor is permanently supplied with a 32kHz clock signal SBCLK from standby oscillator. This signal is also active in STOP mode of the controller keeping active the contact monitoring. The strobe decoder generates control signals for the channel logic in order to sense one contact after the other as shown below. Each channel is activated every 16ms for about 30µs (precisely one period of standby oscillator clock) and strobed after 15µs.

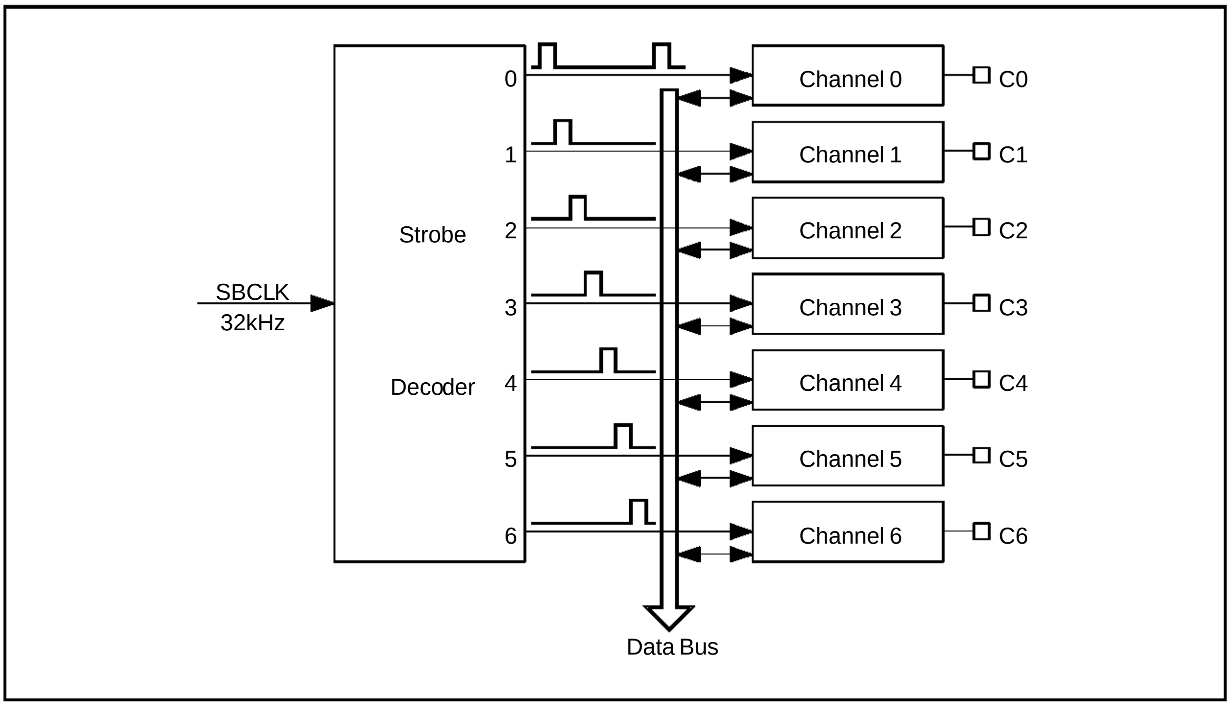
Figure 3. Sensing current for one channel.



This scheme allows 15µs of settling time for the sensing current at the external contacts. The duty cycle of the contact current is 1/512.

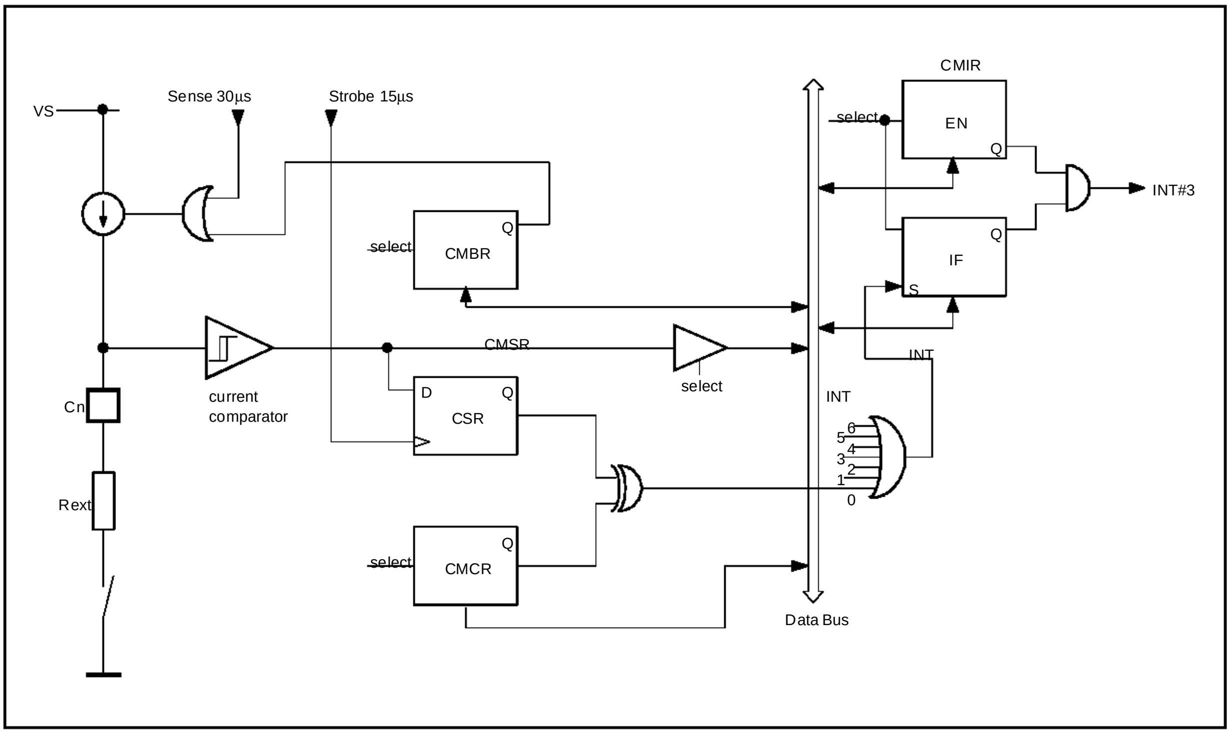
MICROCONTROLLER SECTION

Figure 4. Contact monitor structure and strobe signals.



The seven channels are activated in sequence as shown in fig. 4 to complete one cycle in 16ms. The structure of one channel is shown in fig. 5.

Figure 5. Channel and interrupt logic structure.



MICROCONTROLLER SECTION

Battery voltage VS is applied to the contact monitor pin Cn by the sense signal from strobe generator. The contact current is monitored by the current comparator. If the current is below the threshold level ICMTH a logic zero is generated, if the current is above I_{CMTH} a logic one is generated and sampled in contact sample register CSR with the strobe signal. The content of CSR is permanently compared with the content of contact monitor compare register CMCR.

The purpose of this register is to store the last contact status (written by software). Whenever a contact changes from its previous state a mismatch between CSR and CMCR will occur and an interrupt is generated. The controller has to read the contact status now. As CMSR is valid for 30µs during sensing only (and this is completely asynchronous to CPU operation) the controller can sense the contact permanently by setting contact monitor biasing register CMBR. If a bit is set the corresponding contact is sensed permanently and can be read by the CPU via CMSR independently from the dynamic sensing mechanism. When the CPU has determined the contact which changed its state the corresponding bit in CMCR has to be changed in order to clear the interrupt request.

The interrupt lines from all channels are ored and can set the interrupt flag IF in contact monitor interrupt register CMIR. This flag can be masked with enable bit EN.

When all bits in CMCR and CSR match the interrupt signal INT is cleared and the flag IF can be reset under software control. As long as at least one channel interrupt INTn is active the interrupt flag IF cannot be cleared as the set function is dominant.

This guarantees that no contact state change can be lost. The interrupt output of the contact monitor is connected to level sensitive interrupt input #3 of the CPU. Therefore the interrupt has to be cleared before the interrupt service routine is left.

The CPU controls the operation of the 7 contact monitors, using 4 registers.

- Status register : read only (one for each channel)

MSB							LSB	
bit7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	CMSR

bit7 is always read as zero
CMSR holds the status of those contacts which are determined in CMBR to be sensed permanently. The other bits are not valid and may change randomly.
Set means contact is closed, Reset means contact is open.

- Interrupt register : 2 bits)

EN	IF	n.i.	n.i.	n.i.	n.i.	n.i.	n.i.	CMIR

bit7 is always read as zero
this register is cleared by reset.

EN: Interrupt enable bit: set/reset by the CPU, enables or disables the Contact Monitor Interrupt.

IF: read/write interrupt flag, set if one status bit changes, reset by CPU only

- Biasing register: 7 bit register (one for each channel) set/reset by CPU, enables permanent contact biasing. Set means contact is permanently biased.

bit7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	CMBR

bit7 is always read as zero
this register is cleared by reset.

- Compare register: 7 bit register (one for each channel) set/reset by CPU. This register is permanently compared with CSR (strobed contacts)

bit7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	CMCR

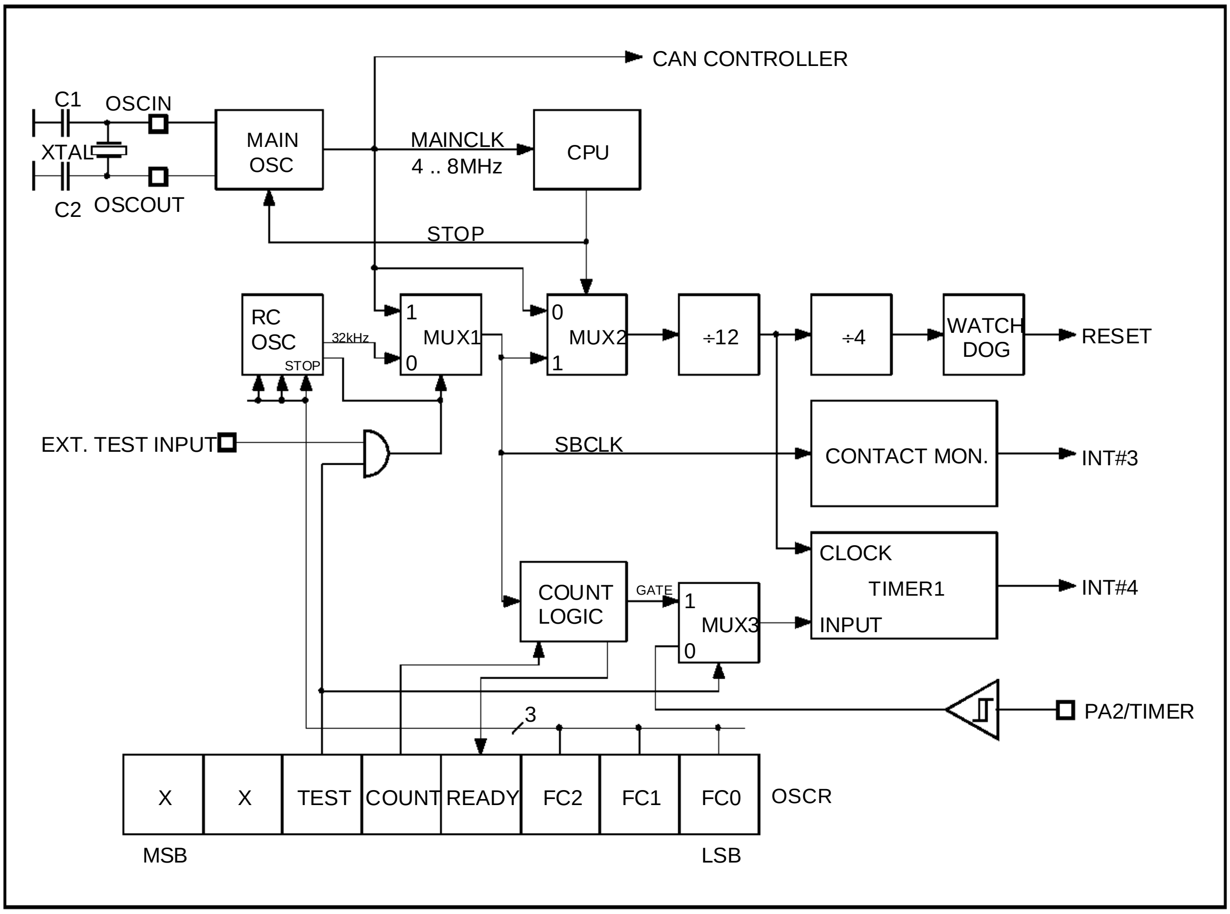
bit7 is always read as zero
this register is cleared by reset.

Oscillators

The L9942 has two oscillators to provide appropriate clock signals in RUN and STOP mode (see Fig. 6).

MICROCONTROLLER SECTION (continued)

Figure 6. System clocking scheme.



The CPU and digital logic is supplied with a clock signal MAINCLK from main oscillator using an external xtal or ceramic resonator. Two external capacitors C1 and C2 of 12 - 22pF each (according to the recommendation of the resonator supplier) have to be connected to the oscillator pins. OSCIN is the input, OSCOUT is the output of the main oscillator. Also an external clock signal can be applied to OSCIN to clock the device. Maximum frequency of the main oscillator is 8MHz.

For standby operation the main oscillator is switched off by execution of a STOP instruction of the application software. After this instruction the CPU is in stop mode:

- no operation is performed
- all registers and memory cells keep their content
- voltage regulator is switched to standby mode
- current consumption is minimized
- contact monitors, TIMER1, watchdog are supplied with standby clock SBCLK

This state can be left only by interrupts (contact monitors, I/O, CAN-controller, timer) or by reset (external, voltage regulator, watchdog).

In order to keep some basic functions in standby mode there is a separate low power RC oscillator. The oscillator frequency of about 32kHz is generated using internal components only. This standby oscillator operates permanently and cannot be stopped. It's output signal SBCLK supplies the contact monitor circuitry as well as TIMER1 and watchdog (in STOP mode only). This configuration allows periodic CPU wake up from STOP mode by timer interrupts as well as watchdog operation also in STOP mode. Therefore in case of failure of the wake up mechanism the STOP mode is left by a watchdog generated reset.

MICROCONTROLLER SECTION (continued)

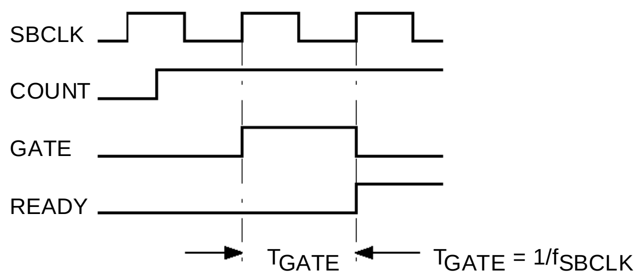
Multiplexer MUX1 is used for test purposes. In normal operation the 32kHz clock signal is passed to signal SBCLK. In test mode however (pin TEST=high) the main clock can be supplied to the peripheral components and the RC oscillator can be stopped by setting bit TEST of oscillator control register OSCR.

Multiplexer MUX2 is used to select main clock or standby clock for TIMER1 and watchdog under control of signal STOP which is active in STOP mode of the CPU.

The RC oscillator is designed to minimize frequency offset caused by temperature, supply voltage, manufacturing tolerances. Nevertheless the deviation from 32kHz might be larger than required and tuning will become necessary. For that purpose the RC oscillator frequency can be measured and adjusted under control of the CPU as described in the following (see also fig. 7).

The device is in normal operation mode (pin TEST=low). The standby oscillator is controlled by oscillator control register OSCR. Setting bit TEST of OSCR will connect the TIMER1 input with signal GATE via MUX3. The timer now has to be initialized and programmed to input gated mode. In this mode it will count clock pulses ($f_{MAINCLK}$ ±12) as long as its input is high. If bit COUNT of OSCR is set now, the block COUNT LOGIC generates one pulse at signal GATE with the length of exactly one period of the RC oscillator clock signal. Therefore the timer will count main/oscillator pulses for one period of the standby clock. At the falling edge of signal GATE bit READY of OSCR is set indicating the end of the measurement. Now the timer can be read by the CPU to determine the actual frequency of the standby oscillator. Bits TEST, COUNT, READY can be cleared now. As long as COUNT is set, READY can not be cleared by software.

Figure 7. Signals of RC oscillator count logic.



Timer resolution at $f_{MAINCLK}$ = 8MHz is 12 · 125ns = 1.5µs.

Measurement of a clock period of TGATE = 1/32kHz = 31.3µs therefore shows a resolution of about 5%.

The RC oscillator has a nominal frequency of 32kHz and can be adjusted with frequency control bits FC2, 1, 0. Adjustment is performed in steps of 4kHz (i. e. 12.5%) from 16kHz to 44kHz as shown in the following table.

FC2	FC1	FC0	f_{RCOSC}/kHz
0	0	0	44
0	0	1	40
0	1	0	36
0	1	1	32
1	0	0	28
1	0	1	24
1	1	0	20
1	1	1	16

Register OSCR is cleared at system reset. Therefore the highest frequency of RC oscillator is selected. Bits 5 and 6 are not implemented. They are read as zero.

MICROCONTROLLER SECTION (continued)

TIMER1

The interrupt output of TIMER1 is connected to the level sensitive interrupt input I4 of the core (start address FF0h). So the interrupt has to be cleared before the interrupt service routine is left.

The autoreset function is not implemented.

TIMER1 can get its clock signal from two internal and one external sources (see Fig. 6 and 8).

Internal sources (output mode).

In RUN and WAIT mode the timer is supplied with a clock signal derived from main oscillator. Its frequency is $f_{MAINCLK}/12$. In STOP mode it is supplied with a clock signal derived from standby oscillator with the frequency $f_{SBCLK}/12$. Therefore the timer can also be operated in STOP mode. A timer interrupt can finish STOP mode. The max. timer interval is $12 \times 2^{15}/f$. This is 49ms in RUN and WAIT mode for $f_{MAINCLK}$ = 8MHz and 12s in STOP mode for f_{SBCLK} = 32kHz.

External source (input mode, input gated mode)

The timer input can be connected with I/O port PA2 or oscillator count logic via multiplexer MUX3. This multiplexer is controlled by bit TEST of oscillator control register OSCR. If this bit is cleared the timer input is connected with PA2 input schmitt trigger. With PA2 configured as input TIMER1 can be operated in input mode or input gated mode.

If bit TEST of OSCR is set the timer input is connected to output GATE of oscillator count logic. In this configuration TIMER1 can be operated in input gated mode in order to measure the clock period of RC oscillator as described above.

There is no output driver available for TIMER1.

WATCHDOG

The ST6WD1 is used to reset the device after a certain period of time if it is not refreshed.

The watchdog is always active and cannot be disabled. In RUN and WAIT mode of the CPU, when the main oscillator works, the watchdog is supplied with a clock signal with the frequency $f_{MAINCLK}$ /48. Therefore the period of the watchdog can be programmed in 64 steps from 1.536ms up to 98ms for a mainclock of 8MHz (see Fig. 5).

In STOP mode of the CPU the watchdog is supplied with a clock signal derived from RC oscillator. It's frequency is $f_{SBCLK}/48$. With f_{SBCLK} = 32.768kHz the period of the watchdog can be programmed in 64 steps from 375ms up to 24 seconds.

After a reset, ST6WD1 is set to it's longest period (98msec. for fMAINCLK = 8MHz, in RUN and WAIT mode; 24 sec in STOP mode).

ST6WD1 is able to produce a SW-Reset (bit0 set to "1", bit1 to "0").

Dataspace address of watchdog register WDT is D8h.

I/O Port

Pins PA0 ... PA3 are of type IOP4.

The polarity of the interrupt output of the port can be selected by bit PAES in Register BPCR.

If this bit is cleared, the I/O interrupt output is not inverted and an interrupt can be generated on falling edge or low level (depending on bit6 of interrupt option register IOR). If this bit is set, interrupts are generated on rising edge or high level.

If more then one port pin is programmed as interrupt input, overlapping interrupts may occur. This situation has to be avoided if edge sensitivity is selected. Otherwise interrupt events might be lost.

Pins PA0 and PA1 may be also used to connect an external line interface circuit with the on-chip CAN Controller.

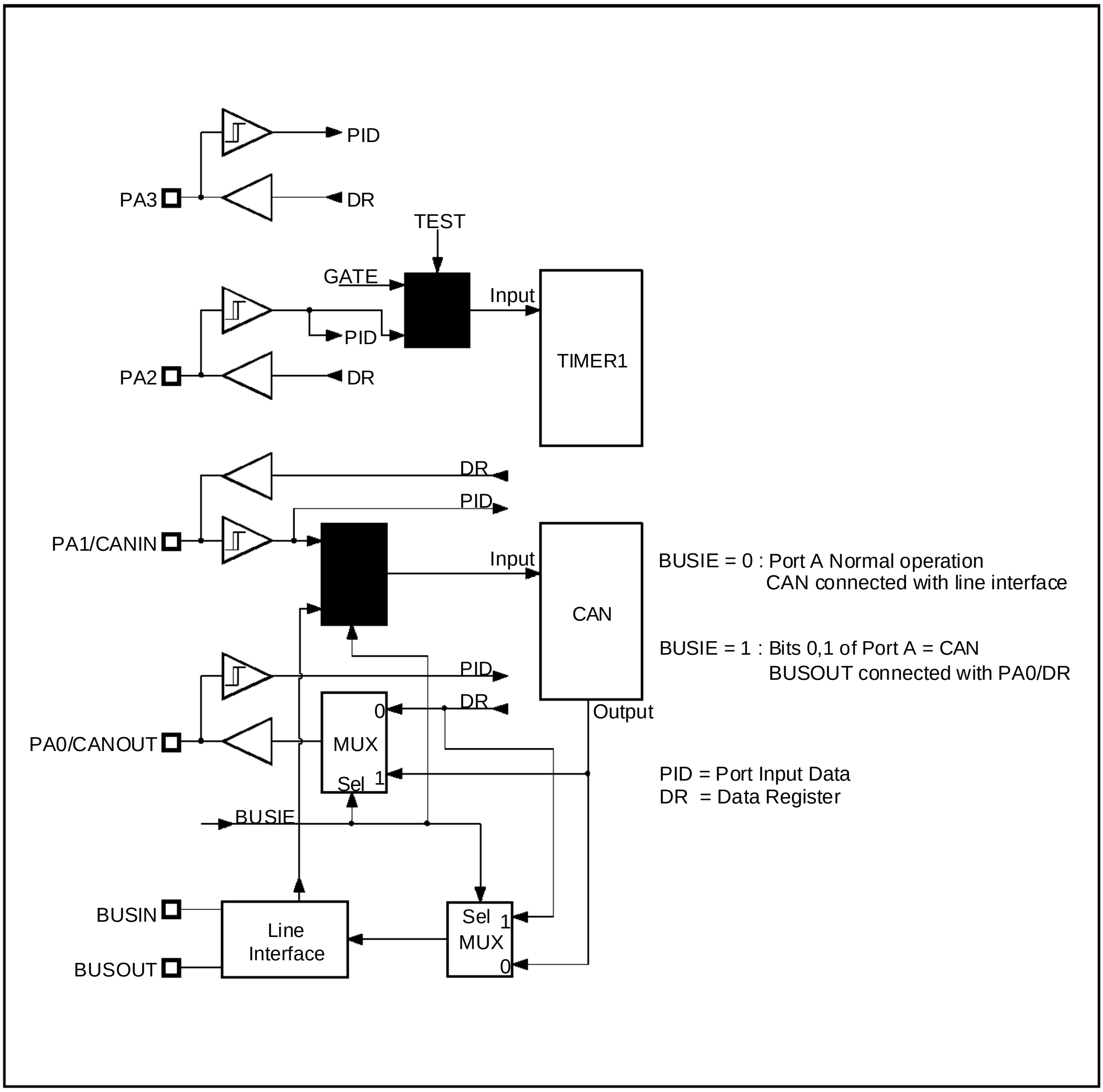
Bit BUSIE of the bridge/Port Control Register BPCR (E2H) is used for multiplexing Port A Data Register bits 0 and 1 with the CAN Module input and output, as shown in Fig. 8.

MICROCONTROLLER SECTION (continued)

If BUSIE is cleared PA0 and PA1 operate as normal I/O pins. IF BUSIE is set the input schmitt trigger of PA1 is connected with data input of the CAN controller. The data output of the CAN controller is connected with the output driver of PA0 as well. For this mode of operation PA0 has to be programmed as output, PA1 as input. In this operation mode port A data register bit 0 is connected with line interface open drain output buffer. Therefore BUSOUT is directly controlled by port A data register bit 0.

Pin PA2 may also be used as external input for TIMER1. For this purpose PA2 has to be programmed as input (with or without pull up / interrupt) and bit TEST of oscillator control register OSCR has to be cleared.

Figure 7. Signals of RC oscillator count logic.



With BUSIE = 1 bit PA1 has to be configured as Input, bit PA0 as output.

MICROCONTROLLER SECTION (continued)

CAN Controller and Interface

The CAN controller module ST6-CAN1 handles all frame types according to CAN Specification 2.0A. The module is supplied with a clock signal derived from MAINCLK. The division factor N of the clock prescaler (see Fig. 9) defines the baud rate of the module as shown below. N is fixed by mask option to 2.

	N	baud rate / kbit/sec
$f_{MAINCLK}$ = 8.0MHz	1	125
	2	62.5
	3	31.25
	4	15.625

With this option a trade off between speed and EMI performance of the bus can be achieved.

The interrupt output of the CAN controller is ored with bus interface interrupt and connected with interrupt input #2. Bit 5 of interrupt option register IOR has to be cleared.

The CAN controller input and output signals are accessible in two ways: via bus line interface or via I/O ports PA0 and PA1 (see Fig. 8). This is controlled with BUSIE of register BPCR (see section I/O Port).

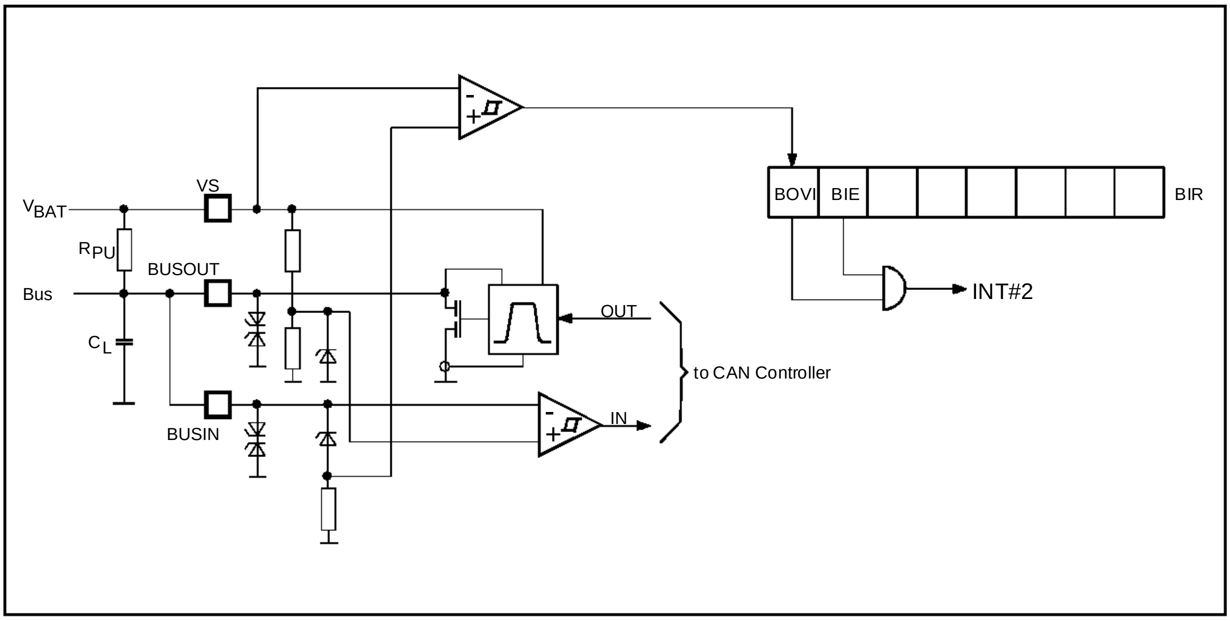
The input pin BUSIN an the output pin BUSOUT of the CAN line interface can be directly connected to a single wire VBAT compatible serial bus.

The slew rate SRBUSOUT of the bus output driver is 3 - 6V/µs. It can be adjusted to 0.5 ·, 1.5 ·, 2.5 · SR by mask option. The bus input line BUSIN has a supply voltage dependent threshold together with sufficient hysteresis to suppress line spikes. BUSIN and bus output line BUSOUT pins are protected against overvoltage, short to GND and VS and can also be driven beyond VS and GND. During lack of VS or GND the output shows high impedance characteristic.

If the voltage at bus input BUSIN exceeds Vin ov an overvoltage condition is recognized and stored in interrupt flag BOVI of bus interface register BIR. This bit can generate a maskable interrupt request at interrupt input #2. BOVI is RESET by software only. If the overvoltage situation is still present, BOVI remains set. Bits 0 ... 5 of register BIR are not implemented. They are read as zero. This register is cleared at system reset.

Suppressing all 4 classes of "Schaffner" signals BUSIN and BUSOUT pins can be loaded with short energy pulses of max. ±0.2mJ. All these features together with a high possible baud rate of 125kbaud, controlled output slope for low EMI and a wide operating range make this interface suitable for automotive bus system.

Figure 9. CAN Bus Line Interface Block Diagram.

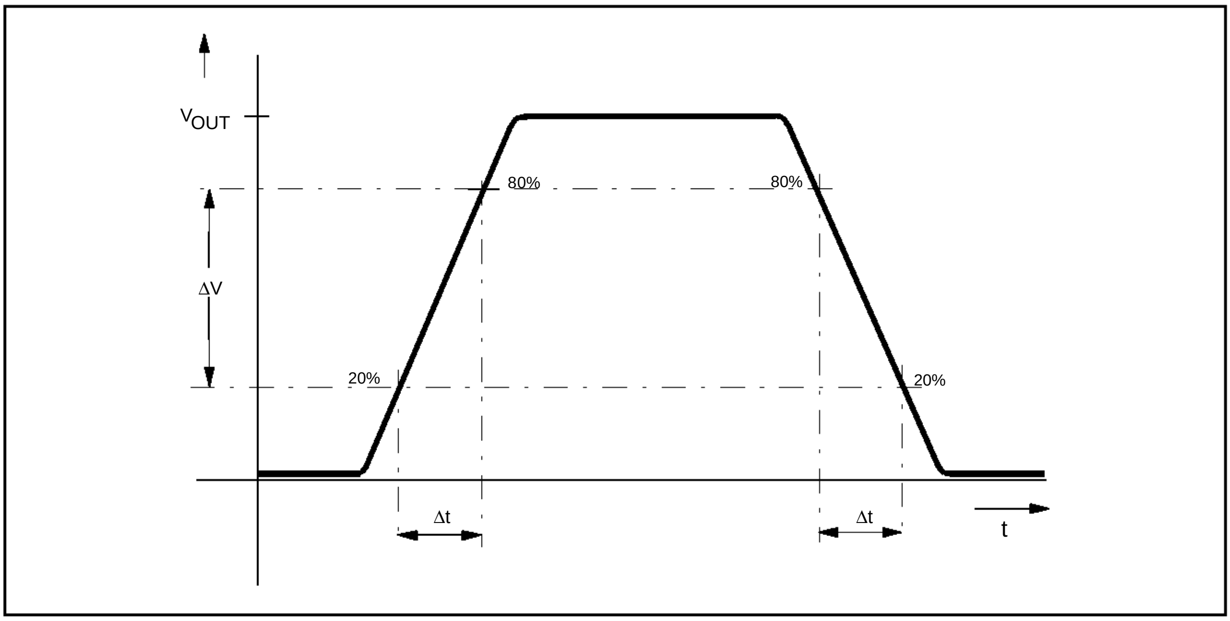


MICROCONTROLLER SECTION (continued)

CAN Bus Line Interface Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{in\,low}$	Input voltage LOW state	8V ≤ VS ≤ 45V	-24		0.53 VS	V
$V_{in\,high}$	Input voltage HIGH state	8V ≤ VS ≤ 45V	0.56 VS		45	V
$V_{in\,hys}$	Input threshold hysteresis	V in high - $V_{in\,low}$		0.03 VS	0.8	V
V_{inov}	Input overvoltage threshold		5.4 + VS	6.0 + VS	6.4 + VS	V
$I_{in\,off}$	Input current	-24 ≤ V_{in} ≤ 45V VS ≥ 0V or VS = open	-5	2	25	µA
R_{outon}	Output ON impedance	@ VS ≥ 6.5V output on I_{out} ≥ 7mA		10	30	Ω
I_{outsc}	Short circuit current		30	60	100	mA
$C_{BUSIN,BUSOUT}$	Transmission frequency	VS = 16V (external loads) R_{PU} = 510Ω, C_L = 1nF	50	100		kHz
SR_{BUSOUT}	slew rate	for the definition of SR see Fig. 10 VS = 12V (external loads) R_{PU} = 510Ω, C_L = 1nF	3		6	V/µs

Figure 10. BUSOUT slew rate definition.



RAM

The RAM consists of two macrocells of 64 bytes each. One page is located in the address range from 80h - BFh and also contains the registers X, Y, V, W. The other page of 64 bytes is located in the address range from 00h - 3Fh.

MICROCONTROLLER SECTION (continued)

Table 2. Program space.

RESERVED *)	0000h ÷007Fh
USER PROGRAM ROM (3872 BYTES)	0080h ÷0F9Fh
RESERVED *)	0FA0h ÷0FEFh
INTERRUPT VECTOR #4	0FF0h,0FF1h
INTERRUPT VECTOR #3	0FF2h,0FF3h
INTERRUPT VECTOR #2	0FF4h,0FF5h
INTERRUPT VECTOR #1	0FF6h,0FF7h
RESERVED *)	0FF8h,0FFBh
INTERRUPT VECTOR #0	0FFCh,0FFDh

*) This area is reserved for test purpose and is not available for the user.

INTERRUPTS STRUCTURE

Interrupt Option Register IOR

Bit 6 of register C8h is used to select negative edge (B6 = 0) or low level (B6 = 1) I1 interrupt sensitivity.

Bit 5 of register C8h is used to select negative edge (B5 = 0) or positive edge (B5 = 1) I2 interrupt sensitivity.

Bit 4 of register C8h is used to disable (B4=0) all maskable interrupts.

Register C8h is cleared during reset.

There are no read and single bit instructions possible.

See also interrupt circuit diagram (Fig. 11).

Test mode pin TEST has to be low for normal operation.

Interrupts

Non maskable interrupt input IO is connected to the power bridge flags (start address FFCH).

I1 is connected to PORT A (start address FF6H).

I2 is connected to Bus Interface and CAN Controller (start address FF4H).

I3 is connected to Contact Monitor (start address FF2H).

I4 is connected to TIMER1 (start address FF0H).

The interrupt characteristics of I/O port A can be programmed in four different modes.

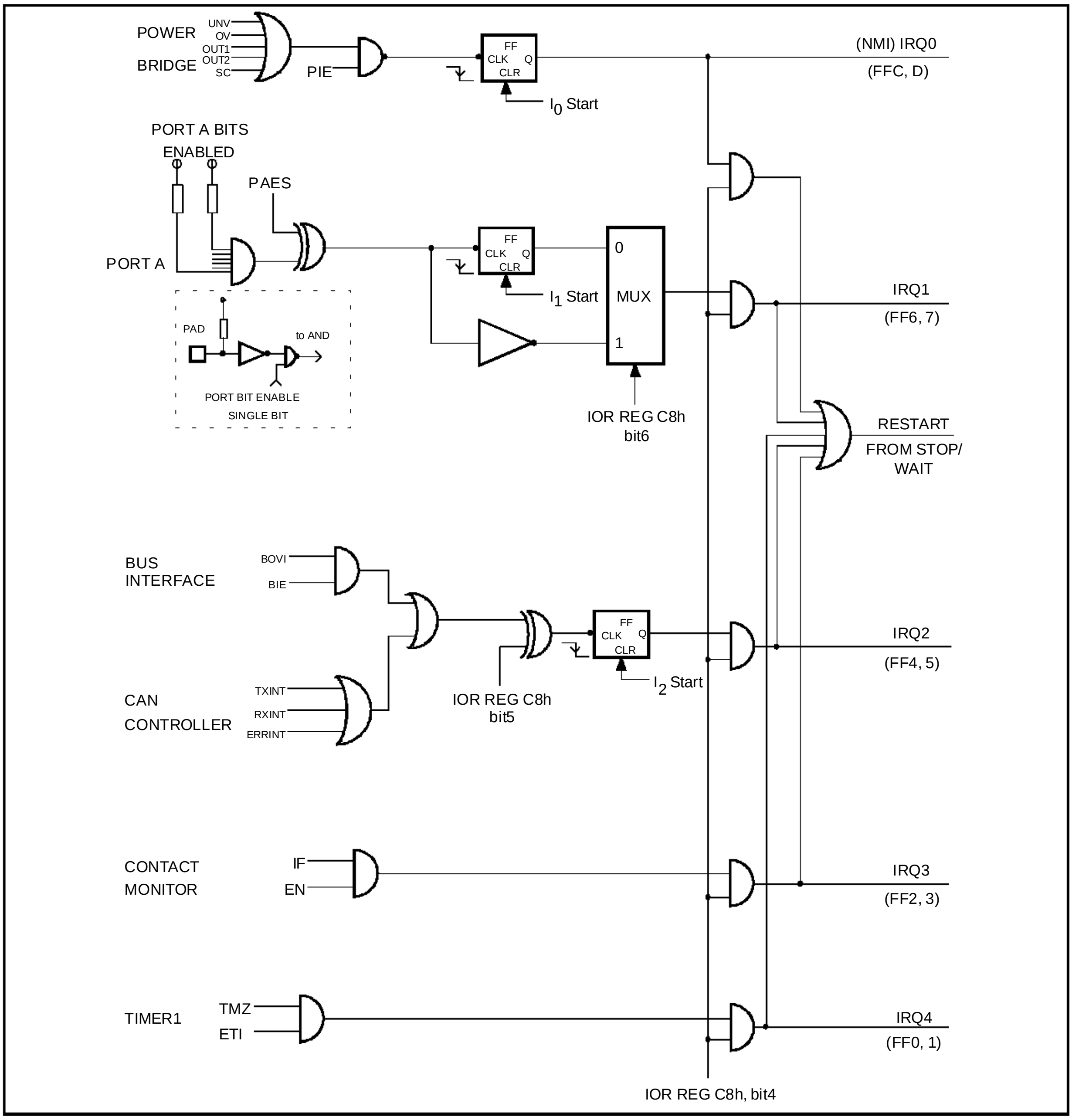
Interrupt polarity is selected by bit PAES of register BPCR, interrupt sensitivity is controlled by bit 6 of register IOR (see following table 3).

Table 3. I/O port interrupt selection.

PAES	IOR6	Port A interrupt
0	0	falling edge
0	1	low level
1	0	rising edge
1	1	high level

MICROCONTROLLER SECTION (continued)

Figure 11. Interrupt circuit diagram.



APPENDIX

1. Core Description ST6 - Core N SD70K F 024
2. Timer Description ST6 - TIM1 SD70K F 029
3. Watchdog Description ST6 -WD1 SD70K F 030
4. Port Description ST6 - IOP4 SD70K F 038
5. 64 Byte RAM Description ST6 - RAM64N SD70K F 058
6. Basic CAN Description ST6 CAN1

POWERSO36 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.025	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8°(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
-Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
Critical dimensions are "a3", "E" and "G".